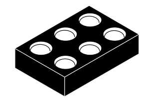
Low On-Resistance, Slew-Rate-Controlled Load Switch

FPF1038



WLCSP6 1.5x1.0x0.582
CASE 567RL

MARKING DIAGRAM

QE&K
&.&2&Z

QE = Specific Device Code
&K = 2−Digits Lot Run Traceability Code
&. = Pin One Dot
&2 = 2−Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Description

The FPF1038 advanced load−management switch target applications requiring a highly integrated solution for disconnecting loads powered from DC power rail (<6 V) with stringent shutdown current targets and high load capacitances (up to 200 μF). The FPF1038 consists of slew−rate controlled low−impedance MOSFET switch (21 mΩ typical) and other integrated analog features. The slew−rate controlled turn−on characteristic prevents inrush current and the resulting excessive voltage droop on power rails.

These devices have exceptionally low shutdown current drain (<1 μA maximum) that facilitates compliance in low standby power applications. The input voltage range operates from 1.2 V to 5.5 V DC to support a wide range of applications in consumer, optical, medical, storage, portable, and industrial device power management.

Switch control is managed by a logic input (active HIGH) capable of interfacing directly with low−voltage control signal / GPIO with no external pull−up required. The device is packaged in advanced fully “green” 1 mm x 1.5 mm Wafer−Level Chip−Scale Packaging (WLCSP); providing excellent thermal conductivity, small footprint, and low electrical resistance for wider application usage.

Features

- 1.2 V to 5.5 V Input Voltage Operating Range
- Typical R_{ON}:
  - 20 mΩ at V_{IN} = 5.5 V
  - 21 mΩ at V_{IN} = 4.5 V
  - 37 mΩ at V_{IN} = 1.8 V
  - 75 mΩ at V_{IN} = 1.2 V
- Slew Rate / Inrush Control with t_R: 2.7 ms (Typical)
- 3.5 A Maximum Continuous Current Capability
- Low <1 μA Shutdown Current
- ESD Protected: Above 8 kV HBM, 1.5 kV CDM
- GPIO / CMOS−Compatible Enable Circuitry
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- HDD, Storage, and Solid−State Memory Devices
- Portable Media Devices, UMPC, Tablets, MIDs
- Wireless LAN Cards and Modules
- SLR Digital Cameras
- Portable Medical Devices
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

APPLICATION DIAGRAM

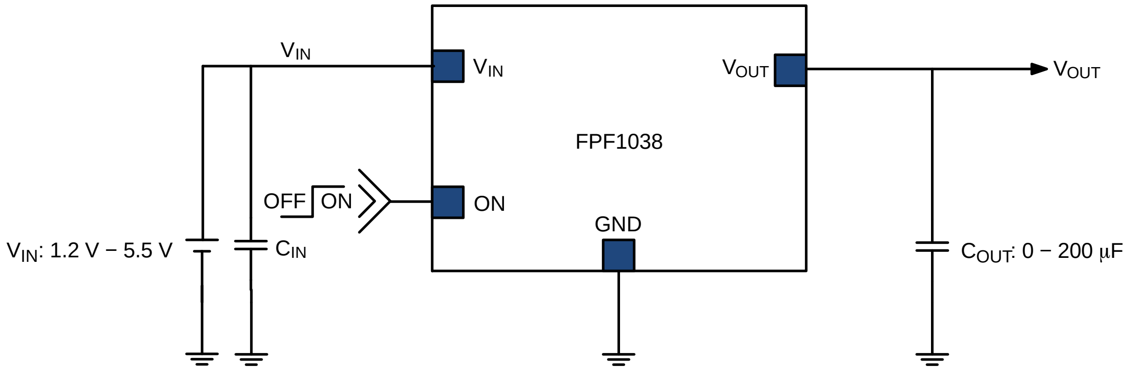


Figure 1. Typical Application

FUNCTIONAL BLOCK DIAGRAM

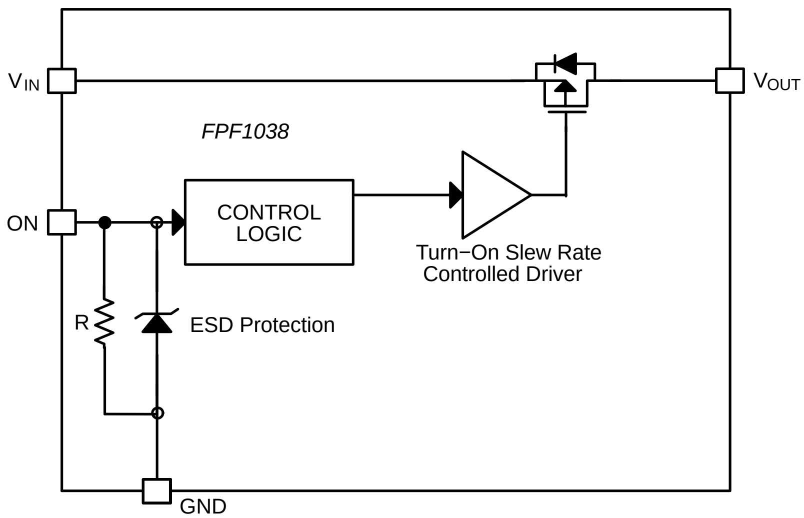


Figure 2. Functional Block Diagram

PIN CONFIGURATION

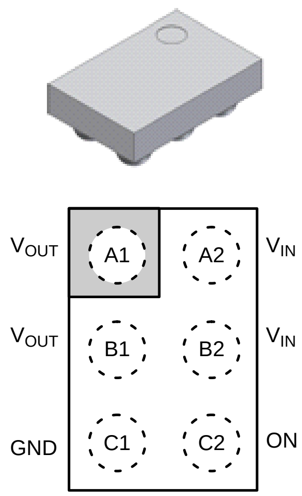


Figure 3. Top View

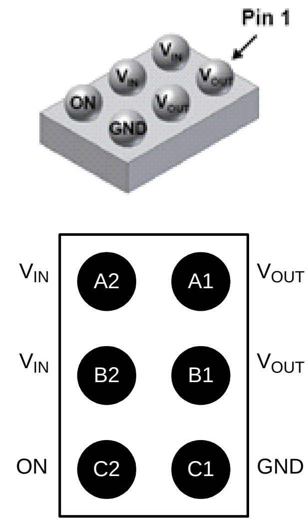


Figure 4. Bottom View

PIN DEFINITIONS

Pin No.	Name	Description
A1, B1	V_{OUT}	Switch Output
A2, B2	V_{IN}	Supply Input: Input to the Power Switch
C1	GND	Ground
C2	ON	ON/OFF Control, Active High − GPIO Compatible

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters		Min	Max	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{ON} to GND		−0.3	6.0	V
I_{SW}	Maximum Continuous Switch Current		−	3.5	A
P_D	Power Dissipation at T_A = 25°C		−	1.2	W
T_{STG}	Storage Junction Temperature		−65	+150	°C
T_A	Operating Temperature Range		−40	+85	°C
Θ_{JA}	Thermal Resistance, Junction−to−Ambient		−	85 (Note 1)	°C/W
			−	110 (Note 2)	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114	8.0	−	kV
		Charged Device Model, JESD22−C101	1.5	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured using 2S2P JEDEC std. PCB.
2. Measured using 2S2P JEDEC PCB COLD PLATE method.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameters	Min	Max	Unit
V_{IN}	Input Voltage	1.2	5.5	V
T_A	Ambient Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{IN} = 1.2 to 5.5 V and T_A = −40 to +85°C; typical values are at V_{IN} = 4.5 V and T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
BASIC OPERATION						
V_{IN}	Input Voltage		1.2	−	5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON} = GND, V_{OUT} = Open	−	−	1.0	μA
I_{SD}	Shutdown Current	V_{ON} = GND, V_{OUT} = GND	−	0.2	1.0	μA
I_Q	Quiescent Current	I_{OUT} = 0 mA	−	5.5	8.0	μA
R_{ON}	On Resistance	V_{IN} = 5.5 V, I_{OUT} = 1 A (Note 3)	−	20	24	mΩ
		V_{IN} = 4.5 V, I_{OUT} = 1 A, T_A = 25°C	−	21	25	
		V_{IN} = 3.3 V, I_{OUT} = 500 mA (Note 3)	−	24	29	
		V_{IN} = 2.5 V, I_{OUT} = 500 mA (Note 3)	−	28	35	
		V_{IN} = 1.8 V, I_{OUT} = 250 mA (Note 3)	−	37	45	
		V_{IN} = 1.2 V, I_{OUT} = 250 mA, T_A = 25°C	−	75	100	
V_{IH}	On Input Logic HIGH Voltage		1.0	−	−	V
V_{IL}	On Input Logic LOW Voltage		−	−	0.4	V
I_{ON}	On Input Leakage		−	−	1.0	μA
DYNAMIC CHARACTERISTICS						
t_{DON}	Turn−On Delay (Note 4)	V_{IN} = 4.5 V, R_L = 5 Ω, C_L = 100 μF, T_A = 25°C		1.7	−	ms
t_R	V_{OUT} Rise Time (Note 4)		−	2.7	−	ms
t_{ON}	Turn−On Time (Note 6)		−	4.4	−	ms
t_{DOFF}	Turn−Off Delay (Note 4)	V_{IN} = 4.5 V, R_L = 150 Ω, C_L = 100 μF, T_A = 25°C, No Load Discharge	−	2.0	−	ms
t_F	V_{OUT} Fall Time (Note 4)		−	30.0	−	ms
t_{OFF}	Turn−Off (Note 7)		−	32.0	−	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. This parameter is guaranteed by design and characterization; not production tested.
4. t_{DON}/t_{DOFF}/t_R/t_F are defined in Figure 27.
5. Output discharge enabled during off−state.
6. $t_{ON} = t_R + t_{DON}$
7. $t_{OFF} = t_F + t_{DOFF}$

TYPICAL CHARACTERISTICS

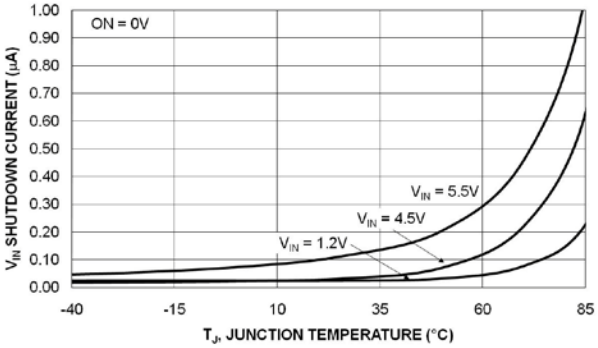


Figure 5. Shutdown Current vs. Temperature

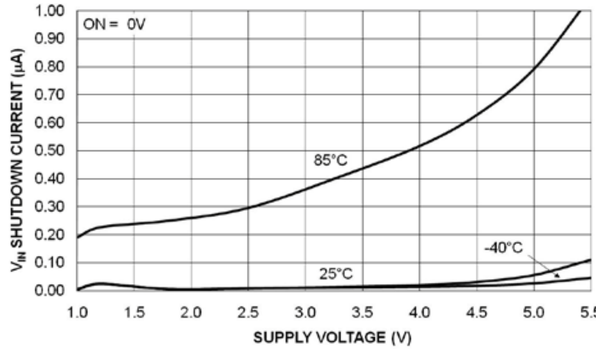


Figure 6. Shutdown Current vs. Supply Voltage

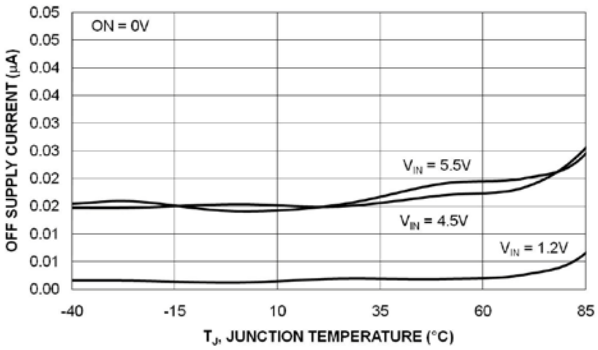


Figure 7. Off Supply Current vs. Temperature (V_{OUT} Floating)

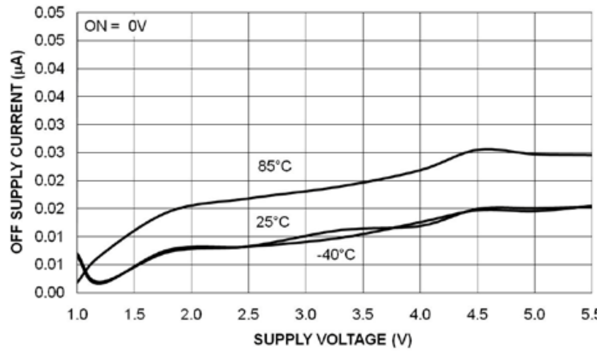


Figure 8. Off Supply Current vs. Supply Voltage (V_{OUT} Floating)

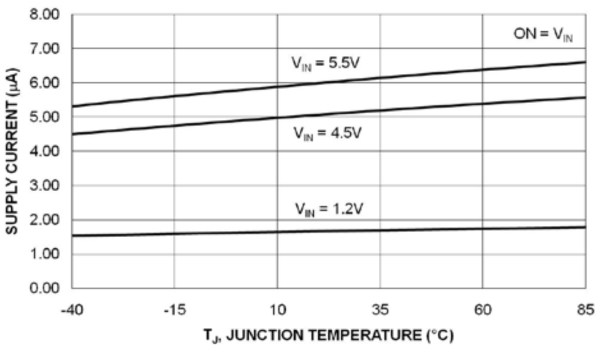


Figure 9. Quiescent Current vs. Temperature

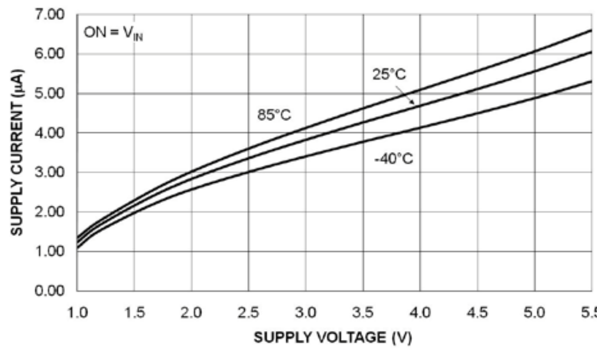


Figure 10. Quiescent Current vs. Supply Voltage

TYPICAL CHARACTERISTICS (continued)

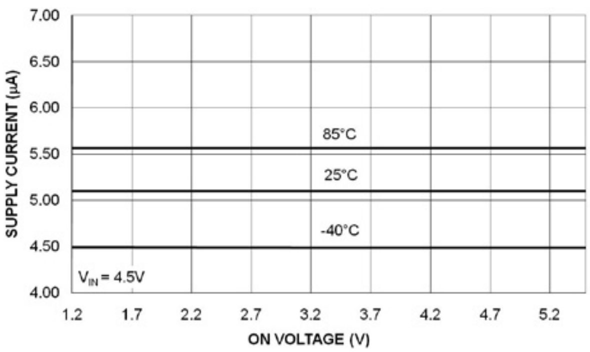


Figure 11. Quiescent Current vs. On Voltage (V_{IN} = 4.5 V)

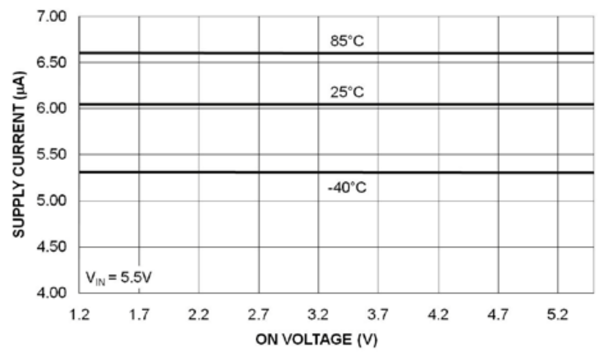


Figure 12. Quiescent Current vs. On Voltage (V_{IN} = 5.5 V)

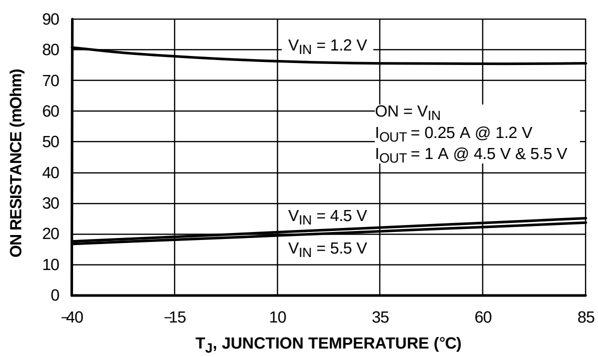


Figure 13. R_{ON} vs. Temperature

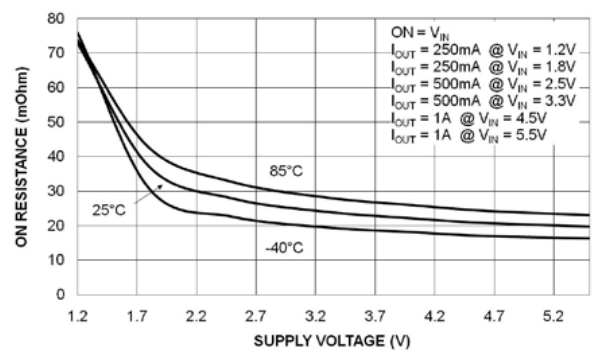


Figure 14. R_{ON} vs. Supply Voltage

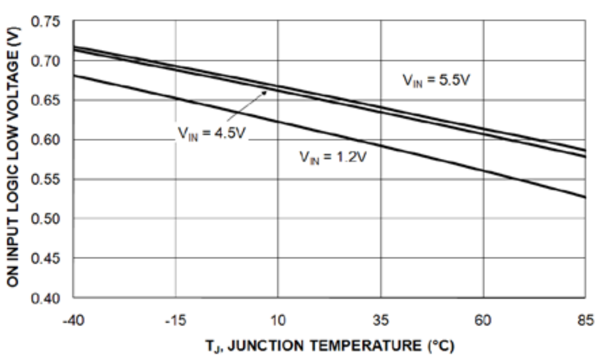


Figure 15. On Pin Threshold Low vs. Temperature

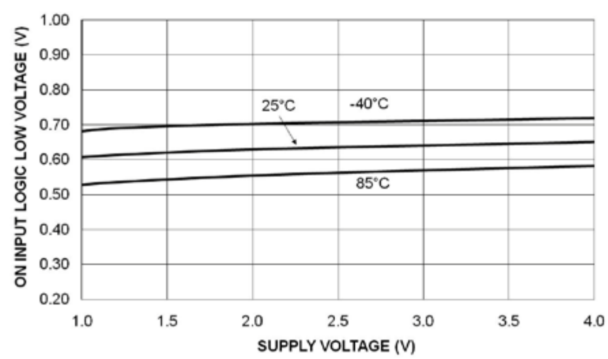


Figure 16. On Pin Threshold Low vs. V_{IN}

TYPICAL CHARACTERISTICS (continued)

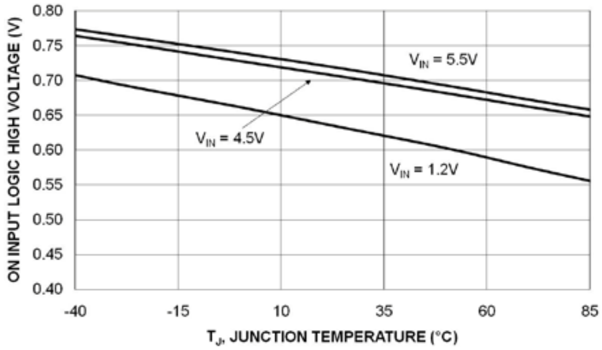


Figure 17. On Pin Threshold High vs. Temperature

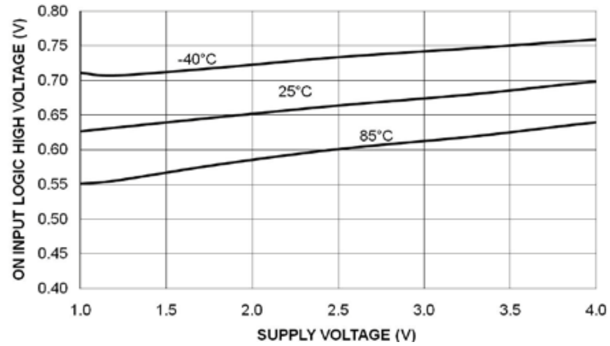


Figure 18. On Pin Threshold High vs. V_{IN}

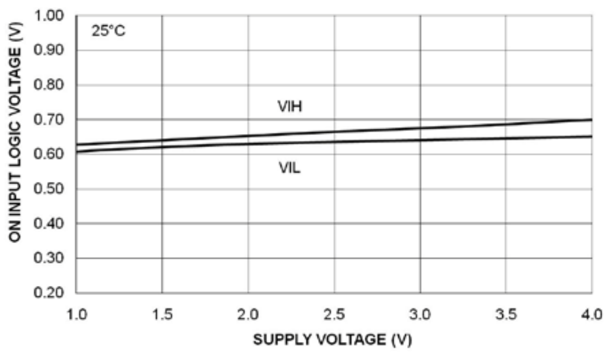


Figure 19. On Pin Threshold vs. Supply Voltage

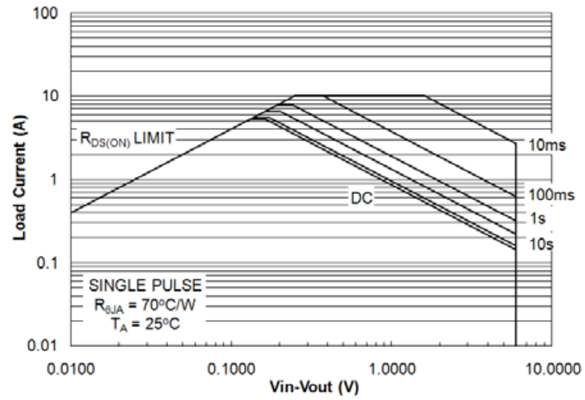


Figure 20. I_{SW} vs. (V_{IN}−V_{OUT}) — SOA

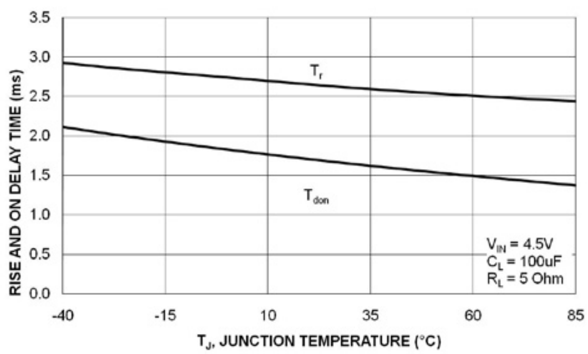


Figure 21. t_R/t_{DON} vs. Temperature

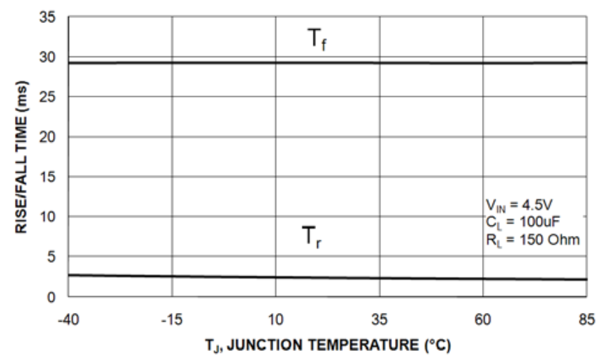


Figure 22. t_R/t_F vs. Temperature

TYPICAL CHARACTERISTICS (continued)

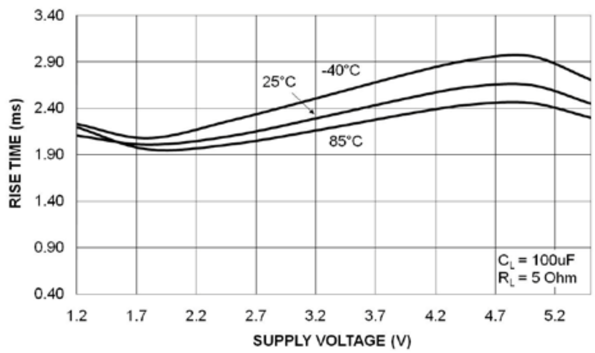


Figure 23. t_R vs. Supply Voltage

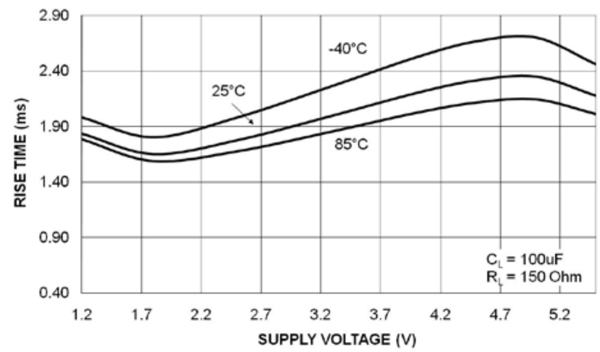


Figure 24. t_R vs. Supply Voltage

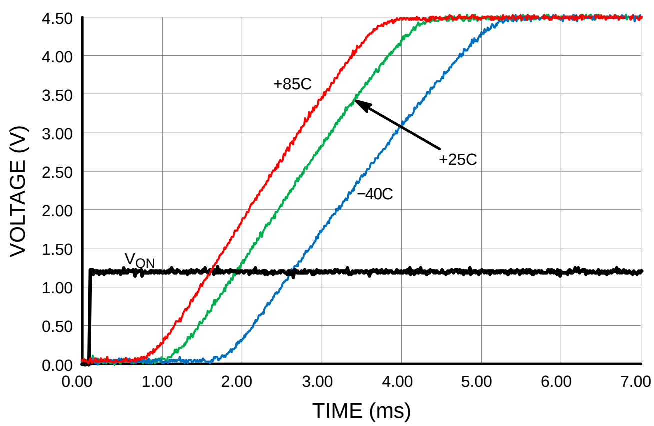


Figure 25. Turn−On Response (V_{IN} = 4.5 V, C_{IN} = 10 μF, C_L = 1 μF, R_L = 50 Ω)

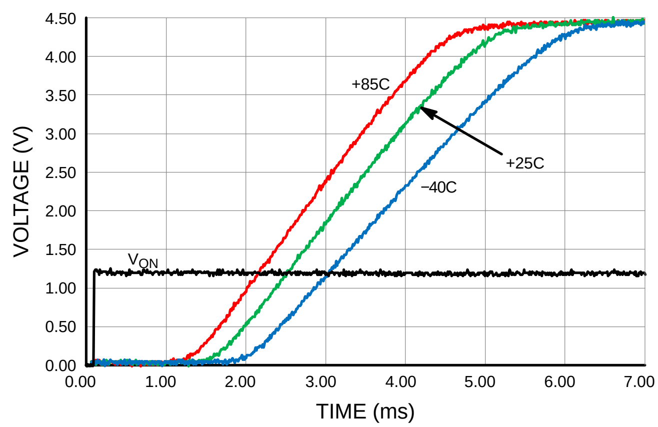


Figure 26. Turn−On Response (V_{IN} = 4.5 V, C_{IN} = 10 μF, C_L = 100 μF, R_L = 5 Ω)

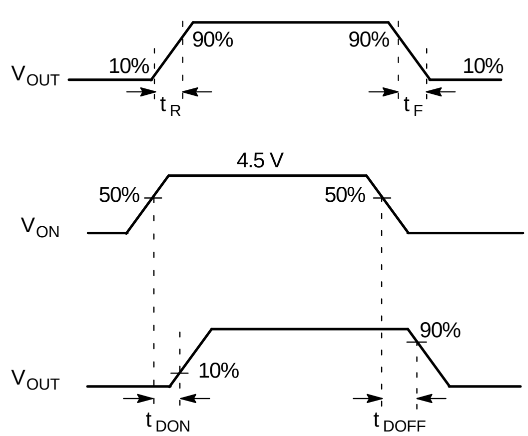


Figure 27. Timing Diagram

APPLICATION INFORMATION

Input Capacitor

This IntelliMAX™ switch doesn't require an input capacitor. To reduce device inrush current, a 0.1 μF ceramic capacitor, C_{IN}, is recommended close to the VIN pin. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

While this switch works without an output capacitor: if parasitic board inductance forces V_{OUT} below GND when switching off; a 0.1 μF capacitor, C_{OUT}, should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on RC constant of the external components as follows:

$$t_F = R_L \times C_L \times 2.2 \quad \text{(eq. 1)}$$

where t_F is 90% to 10% fall time, R_L is output load, and C_L is output capacitor.

The same equation works for a device with a pull−down output resistor. R_L is replaced by a parallel connected pull−down and an external output resistor combination as:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \quad \text{(eq. 2)}$$

where t_F is 90% to 10% fall time, R_L is output load, $R_{PD} = 65\ \Omega$ is output pull−down resistor, and C_L is the output capacitor.

Resistive Output Load

If resistive output load is missing, the IntelliMAX switch without a pull−down output resistor does not discharge the output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

Application Specifics

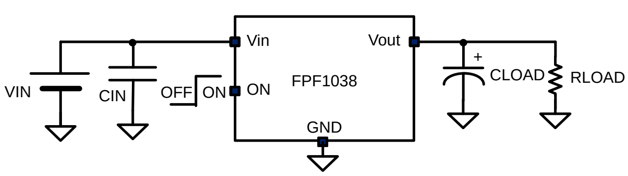


Figure 28. Device Setup

At maximum operational voltage (V_{IN} = 5.5 V), device inrush current might be higher than expected. Spike current should be taken into account if V_{IN} > 5 V and the output capacitor is much larger than the input capacitor. Input current can be calculated as:

$$I_{IN}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + \left(C_{LOAD} - C_{IN}\right)\frac{dV_{OUT}(t)}{dt} \quad \text{(eq. 3)}$$

where switch and wire resistances are neglected and capacitors are assumed ideal.

Estimating $V_{OUT}(t) = V_{IN} / 10$ and using experimental formula for slew rate ($dV_{OUT}(t) / dt$), spike current can be written as:

$$\max\left(I_{IN}\right) = \frac{V_{IN}}{10R_{LOAD}} + \left(C_{LOAD} - C_{IN}\right)\left(0.05V_{IN} - 0.255\right) \quad \text{(eq. 4)}$$

where supply voltage V_{IN} is in volts, capacitances are in micro farads, and resistance is in ohms.

Example: If V_{IN} = 5.5 V, C_{LOAD} = 100 μF, C_{IN} =10 μF, andR_{LOAD} = 50 Ω; calculate the spike current by:

$$\max\left(I_{IN}\right) = \frac{5.5}{10 \times 50} + (100 - 10)(0.05 \times 5.5 - 0.255)\ \text{A} = $$
$$= 1.8\ \text{A} \quad \text{(eq. 5)}$$

Maximum spike current is 1.8 A, while average ramp−up current is:

$$I_{IN}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + \left(C_{LOAD} - C_{IN}\right)\frac{dV_{IN}(t)}{dt}$$
$$\approx 2.75 / 50 + 100 \times 0.0022 = 0.275\ \text{A} \quad \text{(eq. 6)}$$

Recommended Layout

For best thermal performance and minimal inductance and parasitic effects, it is recommended to keep input and output traces short and capacitors as close to the device as possible. Figure 29 is a recommended layout for this device to achieve optimum performance.

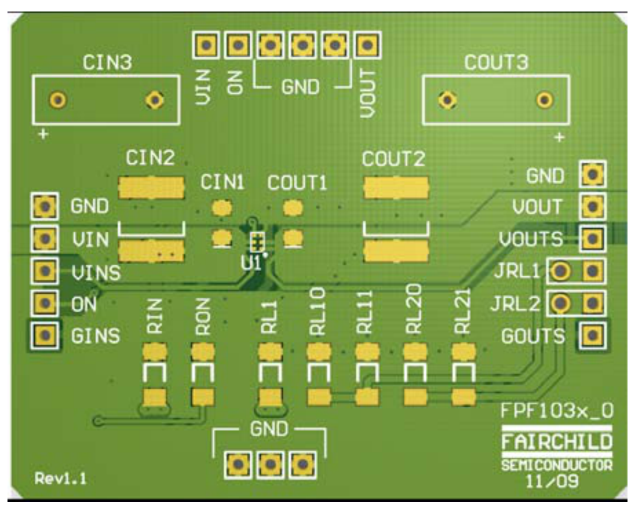


Figure 29. Recommended Land Pattern, Layout

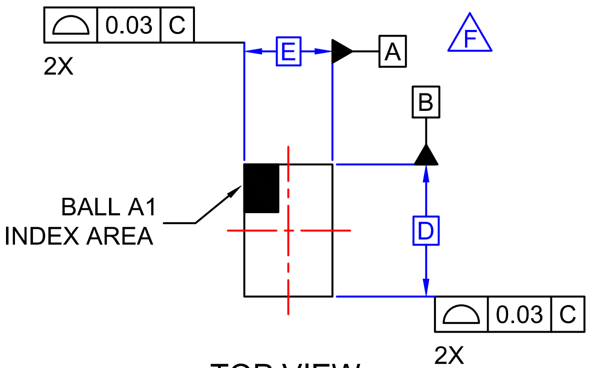
ORDERING INFORMATION

Part Number	Top Mark	Switch R_{ON} (Typical) at 4.5 V_{IN}	Input Buffer	Output Discharge	ON Pin Activity	t_R	Package	Shipping†
FPF1038UCX	QE	21 mΩ	CMOS	NA	Active HIGH	2.7 ms	6−Bump, WLCSP, 1.0 mm x 1.5 mm, 0.5 mm Pitch (Pb−Free)	3000 / Tape & Reel

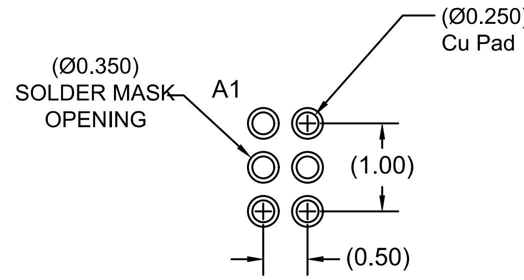
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WLCSP6 1.5x1.0x0.582
CASE 567RL
ISSUE O

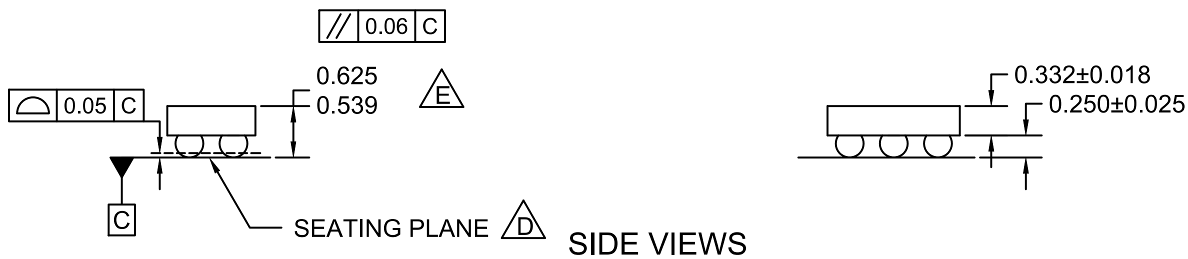
DATE 30 NOV 2016



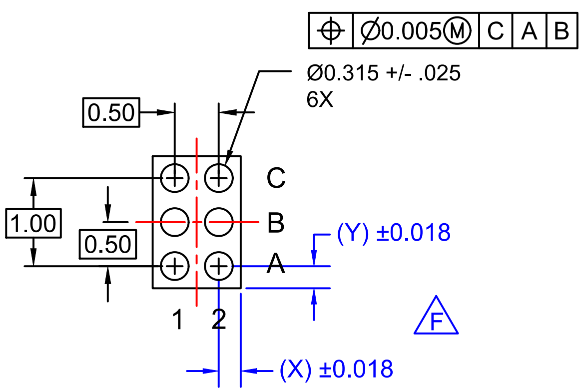
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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DESCRIPTION:	**WLCSP6 1.5x1.0x0.582**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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