

MOSFET – N-Channel, QFET

150 V, 70 A, 28 mΩ

FQA70N15

Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 70 A, 100 V, $R_{DS(on)} = 28 \text{ m}\Omega$ (Max) @ $V_{GS} = 10 \text{ V}$, $I_D = 35 \text{ A}$
- Low Gate Charge (Typ. 135 nC)
- Low C_{rss} (Typ. 135 pF)
- 100% Avalanche Tested
- This is a Pb-Free Device

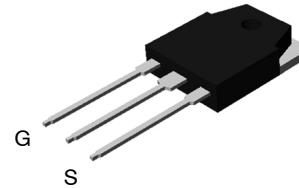
ABSOLUTE MAXIMUM RATINGS

($T_C = 25^\circ\text{C}$ unless otherwise noted)

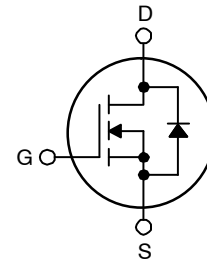
Symbol	Parameter	FQA70N15	Unit
V_{DSS}	Drain to Source Voltage	150	V
I_D	Drain Current Continuous ($T_C = 25^\circ\text{C}$) Continuous ($T_C = 100^\circ\text{C}$)	70 50	A
I_{DM}	Drain Current – Pulsed (Note 1)	250	A
V_{GSS}	Gate to Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1000	mJ
I_{AR}	Avalanche Current (Note 1)	70	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	33	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) – Derate above 25°C	330 2.2	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+175$	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 0.34 \text{ mH}$, $I_{AS} = 70 \text{ A}$, $V_{DD} = 25 \text{ V}$, $R_G = 25 \text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 70 \text{ A}$, $di/dt \leq 300 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.



TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ



MARKING DIAGRAM

&Z&3&K
FQA
70N15

&Z = Assembly Location
&3 = Date Code (Year and Week)
&K = Lot Code
FQA70N15 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FQA70N15	TO-3P (Pb-Free)	450 / Tube

FQA70N15

THERMAL CHARACTERISTICS

Symbol	Parameter	FQA70N15	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max	40	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTIC						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	150	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	0.15	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 150\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$V_{DS} = 120\ \text{V}$, $T_C = 150^\circ\text{C}$	–	–	10	
I_{GSSF}	Gate to Body Leakage Current, Forward	$V_{GS} = 25\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	100	nA
I_{GSSR}	Gate to Body Leakage Current, Reverse	$V_{GS} = -25\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	-100	

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 35\ \text{A}$	–	0.023	0.028	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\ \text{V}$, $I_D = 35\ \text{A}$	–	48	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1.0\ \text{MHz}$	–	4150	5400	pF
C_{oss}	Output Capacitance		–	840	1100	pF
C_{rss}	Reverse Transfer Capacitance		–	135	175	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}$, $I_D = 70\ \text{A}$, $R_G = 25\ \Omega$ (Note 4)	–	60	130	ns
t_r	Turn-On Rise Time		–	420	850	ns
$t_{d(off)}$	Turn-Off Delay Time		–	340	690	ns
t_f	Turn-Off Fall Time		–	290	590	ns
Q_g	Total Gate Charge	$V_{DS} = 120\ \text{V}$, $I_D = 70\ \text{A}$, $V_{GS} = 10\ \text{V}$ (Note 4)	–	135	175	nC
Q_{gs}	Gate to Source Charge		–	25	–	nC
Q_{gd}	Gate to Drain Charge		–	65	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	70	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	280	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 70 A	–	–	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 70 A, dI _F /dt = 100 A/μs	–	150	–	ns
Q _{rr}	Reverse Recovery Charge		–	0.67	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

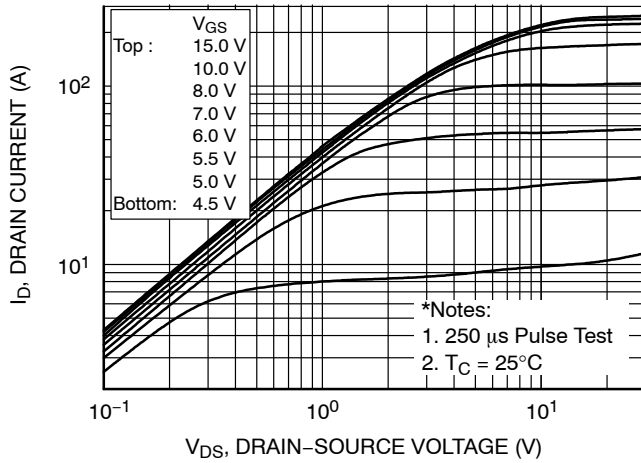


Figure 1. On-Region Characteristics

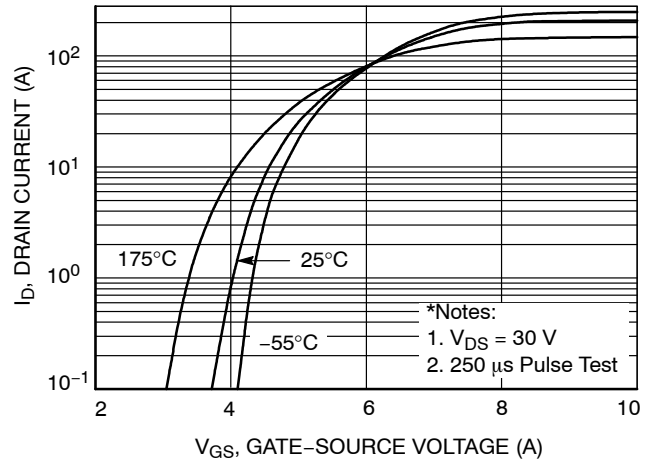


Figure 2. Transfer Characteristics

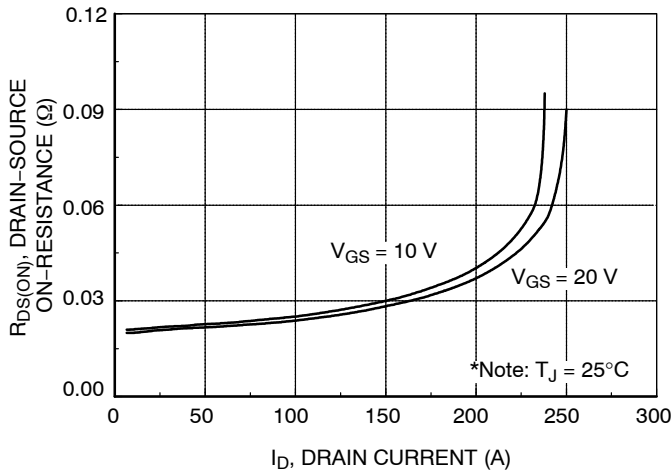


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

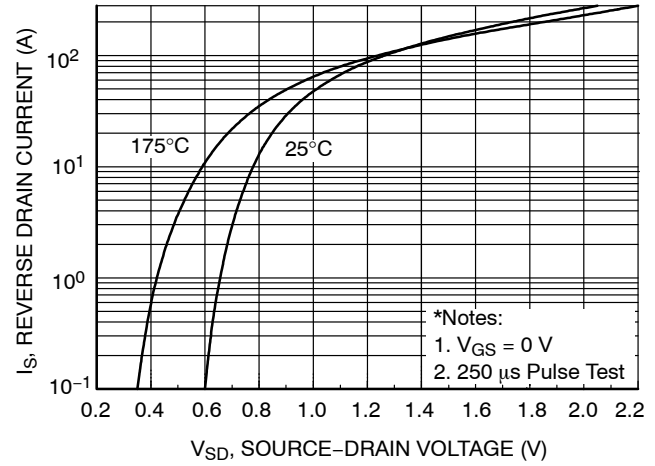


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

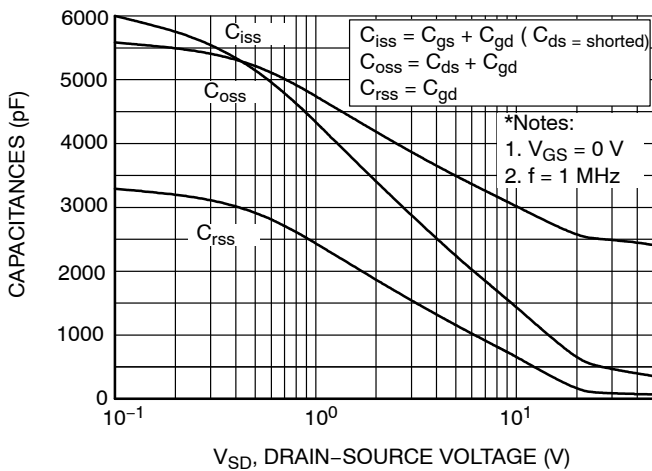


Figure 5. Capacitance Characteristics

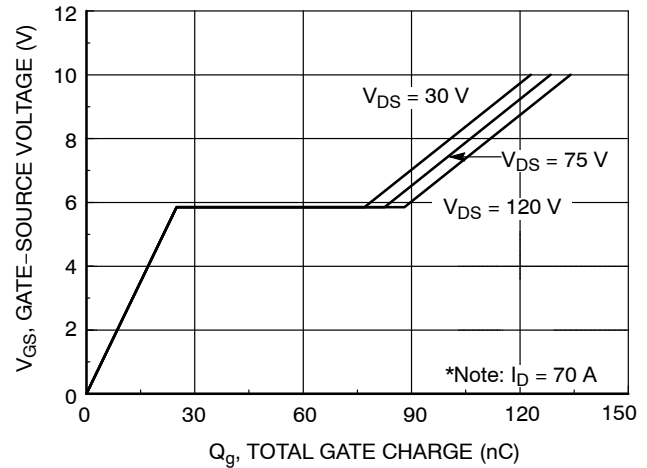


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

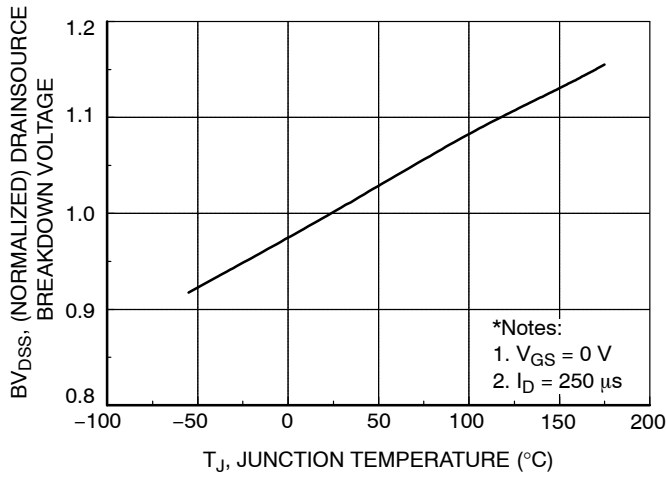


Figure 7. Breakdown Voltage Variation vs. Temperature

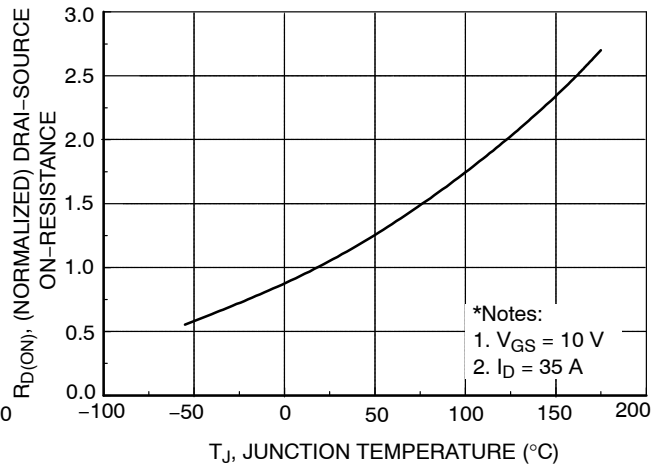


Figure 8. On-Resistance Variation vs. Temperature

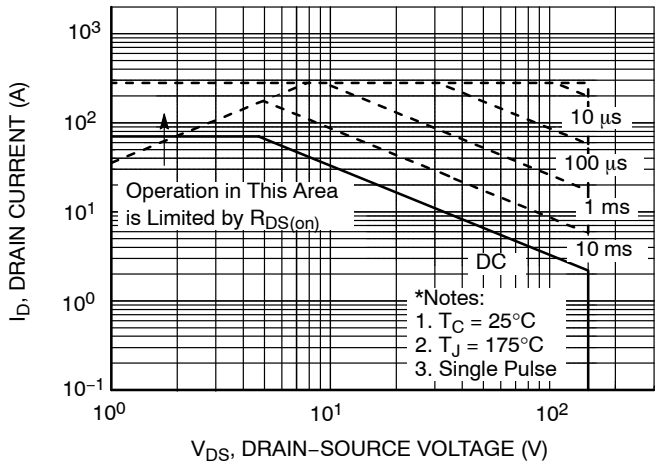


Figure 9. Maximum Safe Operating Area

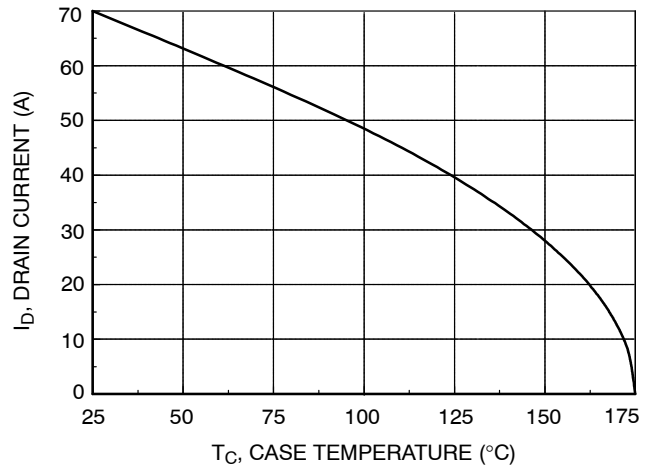


Figure 10. Maximum Drain Current vs. Case Temperature

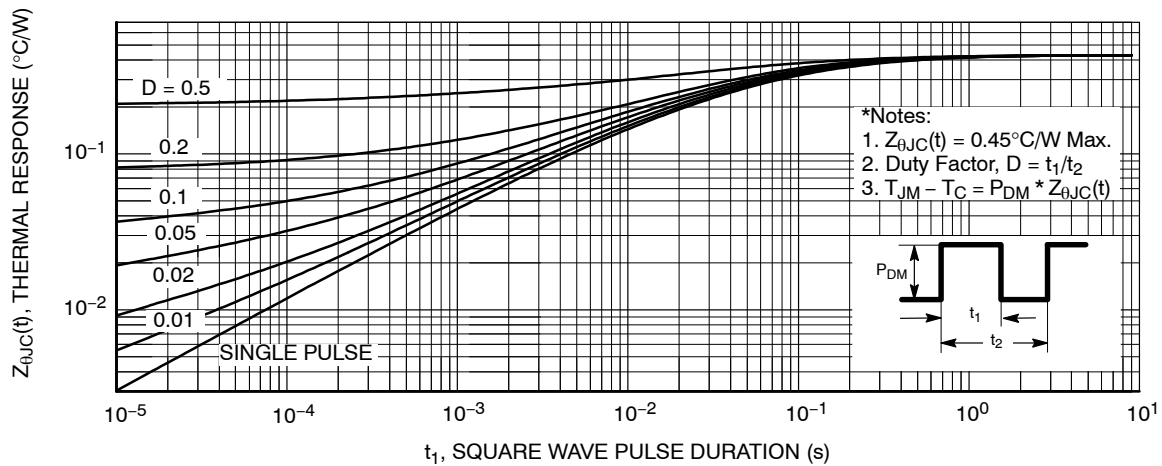


Figure 11. Transient Thermal Response Curve

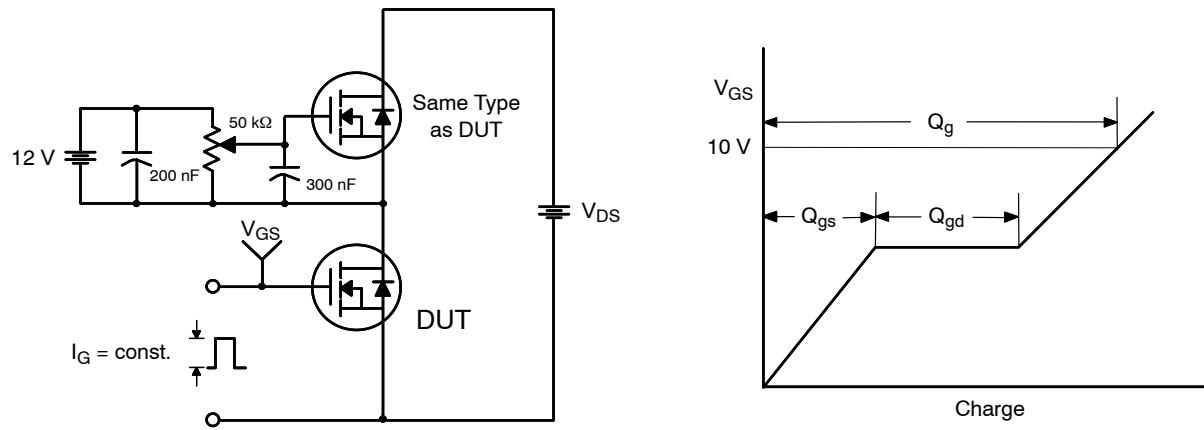


Figure 12. Gate Charge Test Circuit & Waveform

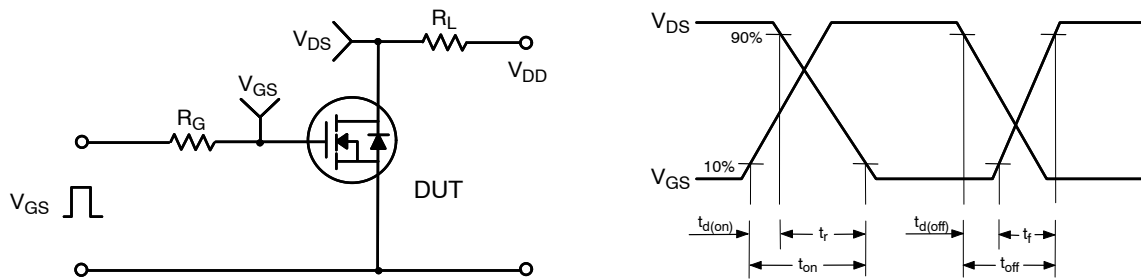


Figure 13. Resistive Switching Test Circuit & Waveforms

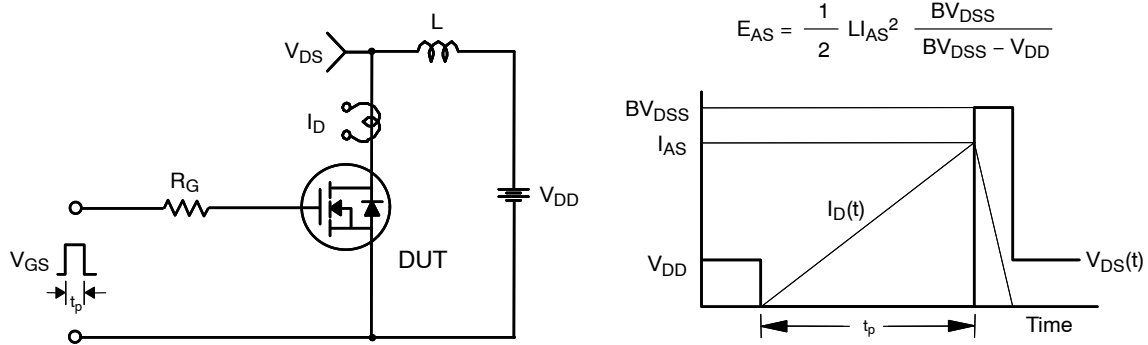


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FQA70N15

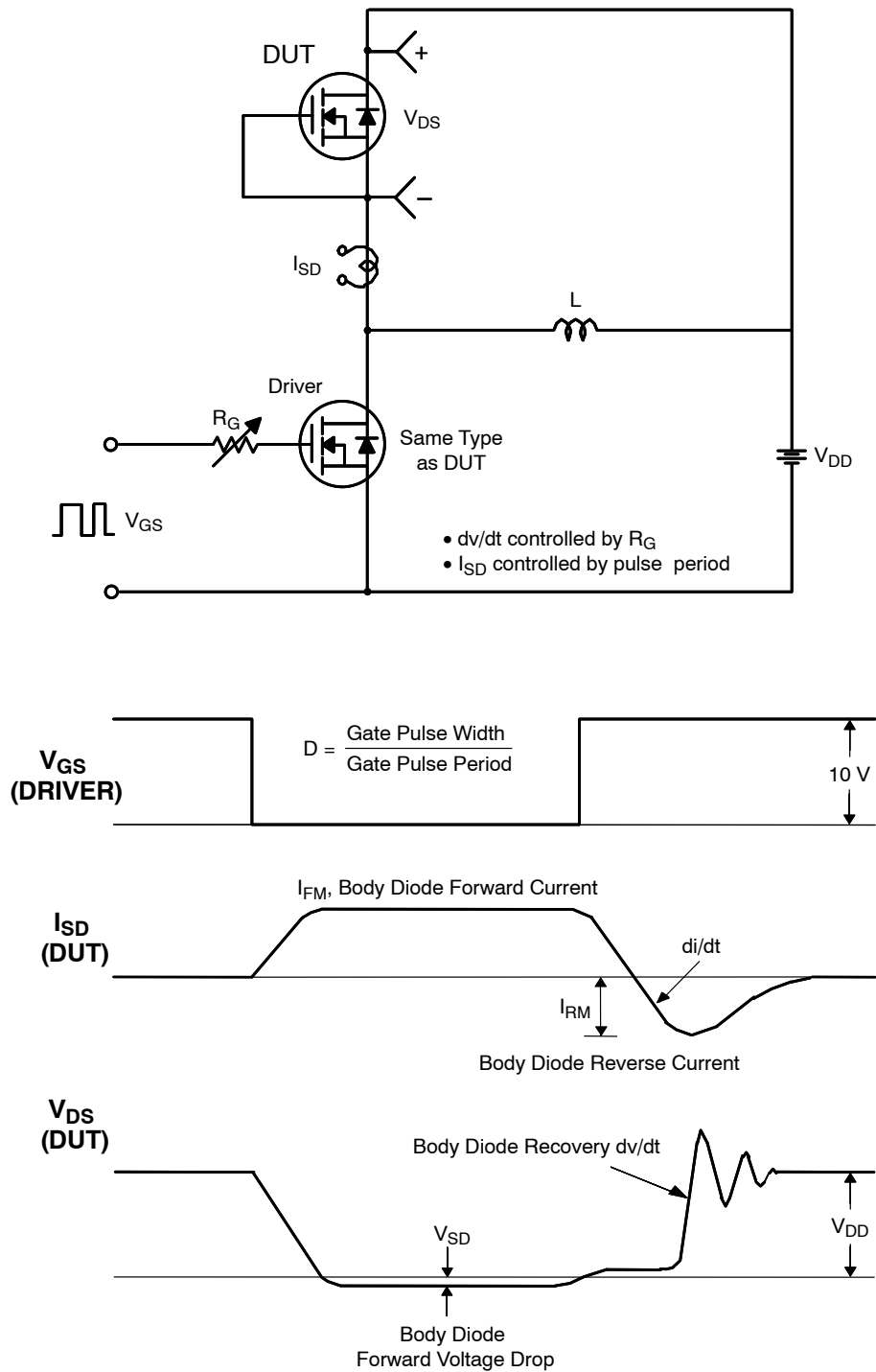
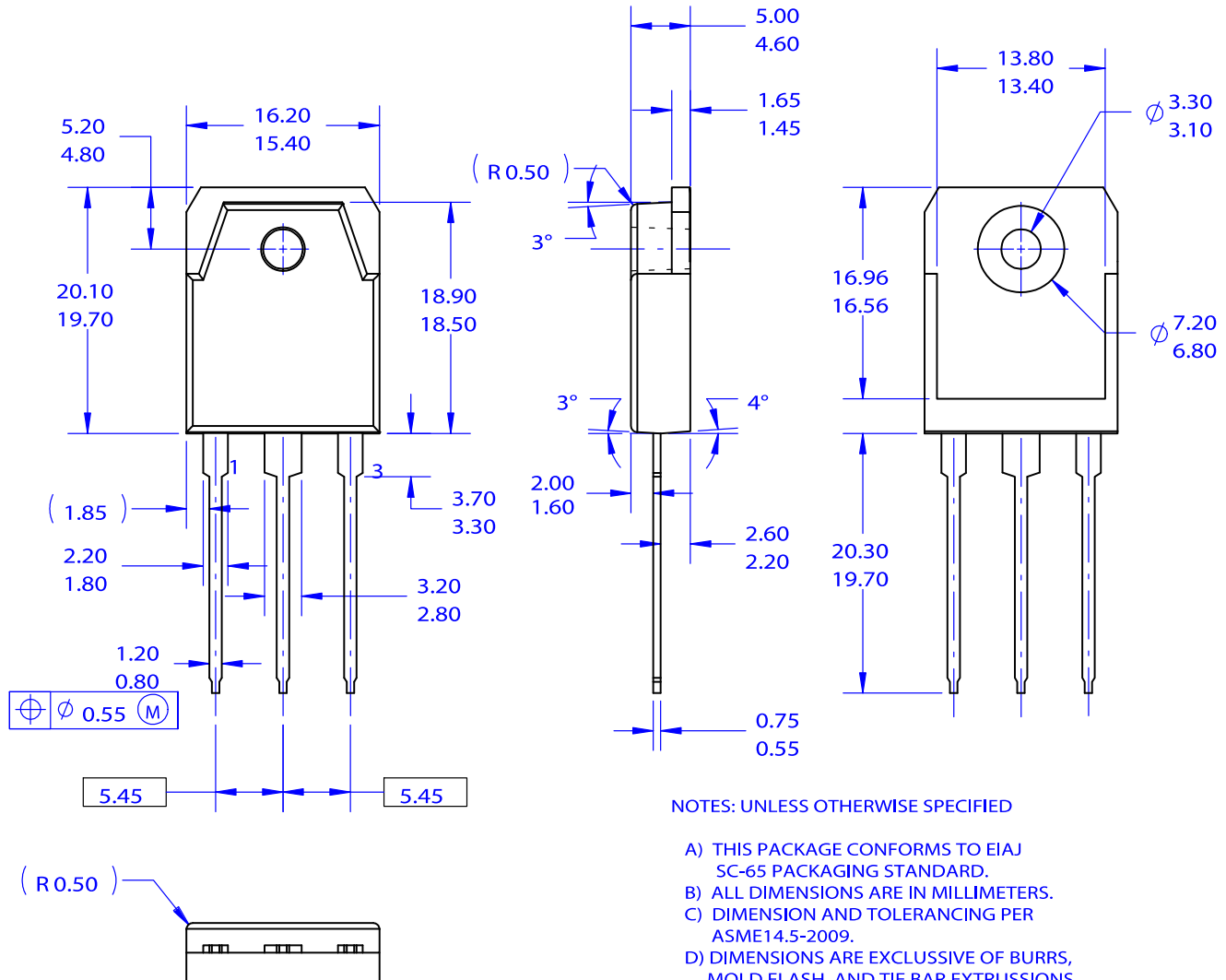


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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CASE 340BZ
ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

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