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# FQB50N06L

## N-Channel QFET® MOSFET

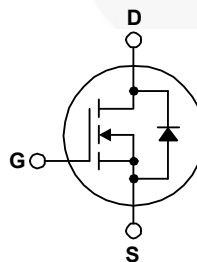
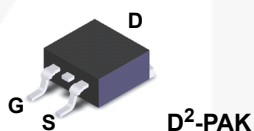
60 V, 52.4 A, 21 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 52.4 A, 60 V,  $R_{DS(on)} = 21 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 26.2 \text{ A}$
- Low Gate Charge (Typ. 24.5 nC)
- Low Crss (Typ. 90 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQB50N06LTM	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	52.4	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	37.1	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	210	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	990	mJ
$I_{AR}$	Avalanche Current (Note 1)	52.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	12.1	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.75	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	121	W
	- Derate above $25^\circ\text{C}$	0.81	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQB50N06LTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB50N06LTM	FQB50N06L	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.06	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 48\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 26.2\text{ A}$	--	0.017	0.021	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 26.2\text{ A}$	--	0.020	0.025	
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 26.2\text{ A}$	--	40	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1250	1630	pF
$C_{oss}$	Output Capacitance		--	445	580	pF
$C_{rss}$	Reverse Transfer Capacitance		--	90	120	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 26.2\text{ A},$ $R_G = 25\ \Omega$	--	20	50	ns
$t_r$	Turn-On Rise Time		--	380	770	ns
$t_{d(off)}$	Turn-Off Delay Time		--	80	170	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	145	300
$Q_g$	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 52.4\text{ A},$ $V_{GS} = 5\text{ V}$	--	24.5	32	nC
$Q_{gs}$	Gate-Source Charge		--	6	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	14.5	--

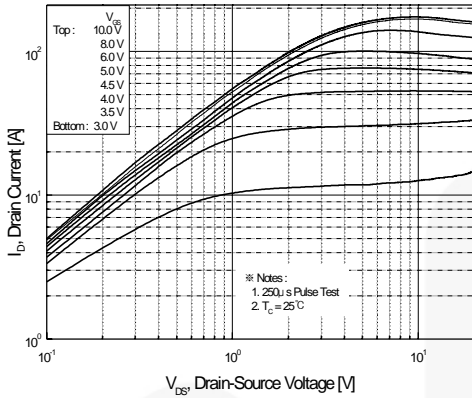
### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	52.4	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	210	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 52.4\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 52.4\text{ A},$	--	65	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	125	--	nC

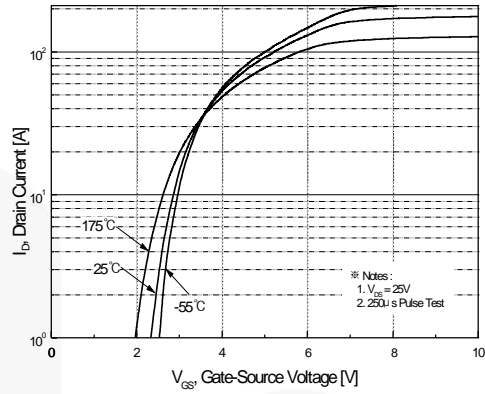
#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 300\ \mu\text{H}, I_{AS} = 52.4\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 52.4\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature.

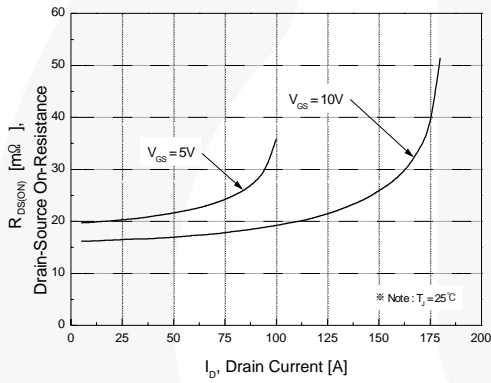
## Typical Characteristics



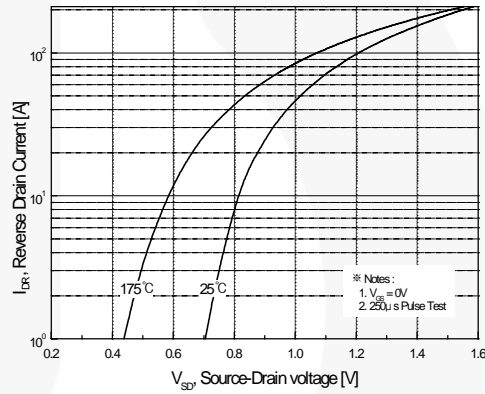
**Figure 1. On-Region Characteristics**



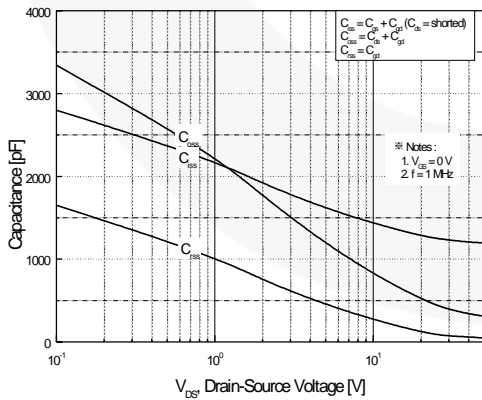
**Figure 2. Transfer Characteristics**



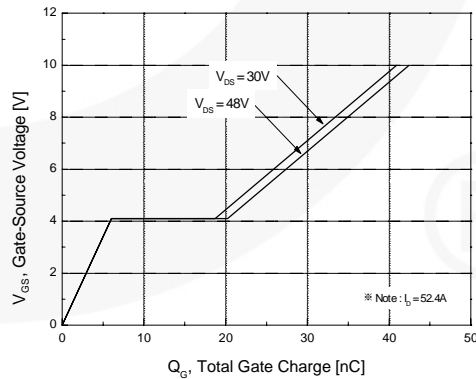
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

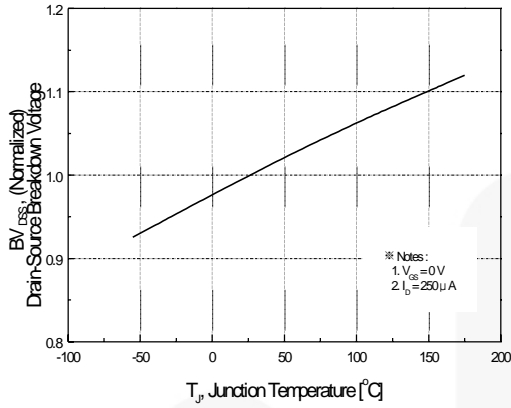


**Figure 5. Capacitance Characteristics**

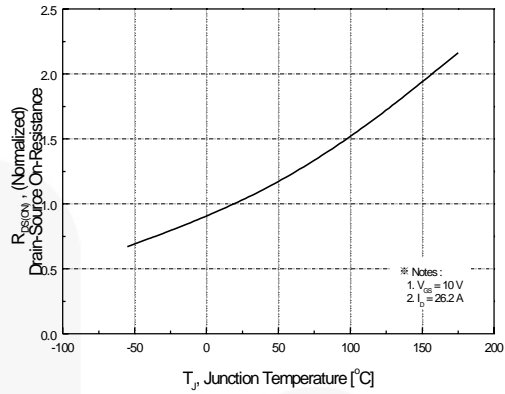


**Figure 6. Gate Charge Characteristics**

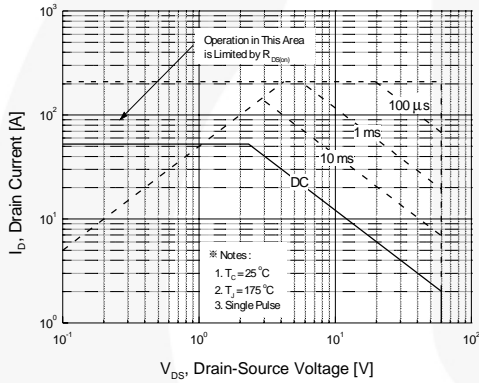
**Typical Characteristics** (Continued)



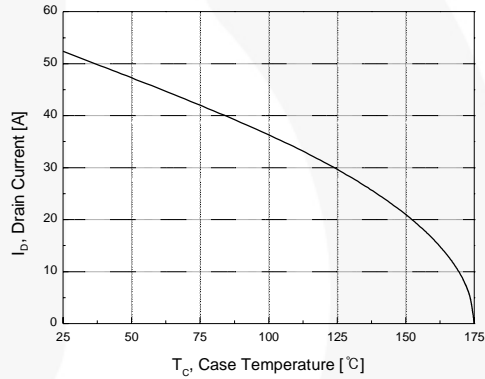
**Figure 7. Breakdown Voltage Variation vs. Temperature**



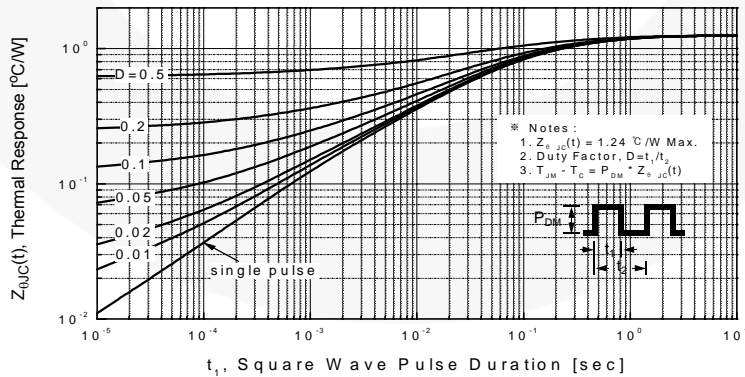
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

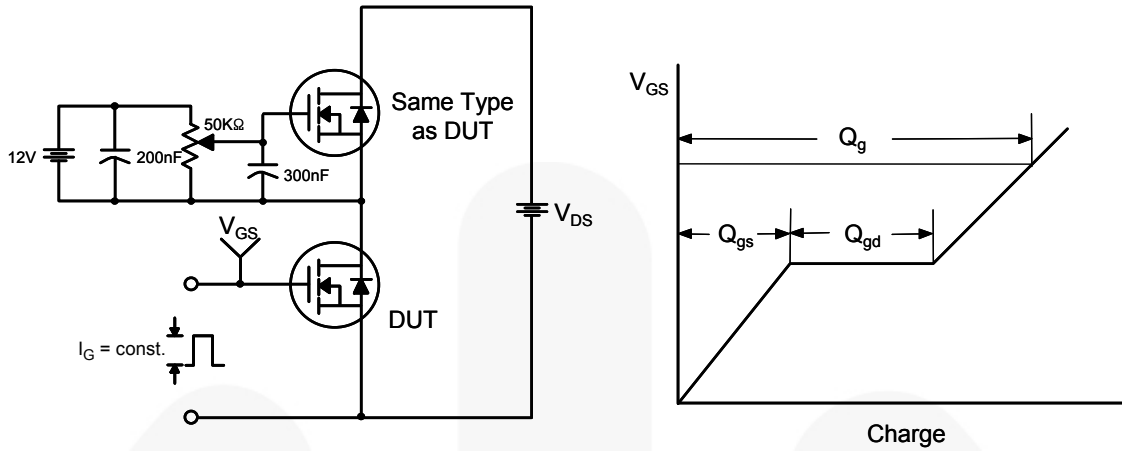


Figure 12. Gate Charge Test Circuit & Waveform

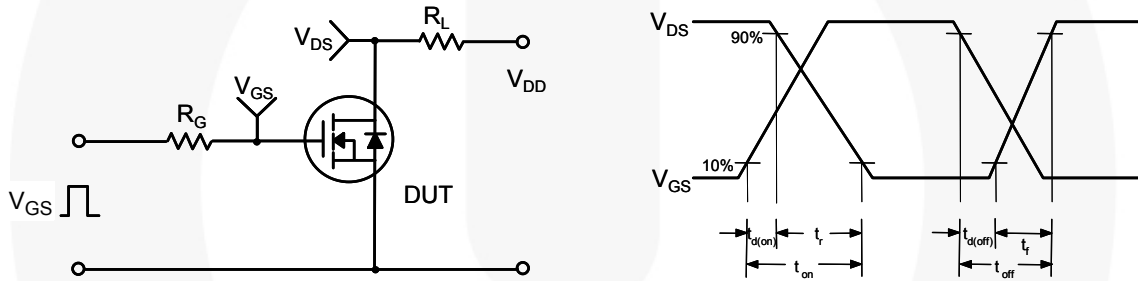


Figure 13. Resistive Switching Test Circuit & Waveforms

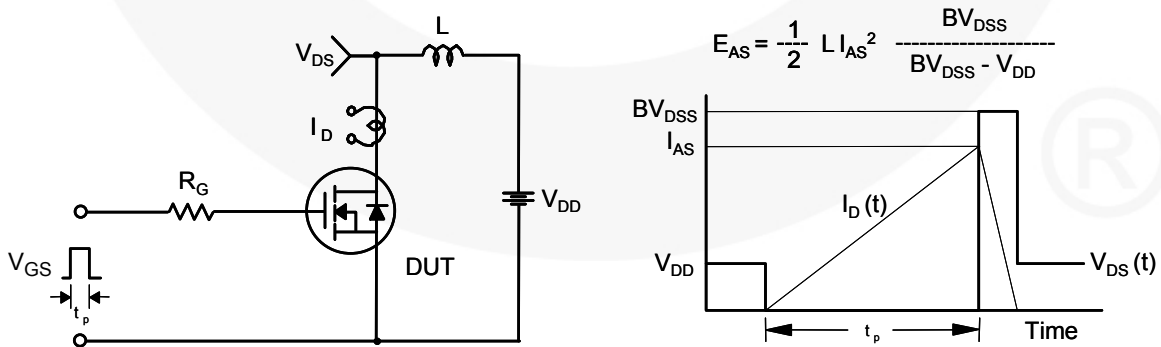
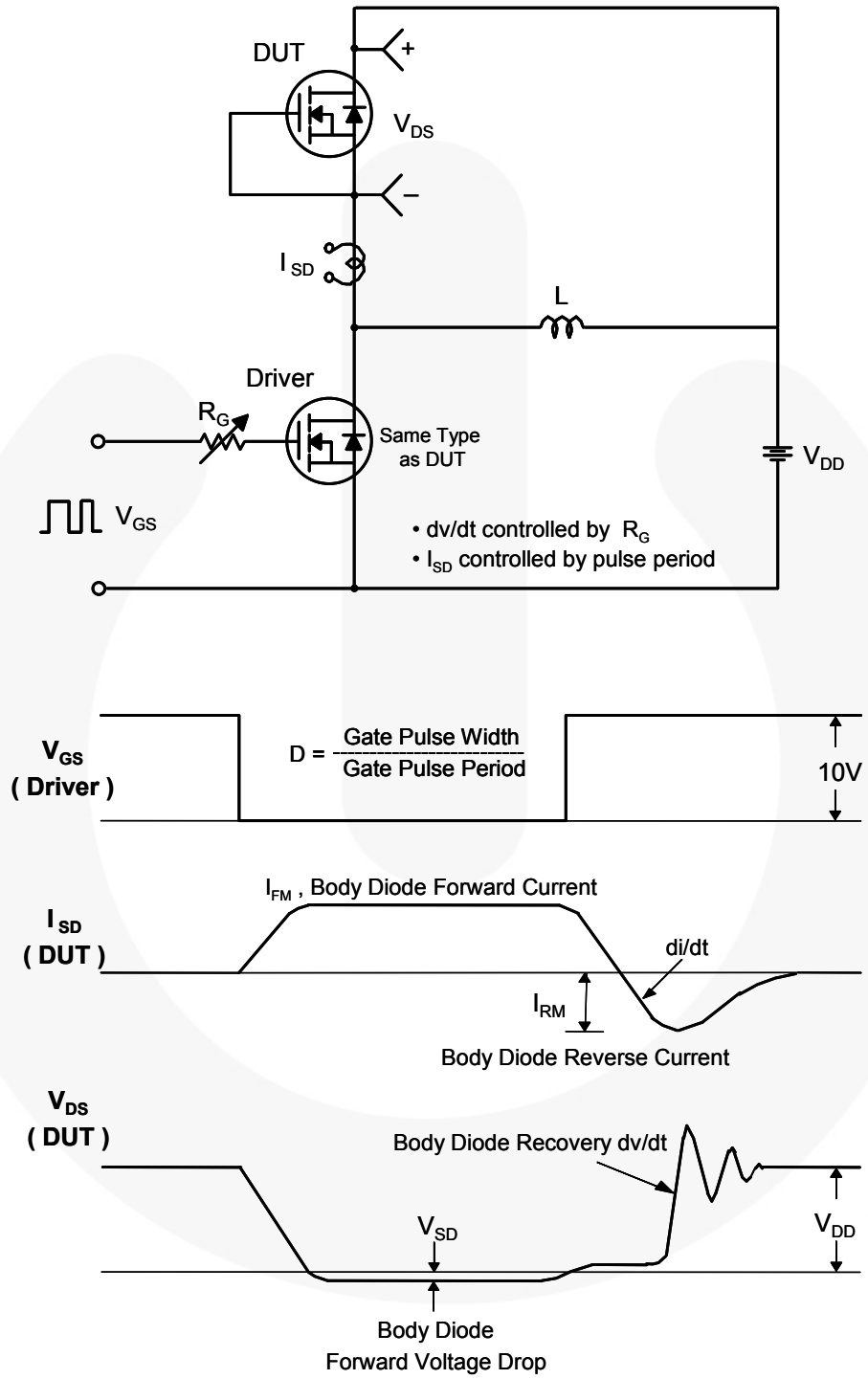
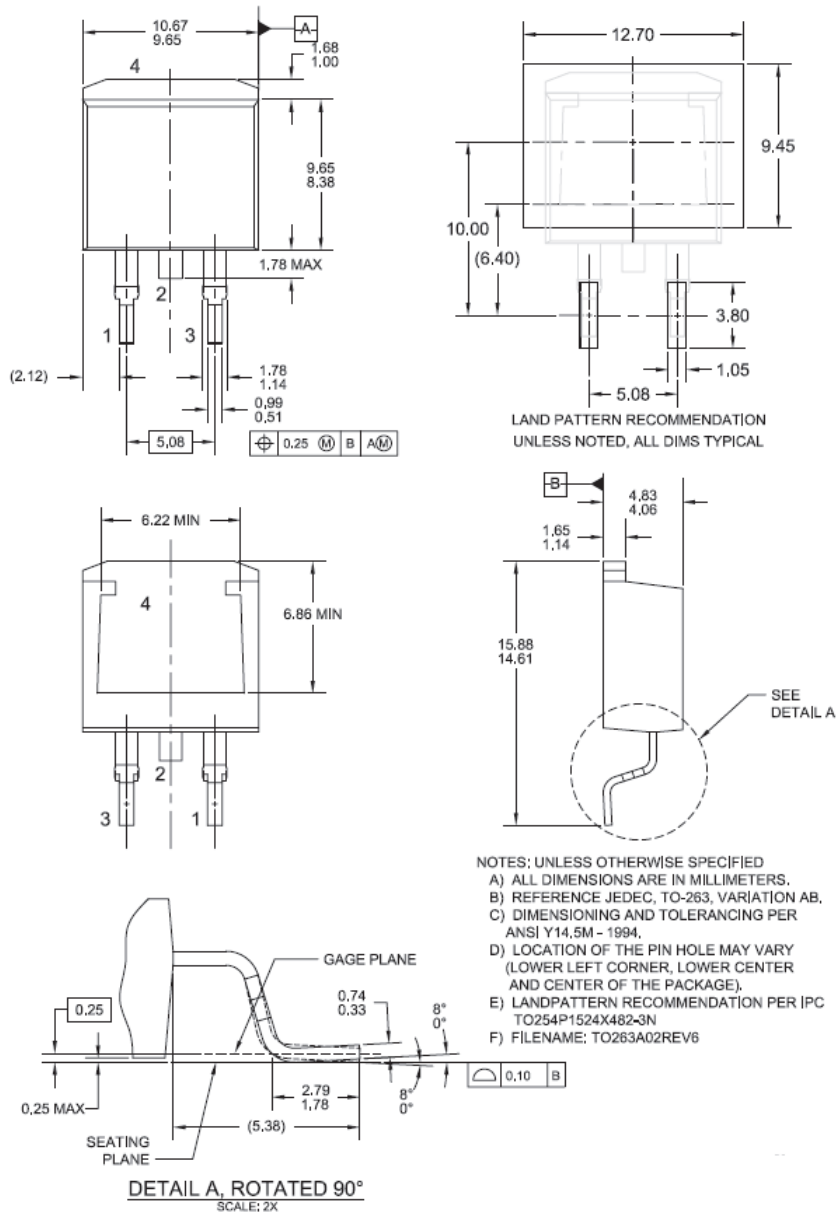


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

**Mechanical Dimensions**



**Figure 16. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount**

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