

# MOSFET – N-Channel, QFET

800 V, 1.5 A, 6.3 mΩ

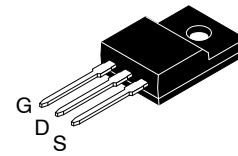
## FQPF2N80

### Description

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

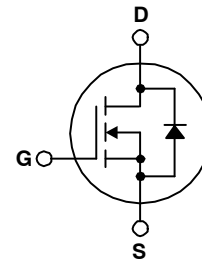
### Features

- 1.5 A, 800 V,  $R_{DS(on)} = 6.3 \Omega$  (Max.) @  $V_{GS} = 10$  V,  $I_D = 0.75$  A
- Low Gate Charge (Typ. 12 nC)
- Low  $C_{rss}$  (Typ. 5.5 pF)
- 100% Avalanche Tested

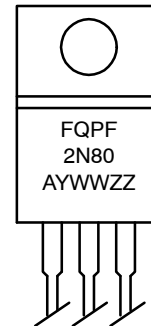


TO-220 Fullpack,  
 3-Lead /  
 TO-220F-3SG  
 CASE 221AT

### N-CHANNEL MOSFET



### MARKING DIAGRAM



FQPF2N80 = Specific Device Code  
 A = Assembly Location  
 YWW = Date Code (Year & Week)  
 ZZ = Assembly Lot

### ORDERING INFORMATION

Device	Package	Shipping
FQPF2N80	TO-220 Fullpack	1,000 Units / Tube

# FQPF2N80

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V <sub>DSS</sub>	Drain–Source Voltage	800	V
I <sub>D</sub>	Drain Current	– Continuous (T <sub>C</sub> = 25°C) – Continuous (T <sub>C</sub> = 100°C)	1.5 A 0.95 A
I <sub>DM</sub>	Drain Current	– Pulsed (Note 1)	6.0 A
V <sub>GSS</sub>	Gate–Source Voltage	±30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	180	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	1.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C) – Derate Above 25°C	35 W 0.28 W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	–55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction–to–Case, Max.	3.57	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction–to–Ambient, Max.	62.5	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	800	–	–	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	0.9	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 640 V, T <sub>C</sub> = 125°C	–	–	10 100	μA μA
I <sub>GSSF</sub>	Gate–Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	–	–	100	nA
I <sub>GSSR</sub>	Gate–Body Leakage Current, Reverse	V <sub>GS</sub> = –30 V, V <sub>DS</sub> = 0V	–	–	–100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	–	5.0	V
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.75 A	–	4.6	6.3	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 0.75 A	–	2.2	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	–	425	550	pF
C <sub>oss</sub>	Output Capacitance		–	45	60	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	5.5	7.0	pF

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## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)(continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}$ , $I_D = 2.4\text{ A}$ , $R_G = 25\ \Omega$ (Note 4)	–	12	35	ns
$t_r$	Turn-On Rise Time		–	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		–	25	60	ns
$t_f$	Turn-Off Fall Time		–	28	65	ns
$Q_g$	Total Gate Charge	$V_{DS} = 640\text{ V}$ , $I_D = 2.4\text{ A}$ , $V_{GS} = 10\text{ V}$ (Note 4)	–	12	15	nC
$Q_{gs}$	Gate-Source Charge		–	2.6	–	nC
$Q_{gd}$	Gate-Drain Charge		–	6.0	–	nC

## DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

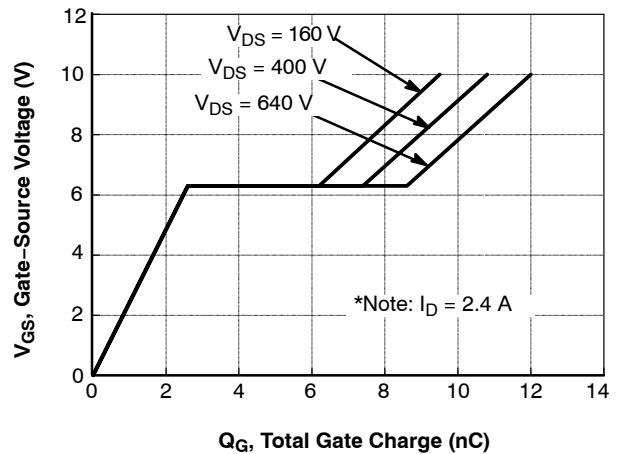
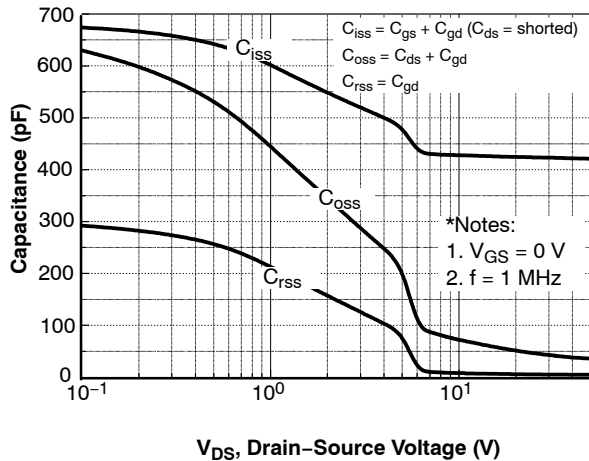
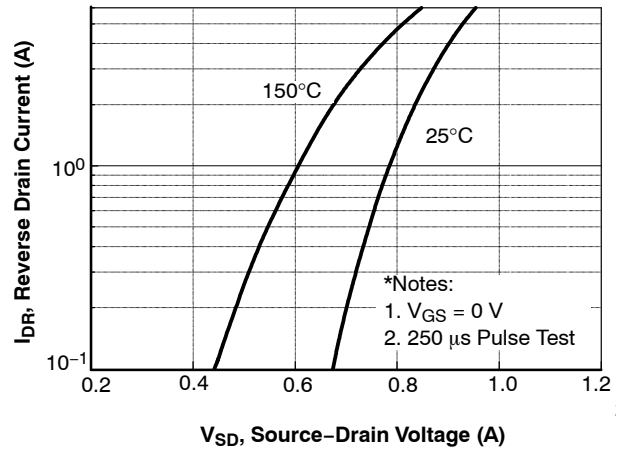
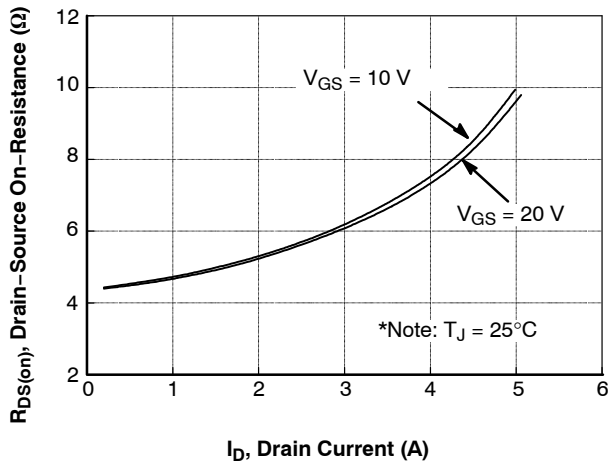
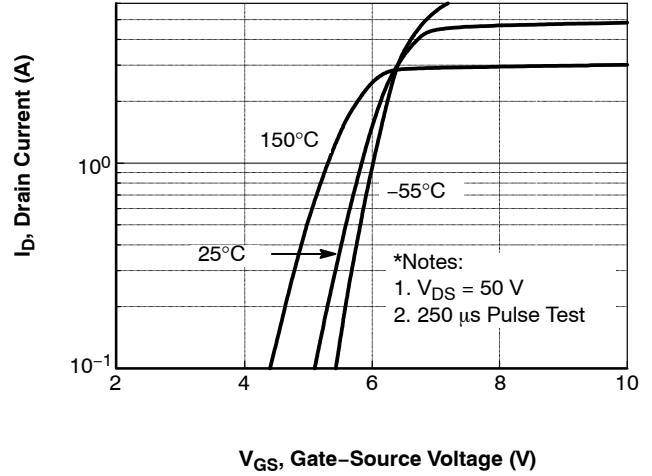
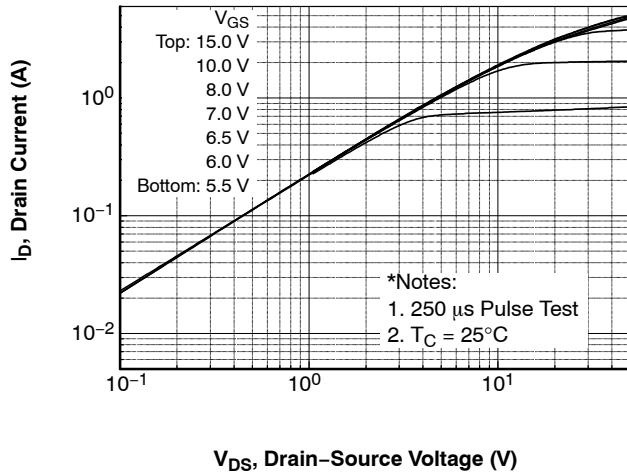
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	–	–	1.5	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	–	–	6.0	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 1.5\text{ A}$	–	–	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}$ , $I_S = 2.4\text{ A}$ , $di_F/dt = 100\text{ A}/\mu\text{s}$	–	480	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	2.0	–	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 150\text{ mH}$ ,  $I_{AS} = 1.5\text{ A}$ ,  $V_{DD} = 50\text{ V}$ ,  $R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 2.4\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

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## TYPICAL CHARACTERISTICS



# FQPF2N80

## TYPICAL CHARACTERISTICS (continued)

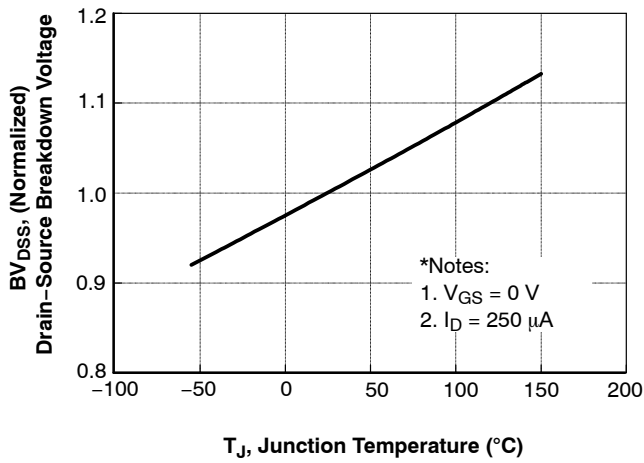


Figure 7. Breakdown Voltage Variation vs. Temperature

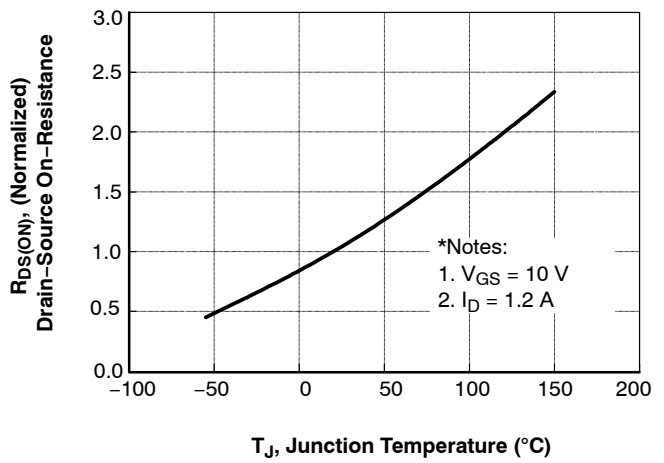


Figure 8. On-Resistance Variation vs. Temperature

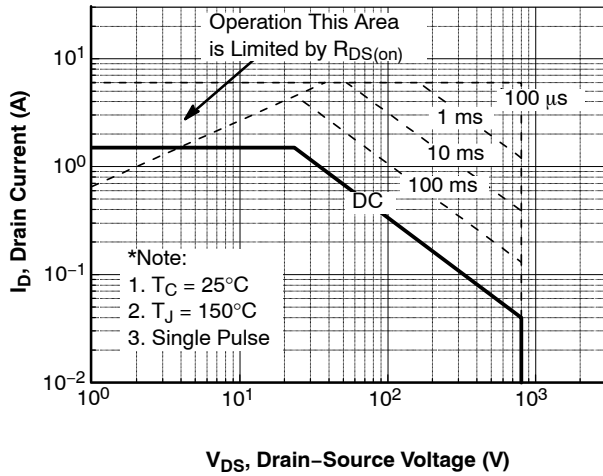


Figure 9. Maximum Safe Operating Area

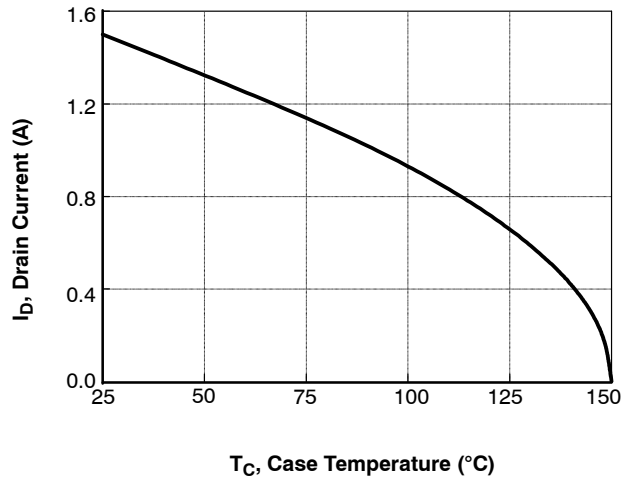


Figure 10. Maximum Drain Current vs. Case Temperature

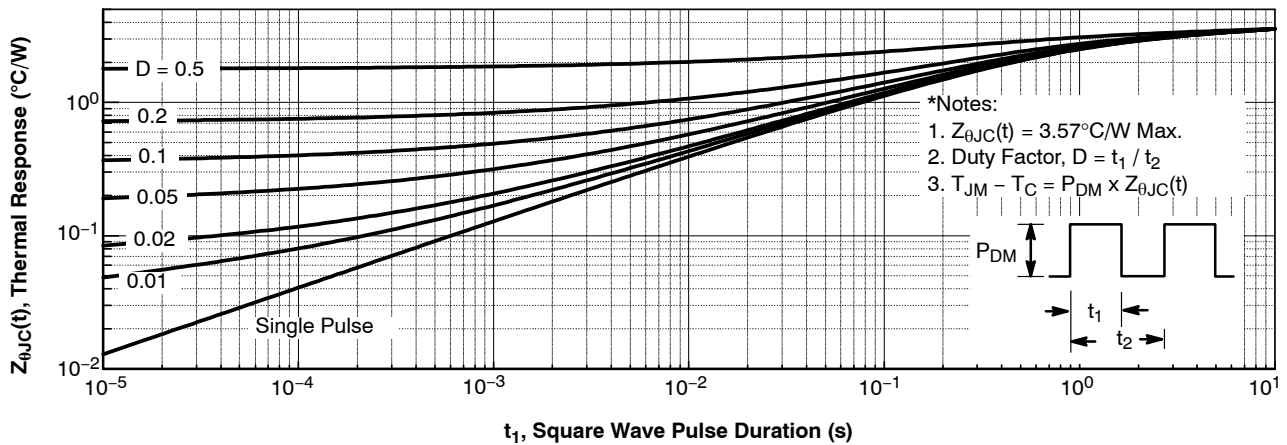


Figure 11. Transient Thermal Response Curve

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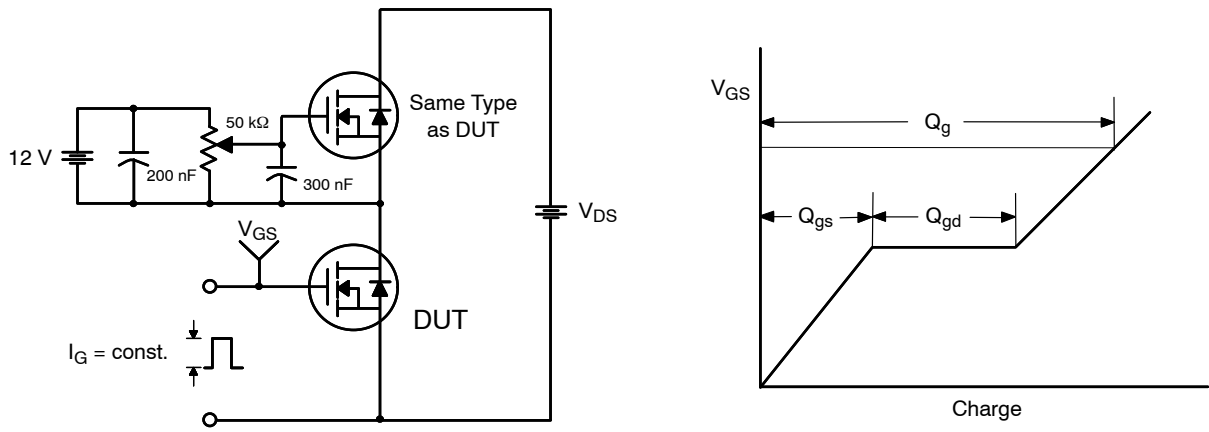


Figure 12. Gate Charge Test Circuit & Waveform

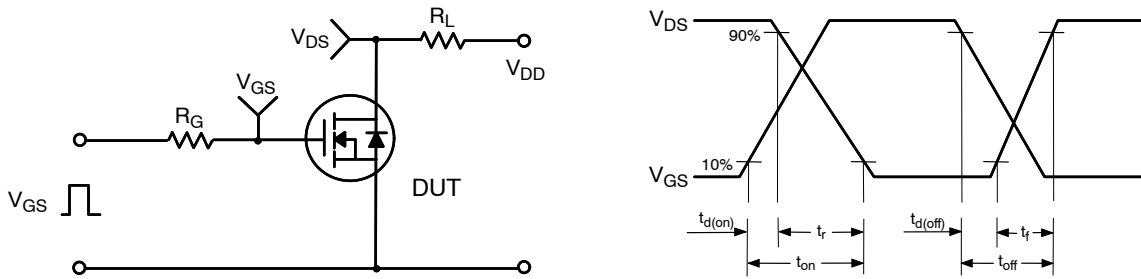


Figure 13. Resistive Switching Test Circuit & Waveforms

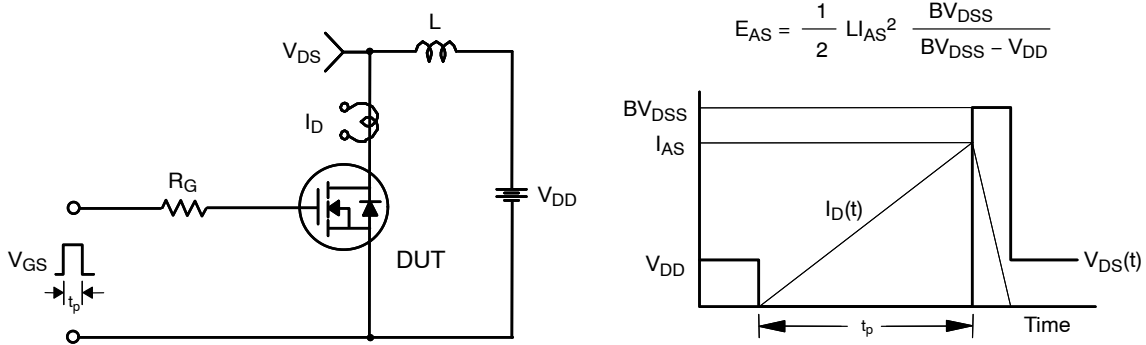


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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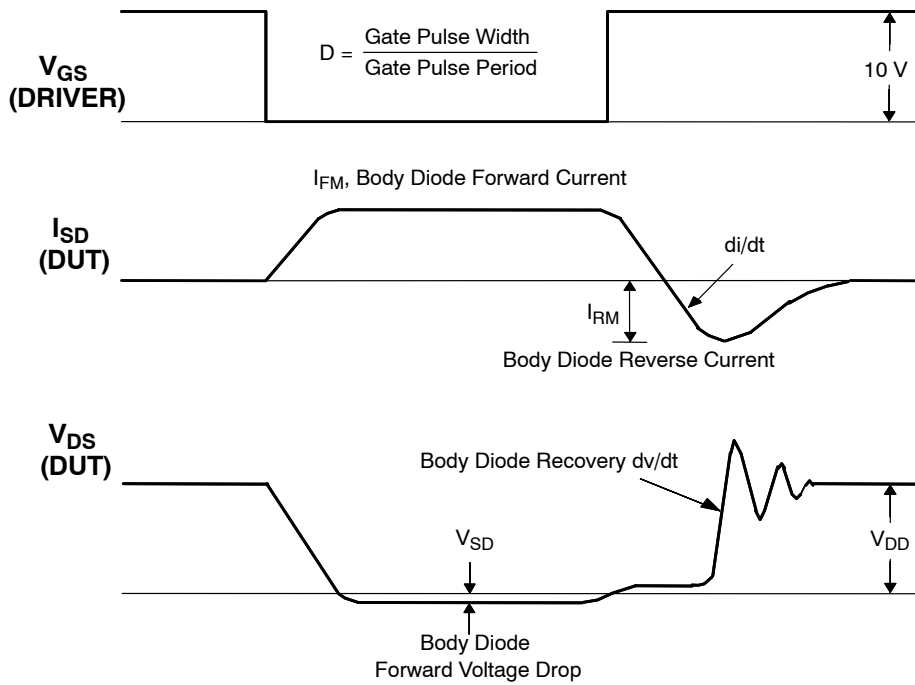
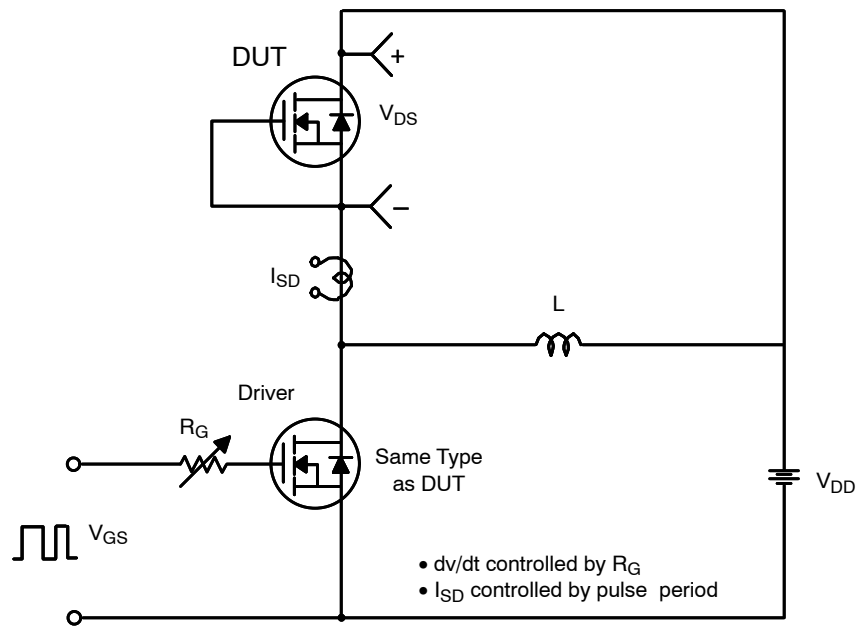


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

# MECHANICAL CASE OUTLINE

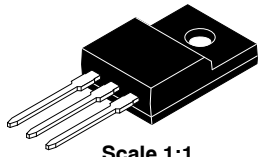
## PACKAGE DIMENSIONS

ON Semiconductor®

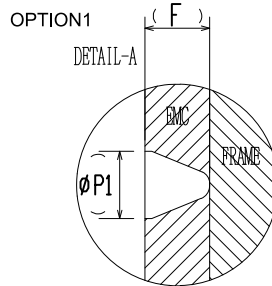
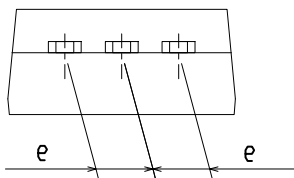
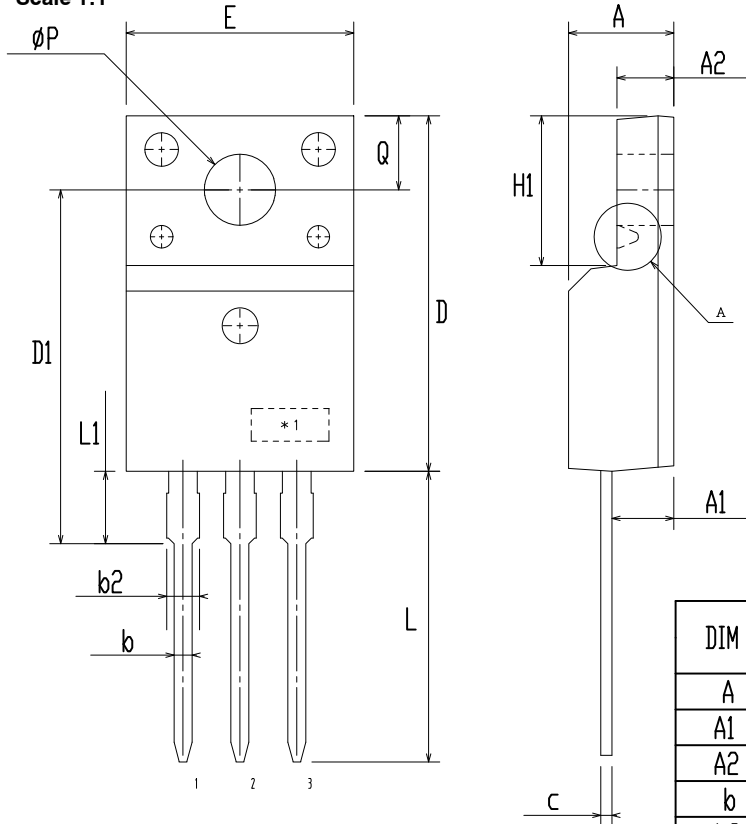


TO-220 Fullpack, 3-Lead / TO-220F-3SG  
CASE 221AT  
ISSUE B

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
∅ P	2.98	3.18	3.38
∅ P1	~	1.00	~
Q	3.20	3.30	3.40

**NOTES:**

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE  
OPTION 2 - NO SUPPORT PIN HOLE

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<b>DESCRIPTION:</b>	<b>TO-220 FULLPACK, 3-LEAD / TO-220F-3SG</b>	<b>PAGE 1 OF 1</b>

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