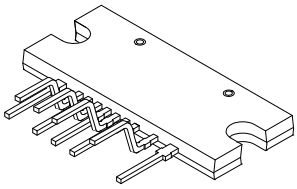
Power Switch for Half-Bridge Resonant Converters

FSFR2100



SIP9 26x10.5
CASE 127EM

Description

The FSFR2100 is a highly integrated power switch designed for high−efficiency half−bridge resonant converters. Offering everything necessary to build a reliable and robust resonant converter, the FSFR2100 simplifies designs and improves productivity, while improving performance. The FSFR2100 combines power MOSFETs with fast−recovery type body diodes, a high−side gate−drive circuit, an accurate current controlled oscillator, frequency limit circuit, soft−start, and built−in protection functions. The high−side gate−drive circuit has a common−mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. The fast−recovery body diode of the MOSFETs improves reliability against abnormal operation conditions, while minimizing the effect of the reverse recovery. Using the zero−voltage−switching (ZVS) technique dramatically reduces the switching losses and efficiency is significantly improved. The ZVS also reduces the switching noise noticeably, which allows a small−sized Electromagnetic Interference (EMI) filter.

The FSFR2100 can be applied to various resonant converter topologies, such as: series resonant, parallel resonant, and LLC resonant converters.

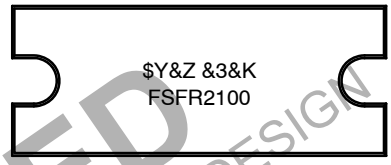
Features

- Variable Frequency Control with 50% Duty Cycle for Half−bridge Resonant Converter Topology
- High Efficiency through Zero Voltage Switching (ZVS)
- Internal SUPERFET® s with Fast−Recovery Type Body Diode (t_{rr} =120 ns)
- Fixed Dead Time (350 ns) Optimized for MOSFETs
- Up to 300kHz Operating Frequency
- Pulse Skipping for Frequency Limit (Programmable) at Light−Load Condition
- Remote On/Off Control Using Control Pin
- Protection Functions: Over−Voltage Protection (OVP), Over−Load Protection (OLP), Over−Current Protection (OCP), Abnormal Over−Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- PDP and LCD TVs
- Desktop PCs and Servers
- Adapters
- Telecom Power Supplies
- Audio Power Supplies

MARKING DIAGRAM



$Y	= Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code
FSFR2100	= Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Related Resources

- AN−4151 — Half−Bridge LLC Resonant Converter Design Using FSFR2100 Power Switch
- Evaluation Board: FEBFSFR2100_D015v1

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ORDERING INFORMATION

Part Number	Package	Operating Junction Temperature	$R_{DS(ON\_MAX)}$	Maximum Output Power without Heatsink (V_{IN} = 350~400 V) (Note 1, 2)	Maximum Output Power with Heatsink (V_{IN} = 350~400 V) (Note 1, 2)	Shipping
FSFR2100	9−SIP	−40 to +130°C	0.38 Ω	200 W	450 W	475 Units / Tube

1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open−frame design at 50°C ambient.

APPLICATION CIRCUIT DIAGRAM

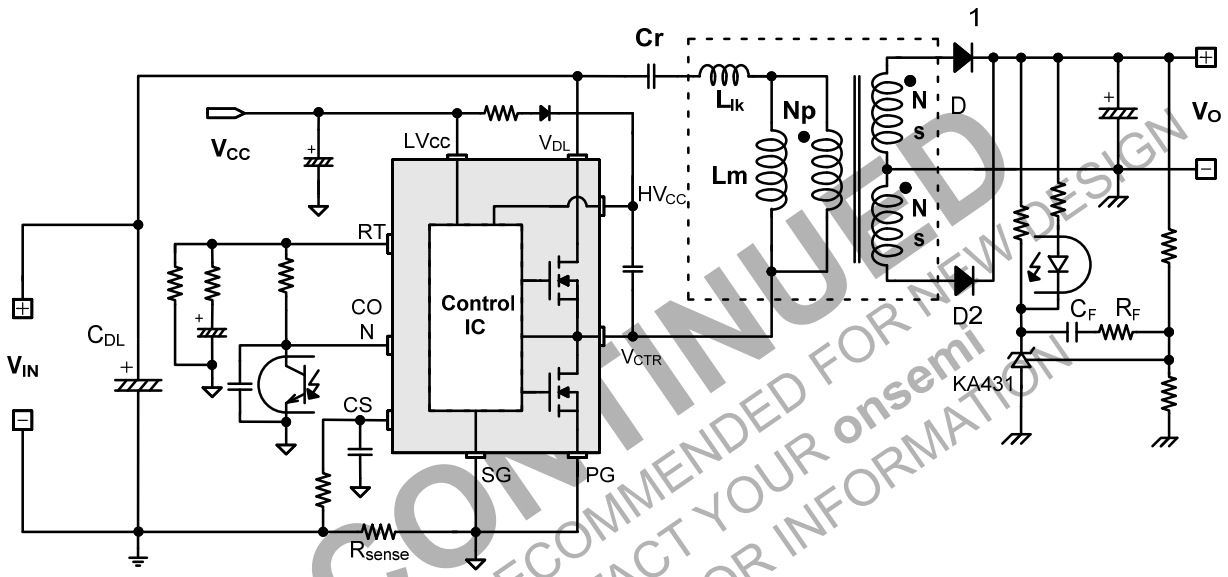

Figure 1. Typical Application Circuit (LLC Resonant Half−Bridge Converter)

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BLOCK DIAGRAM

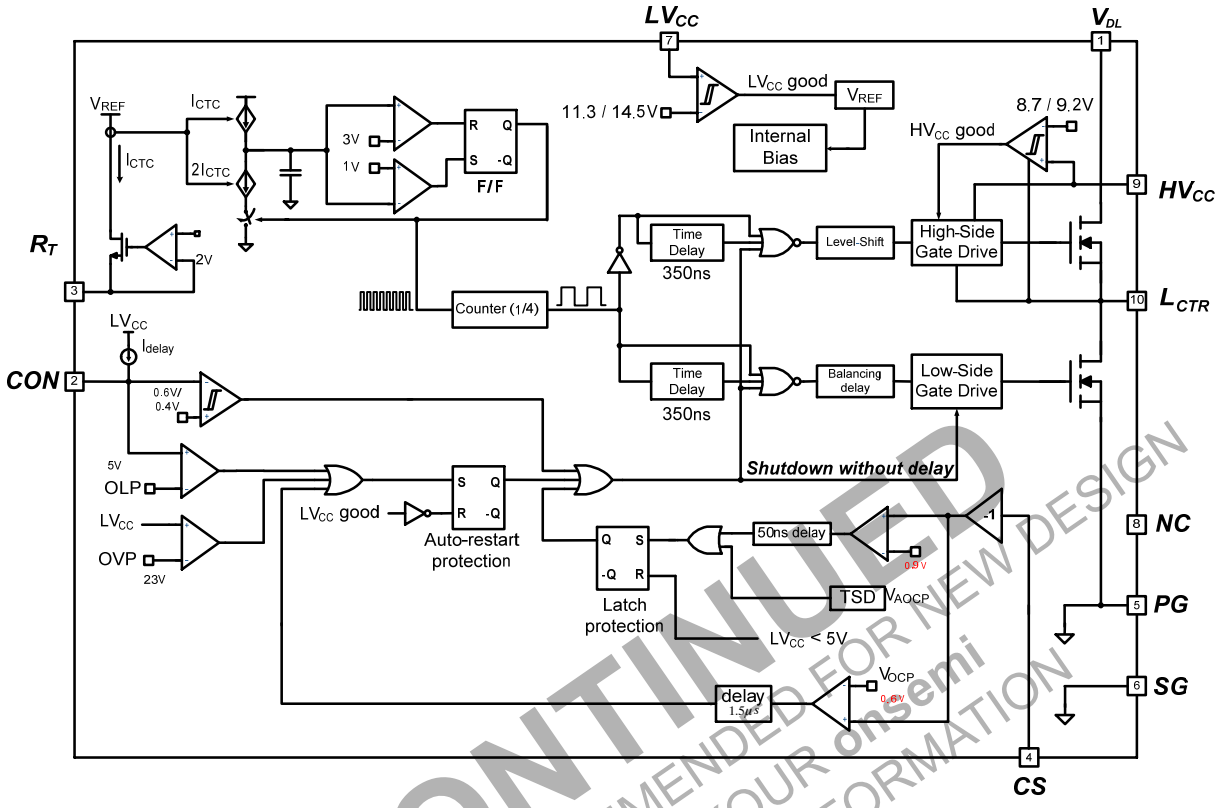

Figure 2. Internal Block Diagram

PIN CONFIGURATION

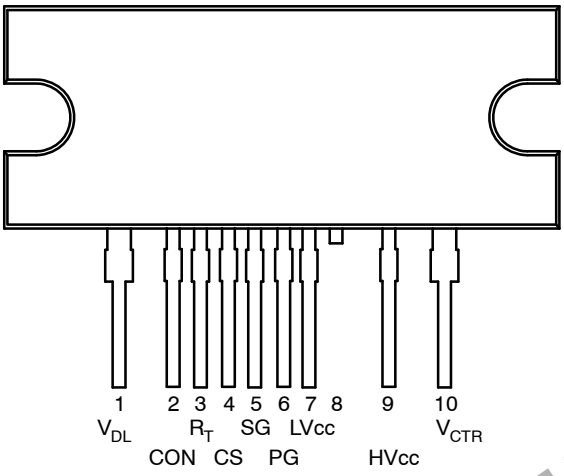

Figure 3. Package Diagram

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PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{DL}	This is the drain of the high−side MOSFET, typically connected to the input DC link voltage.
2	CON	This pin is for enable/disable and protection. When the voltage of this pin is above 0.6 V, the IC operation is enabled. When the voltage of this pin drops below 0.4 V, gate drive signals for both MOSFETs are disabled. When the voltage of this pin increases above 5 V, protection is triggered.
3	R_T	This pin programs the switching frequency. Typically, an opto−coupler is connected to control the switching frequency for the output voltage regulation.
4	CS	This pin senses the current flowing through the low−side MOSFET. Typically, negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low−side MOSFET.
7	LV_{CC}	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	HV_{CC}	This is the supply voltage of the high−side gate−drive circuit IC.
10	V_{CTR}	This is the drain of the low−side MOSFET. Typically, a transformer is connected to this pin.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Min	Max	Unit
V_{DS}	Maximum Drain−to−Source Voltage (V_{DL}−V_{CTR} and V_{CTR}−PG)	600	–	V
LV_{CC}	Low−Side Supply Voltage	−0.3	25.0	V
HV_{CC} to V_{CTR}	High−Side V_{CC} Pin to Low−Side Drain Voltage	−0.3	25.0	V
HV_{CC}	High−Side Floating Supply Voltage	−0.3	625.0	V
V_{CON}	Control Pin Input Voltage	−0.3	LV_{CC}	V
V_{CS}	Current−Sense (CS) Pin Input Voltage	−5.0	1.0	V
V_{RT}	R_T Pin Input Voltage	−0.3	5.0	V
dV_{CTR}/dt	Allowable Low−Side MOSFET Drain Voltage Slew Rate	–	50	V/ns
P_D	Total Power Dissipation (Note 3)	–	12	W
T_J	Maximum Junction Temperature (Note 4)	–	+150	°C
	Recommended Operating Junction Temperature (Note 4)	−40	+130	
T_{STG}	Storage Temperature Range	−55	+150	°C

MOSFET SECTION

V_{DGR}	Drain Gate Voltage (R_{GS} = 1 MΩ)		600	–	V
V_{GS}	Gate Source (GND) Voltage		–	±30	V
I_{DM}	Drain Current Pulsed (Note 5)		–	33	A
I_D	Continuous Drain Current	T_C = 25°C	–	11	A
		T_C = 100°C	–	7	

PACKAGE SECTION

Torque	Recommended Screw Torque	5~7	kgf·cm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Per MOSFET when both MOSFETs are conducting.
4. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.
5. Pulse width is limited by maximum junction temperature.

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THERMAL IMPEDANCE (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
θ_{JC}	Junction−to−Case Center Thermal Impedance (Both MOSFETs Conducting)	10.44	°C/W
θ_{JA}	Junction−to−Ambient Thermal Impedance	80	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
MOSFET SECTION						
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 200 μA, T_A = 25°C	600	–	–	V
		I_D = 200 μA, T_A = 125°C	–	650	–	
$R_{DS(ON)}$	On−State Resistance	V_{GS} = 10 V, I_D = 5.5 A	–	0.32	0.38	Ω
t_{rr}	Body Diode Reverse Recovery Time (Note 6)	V_{GS} = 0 V, I_{Diode} = 11.0 A	–	120	–	ns
C_{ISS}	Input Capacitance (Note 6)	V_{DS} = 25V, V_{GS} = 0 V, f = 1.0 MHz	–	1148	–	pF
C_{OSS}	Output Capacitance (Note 6)		–	671	–	pF
SUPPLY SECTION						
I_{LK}	Offset Supply Leakage Current	H−V_{CC} = V_{CTR} = 600 V/500 V	–	–	50	μA
I_QHV_{CC}	Quiescent HV_{CC} Supply Current	(HV_{CC}UV+) − 0.1 V	–	50	120	μA
I_QLV_{CC}	Quiescent LV_{CC} Supply Current	(LV_{CC}UV+) − 0.1 V	–	100	200	μA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SUPPLY SECTION						
I_OHV_{CC}	Operating HV_{CC} Supply Current (RMS Value)	f_{OSC} = 100 kHz, V_{CON} > 0.6 V	–	6	9	mA
		No Switching, V_{CON} < 0.4 V	–	100	200	μA
I_OLV_{CC}	Operating LV_{CC} Supply Current (RMS Value)	f_{OSC} = 100 kHz, V_{CON} > 0.6 V	–	7	11	mA
		No Switching, V_{CON} < 0.4 V	–	2	4	mA
UVLO SECTION						
$LV_{CC}UV+$	LV_{CC} Supply Under−Voltage Positive−Going Threshold (LV_{CC} Start)		13.0	14.5	16.0	V
$LV_{CC}UV-$	LV_{CC} Supply Under−Voltage Negative−Going Threshold (LV_{CC} Stop)		10.2	11.3	12.4	V
$LV_{CC}UVH$	LV_{CC} Supply Under−Voltage Hysteresis		–	3.2	–	V
$HV_{CC}UV+$	HV_{CC} Supply Under−Voltage Positive−Going Threshold (HV_{CC} Start)		8.2	9.2	10.2	V
$HV_{CC}UV-$	HV_{CC} Supply Under−Voltage Negative−Going Threshold (HV_{CC} Stop)		7.8	8.7	9.6	V
$HV_{CC}UVH$	HV_{CC} Supply Under−Voltage Hysteresis		–	0.5		V
OSCILLATOR & FEEDBACK SECTION						
V_{CONDIS}	Control Pin Disable Threshold Voltage		0.36	0.40	0.44	V
V_{CONEN}	Control Pin Enable Threshold Voltage		0.54	0.60	0.66	V
V_{RT}	V−I Converter Threshold Voltage	R_T = 5.2 KΩ	1.5	2.0	2.5	V
f_{OSC}	Output Oscillation Frequency		94	100	106	kHz
DC	Output Duty Cycle		48	50	52	%
f_{SS}	Internal Soft−Start Initial Frequency	$f_{SS} = f_{OSC}$ + 40 kHz, R_T = 5.2 kΩ	–	140	–	kHz
t_{SS}	Internal Soft−Start Time		2	3	4	ms
PROTECTION SECTION						
I_{OLP}	OLP Delay Current	V_{CON} = 4 V	3.6	4.8	6.0	μA
V_{OLP}	OLP Protection Voltage	V_{CON} > 3.5 V	4.5	5.0	5.5	V
V_{OVP}	LV_{CC} Over−Voltage Protection	$L-V_{CC}$ > 21 V	21	23	25	V
V_{AOCP}	AOCP Threshold Voltage	ΔV/Δt = −0.1 V/μs	−1.0	−0.9	−0.8	V
t_{BAO}	AOCP Blanking Time (Note 6)	V_{CS} < V_{AOCP}; ΔV/Δt = −0.1 V/μs	–	50	–	ns
V_{OCP}	OCP Threshold Voltage	V/Δt = −1 V/μs	−0.64	−0.58	−0.52	V
t_{BO}	OCP Blanking Time (Note 6)	V_{CS} < V_{OCP}; ΔV/Δt = −1 V/μs	1.0	1.5	2.0	μs
t_{DA}	Delay Time (Low Side) Detecting from V_{AOCP} to Switch Off (Note 6)	ΔV/Δt = −1 V/μs	–	250	400	ns
T_{SD}	Thermal Shutdown Temperature (Note 6)		110	130	150	°C
I_{SU}	Protection Latch Sustain LV_{CC} Supply Current	LV_{CC} = 7.5 V	–	100	150	μA
V_{PRSET}	Protection Latch Reset LV_{CC} Supply Voltage		5	–	–	V
DEAD−TIME CONTROL SECTION						
D_T	Dead Time (Note 7)		–	350	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. This parameter, although guaranteed, is not tested in production.
7. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

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TYPICAL PERFORMANCE CHARACTERISTICS

(These characteristic graphs are normalized at T_A = 25°C)

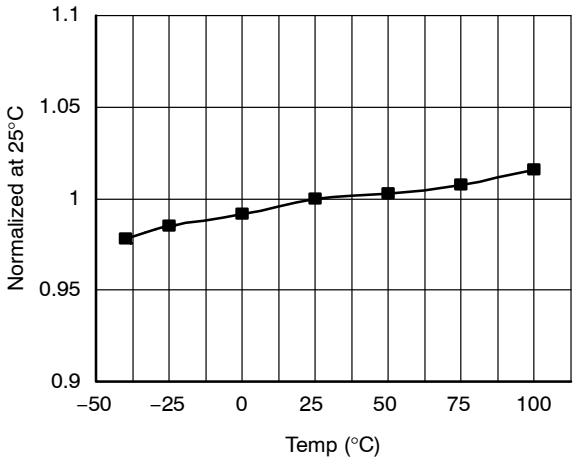

Figure 4. Low−Side MOSFET Duty Cycle vs. Temperature

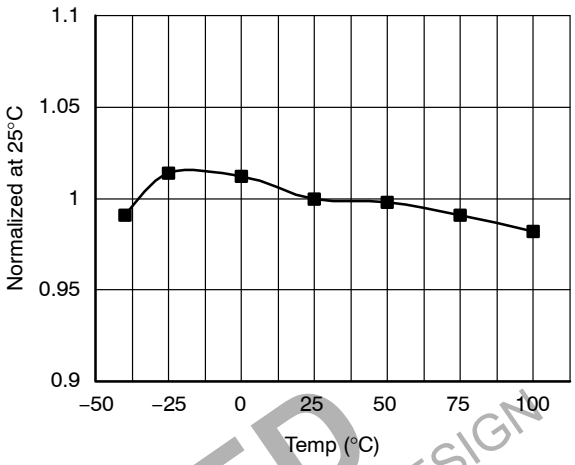

Figure 5. Switching Frequency vs. Temperature

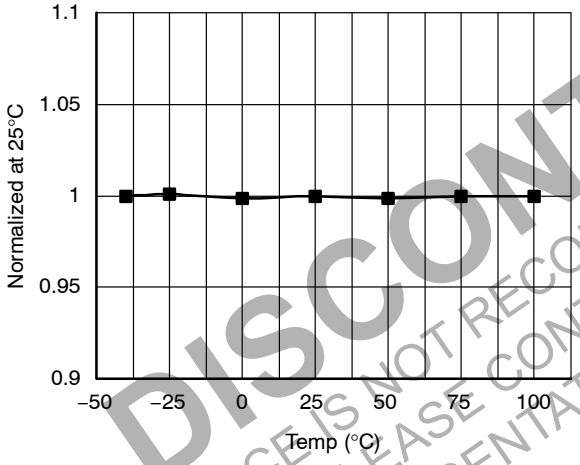

Figure 6. High−Side V_{CC} (HV_{CC}) Start vs. Temperature

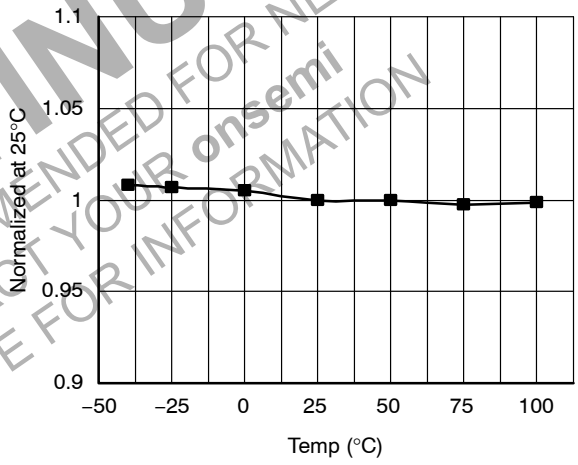

Figure 7. High−Side V_{CC} (HV_{CC}) Stop vs. Temperature

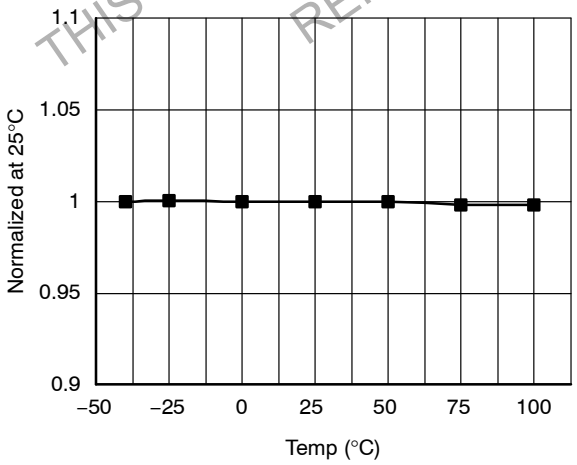

Figure 8. Low−Side V_{CC} (LV_{CC}) Start vs. Temperature

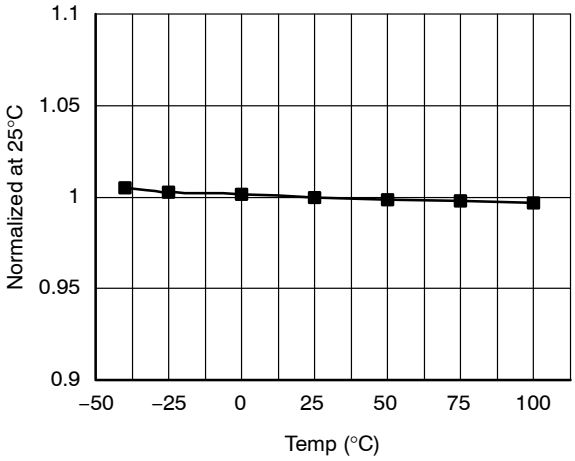

Figure 9. Low−Side V_{CC} (LV_{CC}) Stop vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(These characteristic graphs are normalized at T_A = 25°C)

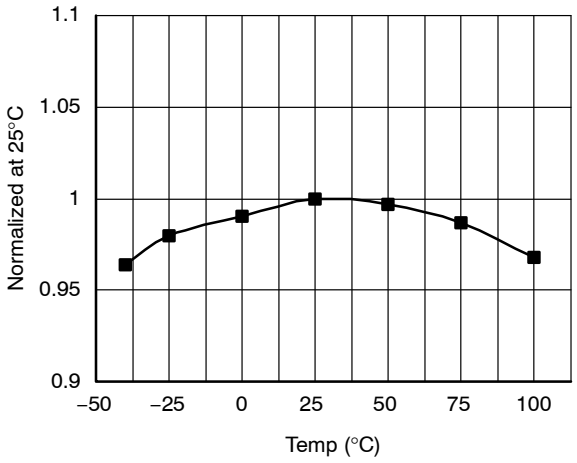

Figure 10. OLP Delay Current vs. Temperature

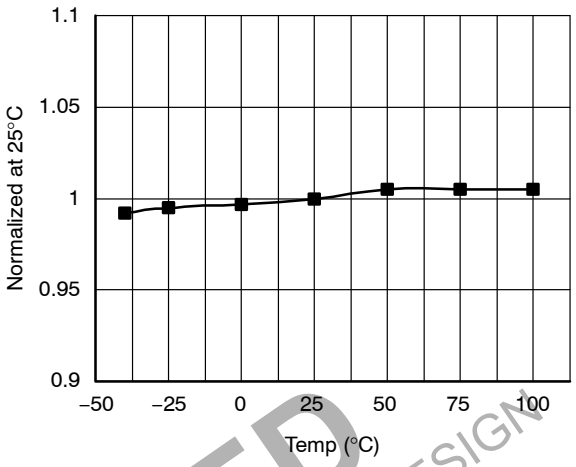

Figure 11. OLP Protection Voltage vs. Temperature

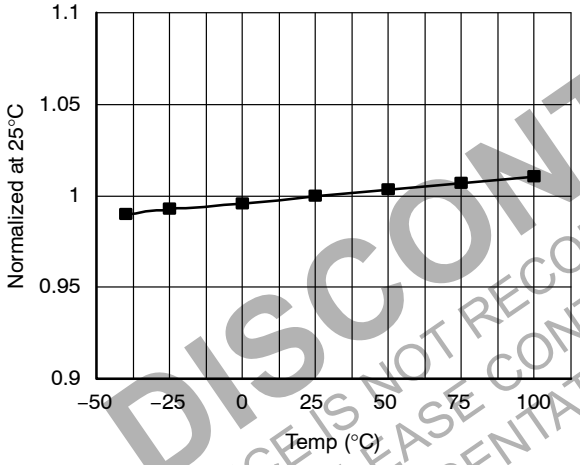

Figure 12. LV_{CC} OVP Voltage vs. Temperature

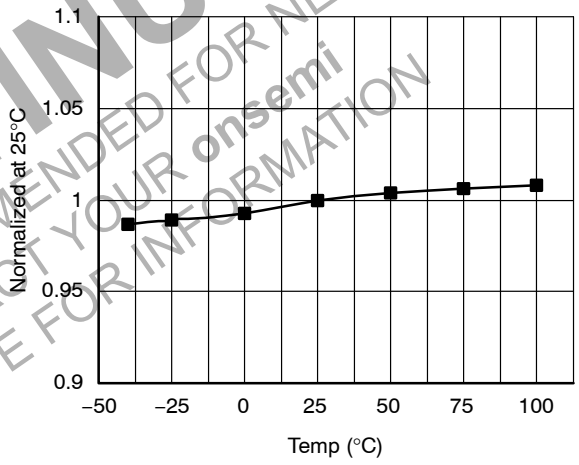

Figure 13. R_T Voltage vs. Temperature

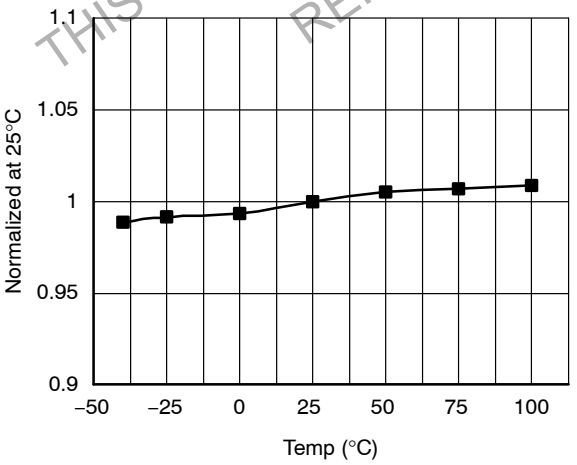

Figure 14. CON Pin Enable Voltage vs. Temperature

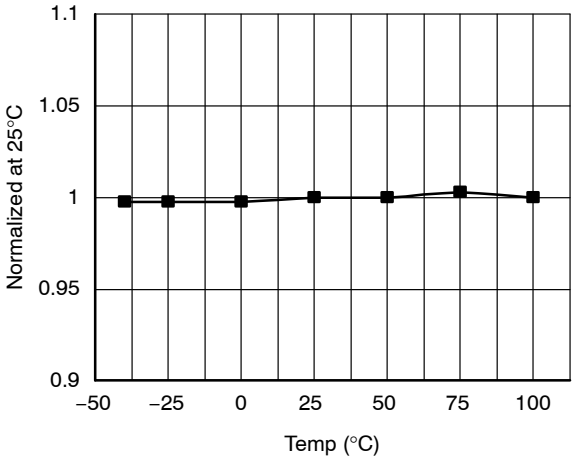

Figure 15. OCP Voltage vs. Temperature

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FUNCTIONAL DESCRIPTION

Basic Operation

FSFR2100 is designed to drive high−side and low−side MOSFETs complementarily with 50% duty cycle. A fixed dead time of 350 ns is introduced between consecutive transitions, as shown in Figure 16.

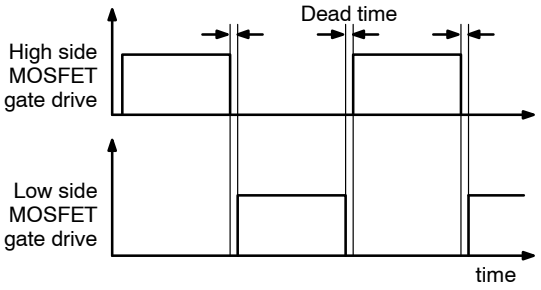

Figure 16. MOSFETs Gate Drive Signal

Internal Oscillator

FSFR2100 employs a current−controlled oscillator, as shown in Figure 17. Internally, the voltage of R_T pin is regulated at 2 V and the charging/discharging current for the oscillator capacitor, C_T, is obtained by copying the current flowing out of R_T pin (I_{CTC}) using a current mirror. Therefore, the switching frequency increases as I_{CTC} increases.

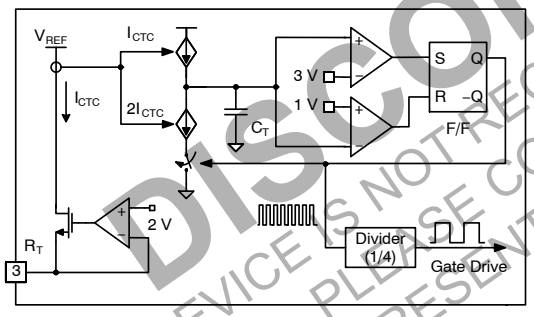

Figure 17. Current−Controlled Oscillator

Frequency Setting

Figure 18 shows a typical voltage gain curve of a resonant converter, where the gain is inversely proportional to the switching frequency in the ZVS region. The output voltage can be regulated by modulating the switching frequency. Figure 19 shows the typical circuit configuration for R_T pin, where the opto−coupler transistor is connected to the R_T pin to modulate the switching frequency.

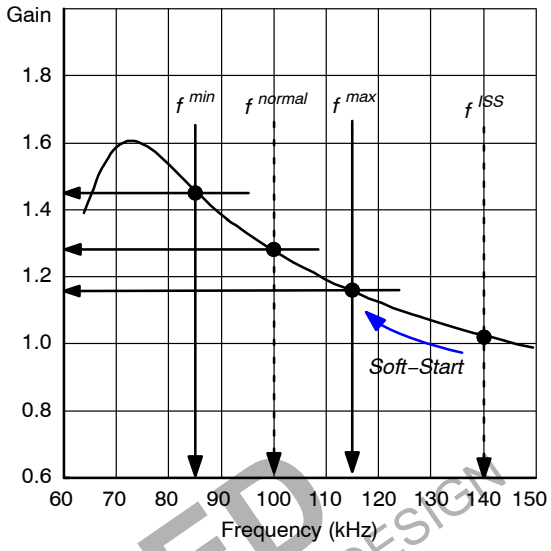

Figure 18. Resonant Converter Typical Gain Curve

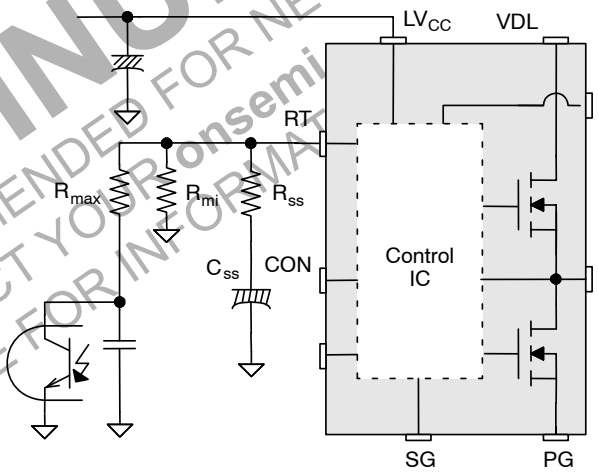

Figure 19. Frequency Control Circuit

The minimum switching frequency is determined as:

$$f^{min} = \frac{5.2\ k\Omega}{R_{min}} \times 100\ (kHz) \qquad \text{(eq. 1)}$$

Assuming the saturation voltage of opto−coupler transistor is 0.2 V, the maximum switching frequency is determined as:

$$f^{max} = \left(\frac{5.2\ k\Omega}{R_{min}} + \frac{4.68\ k\Omega}{R_{max}}\right) \times 100\ (kHz) \qquad \text{(eq. 2)}$$

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To prevent excessive inrush current and overshoot of output voltage during startup, increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, the soft−start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established. The soft−start circuit is made by connecting R−C series network on the R_T pin, as shown in Figure 19. FSFR2100 also has an internal soft−start for 3 ms to reduce the current overshoot during the initial cycles, which adds 40 kHz to the initial frequency of the external soft−start circuit, as shown in Figure 20. The initial frequency of the soft−start is given as:

$$f^{ISS} = \left(\frac{5.2\ k\Omega}{R_{min}} + \frac{5.2\ k\Omega}{R_{SS}}\right) \times 100 + 40\ (kHz) \qquad \text{(eq. 3)}$$

It is typical to set the initial frequency of soft−start two~three times the resonant frequency (f_O) of the resonant network.

The soft−start time is three to four times of the RC time constant. The RC time constant is as follows:

$$T_{SS} = R_{SS} \cdot C_{SS} \qquad \text{(eq. 4)}$$

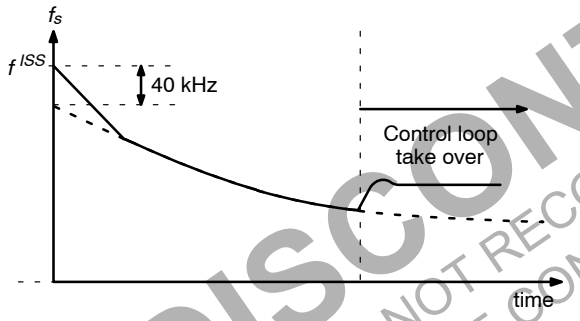

Figure 20. Frequency Sweeping of Soft−start

Control Pin

The FSFR2100 has a control pin for protection, cycle skipping, and remote on/off. Figure 21 shows the internal block diagram for control pin.

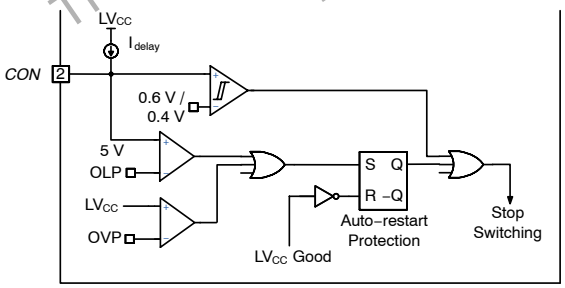

Figure 21. Internal Block of Control Pin

Protection

When the control pin voltage exceeds 5 V, protection is triggered. Detailed applications are described in the protection section.

Pulse Skipping

FSFR2100 stops switching when the control pin voltage drops below 0.4 V and resumes switching when the control pin voltage rises above 0.6 V. To use pulse−skipping, the control pin should be connected to the opto−coupler collector pin. The frequency that causes pulse skipping is given as:

$$f^{SKIP} = \left(\frac{5.2\ k\Omega}{R_{min}} + \frac{4.16\ k\Omega}{R_{max}}\right) \times 100\ (kHz) \qquad \text{(eq. 5)}$$

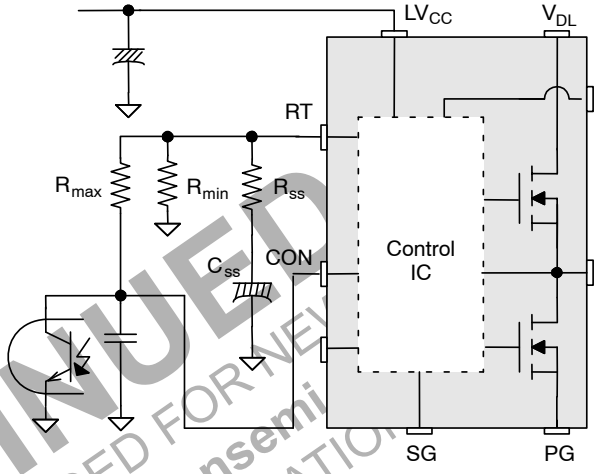

Figure 22. Control Pin Configuration for Pulse Skipping

Remote On / Off

When an auxiliary power supply is used for standby, the main power stage using FSFR2100 can be shut down by pulling down the control pin voltage, as shown in Figure 23. R1 and C1 are used to ensure soft−start when switching resumes.

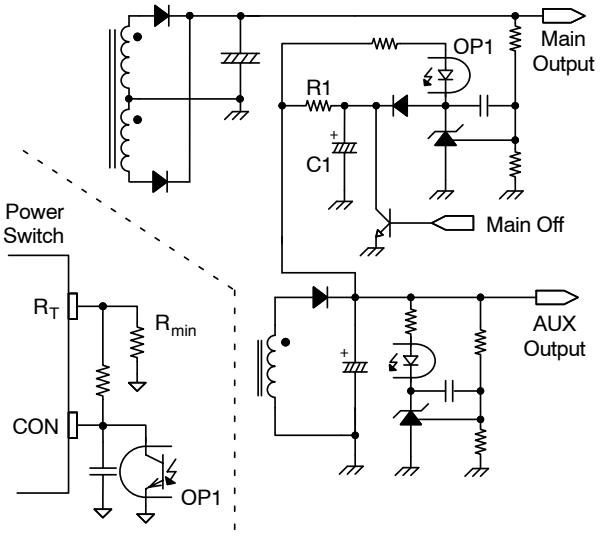

Figure 23. Remote On / Off Circuit

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Current Sensing

Current Sensing Using Resistor

FSFR2100 senses drain current as a negative voltage, as shown in Figure 24 and Figure 25. Half−wave sensing allows low power dissipation in the sensing resistor, while full−wave sensing has less switching noise in the sensing signal.

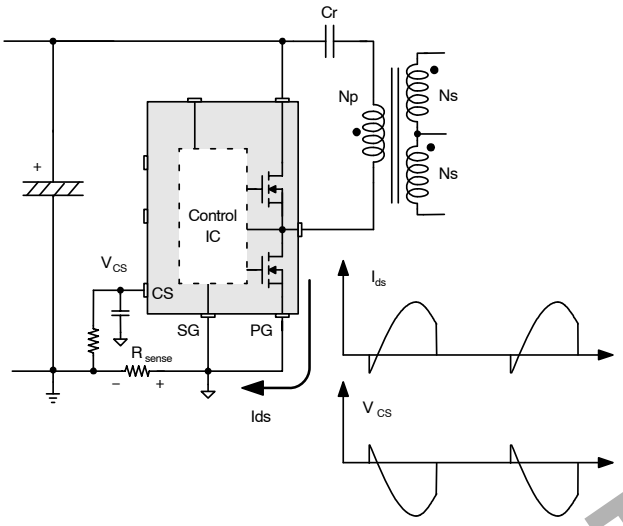

Figure 24. Half−Wave Sensing

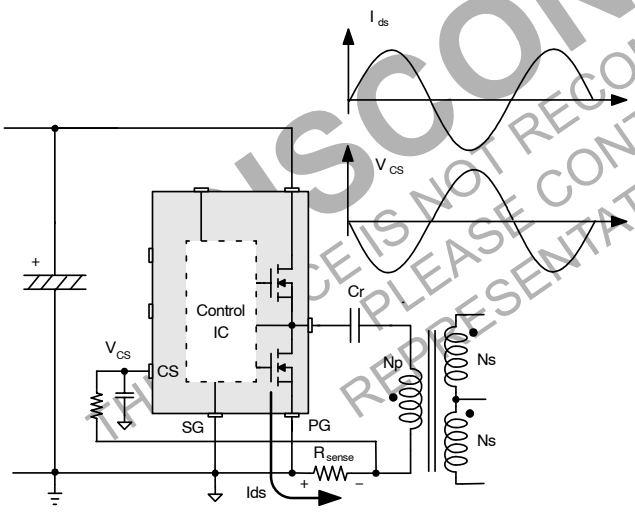

Figure 25. Full−Wave Sensing

Current Sensing Using Resonant Capacitor Voltage

For high−power applications, current sensing using a resistor may not be available due to the severe power dissipation in the resistor. In that case, indirect current sensing using the resonant capacitor voltage can be a good alternative because the amplitude of the resonant capacitor voltage (V_{cr}^{p-p}) is proportional to the resonant current in the primary side (I_p^{p-p}) as:

$$V_{Cr}^{p-p} = \frac{I_p^{p-p}}{2\pi f_s C_r} \quad \text{(eq. 6)}$$

To minimize power dissipation, a capacitive voltage divider is generally used for capacitor voltage sensing, as shown in Figure 26.

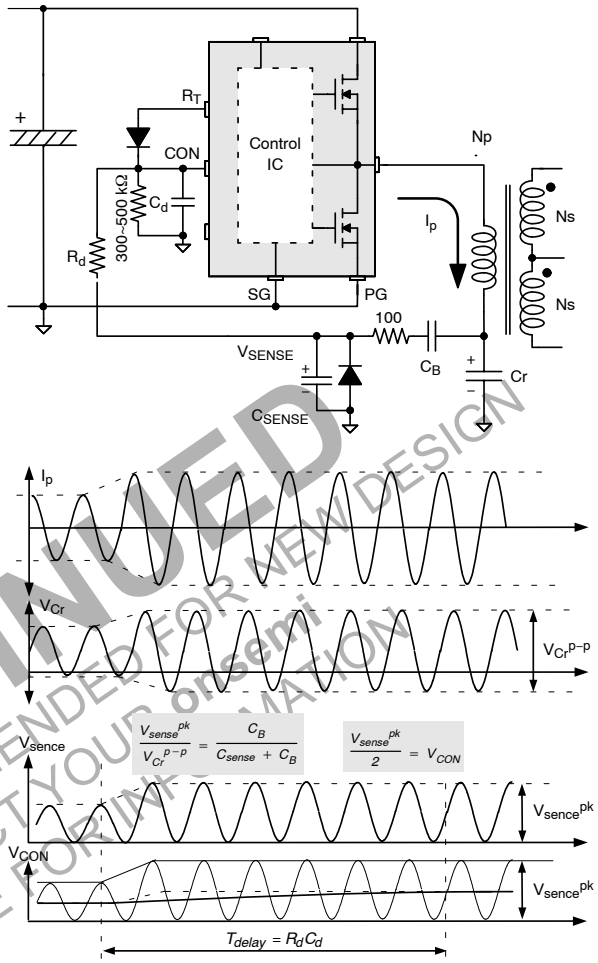

Figure 26. Current Sensing Using Resonant Capacitor Voltage

Protection Circuits

The FSFR2100 has several self−protective functions, such as Overload Protection (OLP), Over−Current Protection (OCP), Abnormal Over−Current Protection (AOCP), Over−Voltage Protection (OVP), and Thermal Shutdown (TSD). OLP, OCP, and OVP are auto−restart mode protections; while AOCP and TSD are latch−mode protections, as shown in Figure 27.

Auto−restart Mode Protection

Once a fault condition is detected, switching is terminated and the MOSFETs remain off. When LV_{CC} falls to the LV_{CC} stop voltage of 11.3 V, the protection is reset. The power switch resumes normal operation when LV_{CC} reaches the start voltage of 14.5 V.

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Latch−Mode Protection

Once this protection is triggered, switching is terminated and the MOSFETs remain off. The latch is reset only when LV_{CC} is discharged below 5 V.

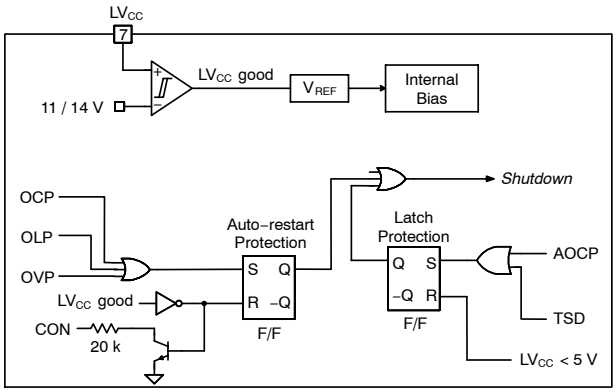

Figure 27. Protection Blocks

Over−Current Protection (OCP)

When the sensing pin voltage drops below −0.58 V, OCP is triggered and the MOSFETs remain off. This protection has a shutdown time delay of 1.5 μs to prevent premature shutdown during startup.

Abnormal Over−Current Protection (AOCP)

If the secondary rectifier diodes are shorted, large current with extremely high di/dt can flow through the MOSFET before OCP or OLP is triggered. AOCP is triggered without shutdown delay when the sensing pin voltage drops below −0.9 V. This protection is latch mode and reset when LV_{CC} is pulled down below 5 V.

Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the power supply. However, even when the power supply is in the normal condition, the overload situation can occur during the load transition. To avoid premature triggering of protection, the overload protection circuit should be designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Figure 26 shows a typical overload protection circuit. By sensing the resonant capacitor voltage on the control pin, the overload protection can be implemented. Using RC time constant, shutdown delay can be also introduced. The voltage obtained on the control pin is given as:

$$V_{CON} = \frac{C_B}{2(C_B + C_{sense})} V_{Cr}^{p-p} \qquad \text{(eq. 7)}$$

where V_{Cr}^{p-p} is the amplitude of the resonant capacitor voltage.

Over−Voltage Protection (OVP)

When the LV_{CC} reaches 23 V, OVP is triggered. This protection is used when auxiliary winding of the transformer to supply V_{CC} to power switch is utilized.

Thermal Shutdown (TSD)

The MOSFETs and the control IC in one package makes it easy for the control IC to detect the abnormal over−temperature of the MOSFETs. If the temperature exceeds approximately 130°C, the thermal shutdown triggers.

PCB Layout Guidelines

Duty unbalance problems may occur due to the radiated noise from main transformer, the inequality of the secondary side leakage inductances of main transformer, and so on. Among them, it is one of the dominant reasons that the control components in the vicinity of R_T pin are enclosed by the primary current flow pattern on PCB layout. The direction of the magnetic field on the components caused by the primary current flow is changed when the high and low side MOSFET turns on by turns. The magnetic fields with opposite direction from each other induce a current through, into, or out of the R_T pin, which makes the turn−on duration of each MOSFET different. It is highly recommended to separate the control components in the vicinity of R_T pin from the primary current flow pattern on PCB layout. Figure 28 shows an example for the duty balanced case.

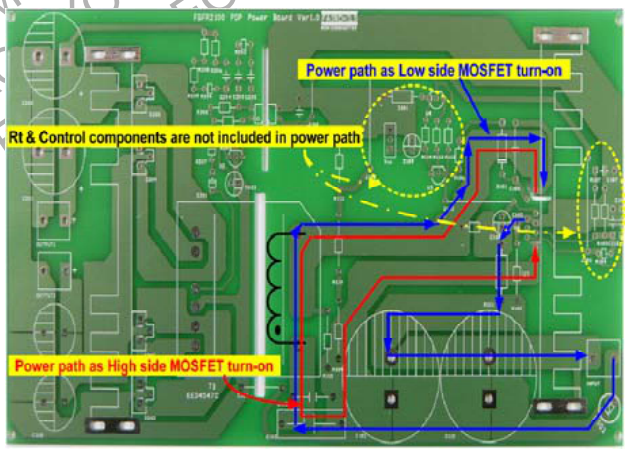

Figure 28. Example for Duty Balancing

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TYPICAL APPLICATION CIRCUIT (HALF−BRIDGE LLC RESONANT CONVERTER)

Table 1.

Application	Power Switch Device	Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
LCD TV	FSFR2100	390 V_{DC} (340~400 V_{DC})	200 W	24 V − 8.3 A

Features

- High efficiency (>94% at 400 V_{DC} input)
- Reduced EMI noise through zero−voltage−switching (ZVS)
- Enhanced system reliability with various protection functions

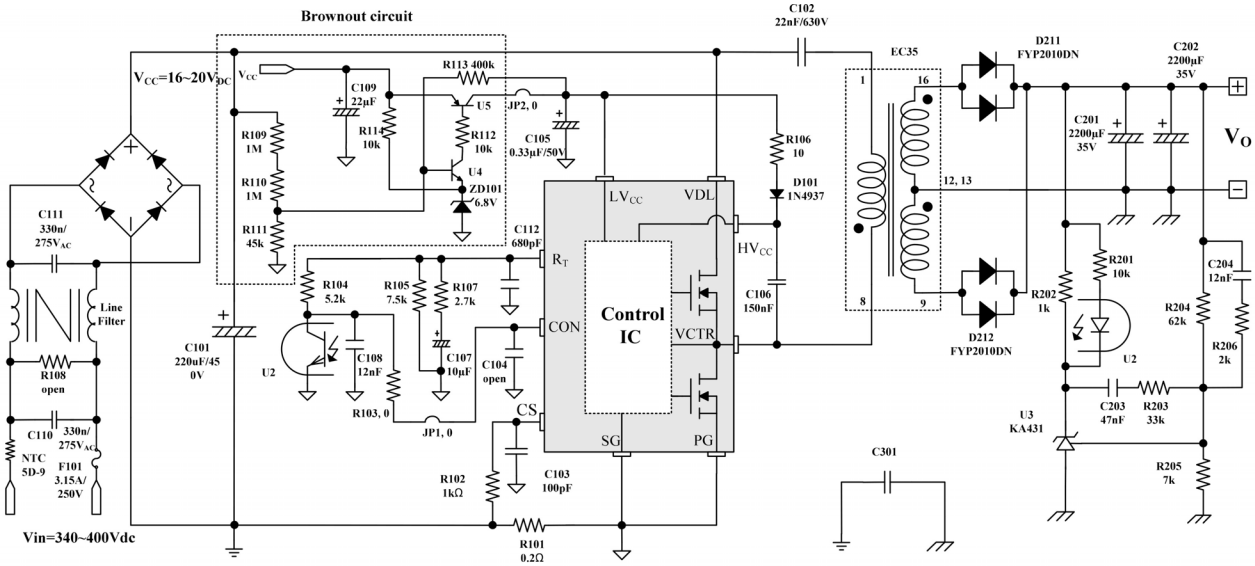

Figure 29. Typical Application Circuit

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TYPICAL APPLICATION CIRCUIT (Continued)

Usually, LLC resonant converters require large leakage inductance value. To obtain a large leakage inductance, sectional winding method is used.

- Core: EC35 (Ae = 106 mm2)
- Bobbin: EC35 (Horizontal)
- Transformer Model Number: SNX−2468−1

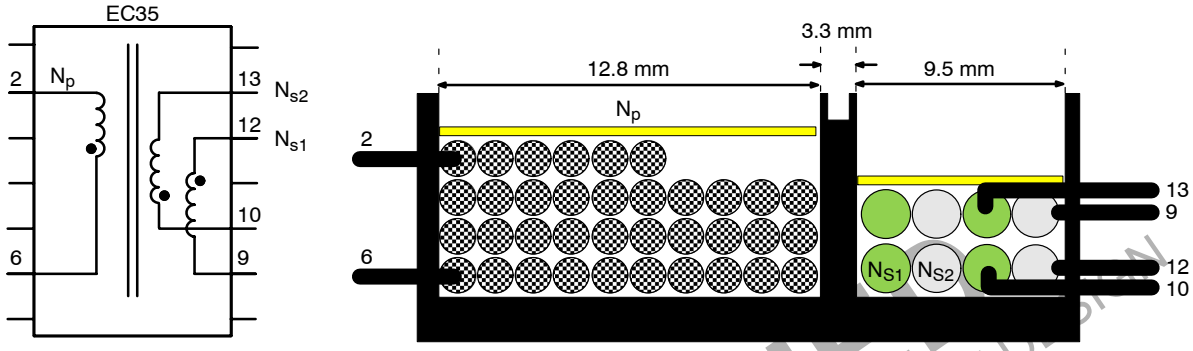

Figure 30. Transformer Construction

Table 2.

	Pin (S → F)	Wire	Turns	Note
N_p	6 → 2	0.08φ x 88 (Litz Wire)	36	
N_{s1}	12 → 9	0.08φ x 234 (Litz Wire)	4	Bifilar Winding
N_{s2}	10 → 13	0.08φ x 234 (Litz Wire)	4	Bifilar Winding

Table 3.

	Pins	Specifications	Remark
Primary−Side Inductance (L_p)	2−6	550 μH ±10%	100 kHz, 1 V
Primary−Side Effective Leakage (L_r)	2−6	110 μH ±10%	Short one of the Secondary Windings

For more detailed information regarding the transformer, visit http://www.santronics−usa.com/documents.html or contact sales@santronics−usa.com or +1−408−734−1878 (Sunnyvale, California USA).

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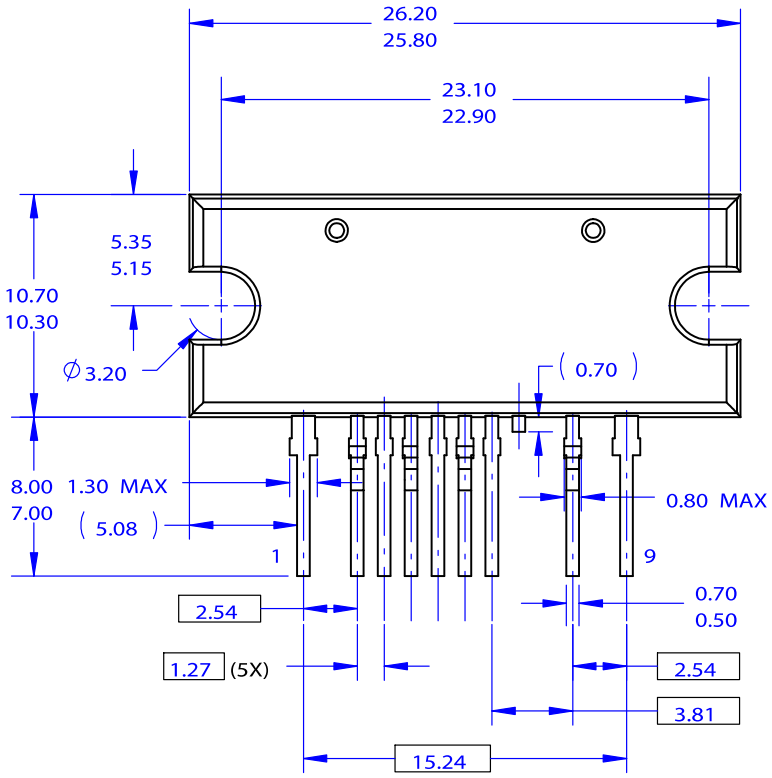
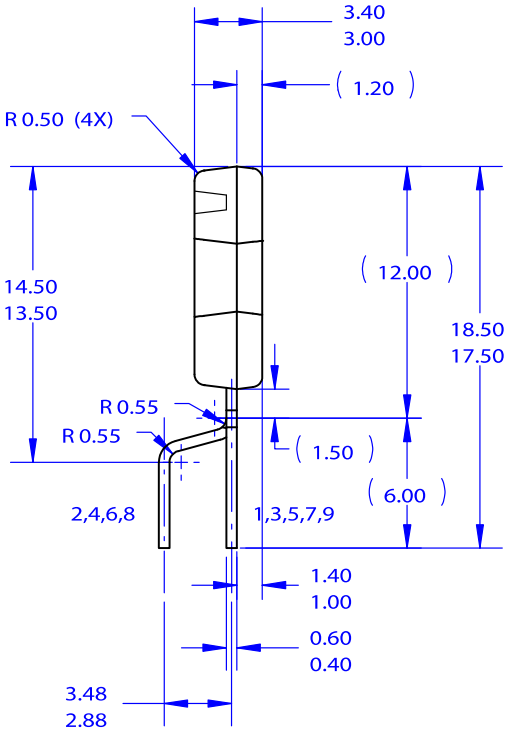
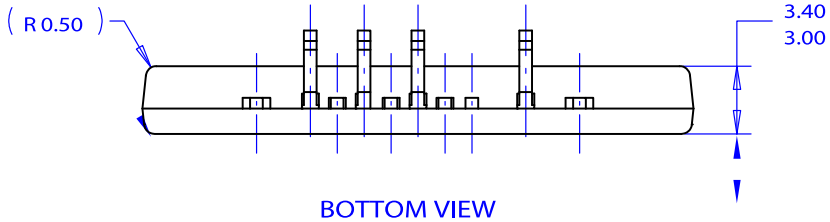


FRONT VIEW



RIGHT SIDE VIEW



BOTTOM VIEW

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