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April 2009

FSQ0765RQ
Green-Mode Fairchild Power Switch (FPS™) for Quasi-Resonant Operation - Low EMI and High Efficiency

Features

- Optimized for Quasi-Resonant Converter (QRC)
- Low EMI through Variable Frequency Control and AVS (Alternating Valley Switching)
- High-Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Simple Scheme for Sync Voltage Detection
- Pulse-by-Pulse Current Limit
- Various Protection functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output Short Protection (OSP)
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Startup Circuit
- Internal High-Voltage Sense FET (650V)
- Built-in Soft-Start (17.5ms)

Applications

- Power Supply for LCD TV and Monitor, VCR, SVR, STB, and DVD & DVD Recorder
- Adapter

Related Resources

Visit http://www.fairchildsemi.com/apnotes/ for:

- *AN-4134: Design Guidelines for Offline Forward Converters Using Fairchild Power Switch (FPS™)*
- *AN-4137: Design Guidelines for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*
- *AN-4140: Transformer Design Consideration for Offline Flyback Converters Using Fairchild Power Switch (FPS™)*
- *AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4145: Electromagnetic Compatibility for Power Converters*
- *AN-4147: Design Guidelines for RCD Snubber of Flyback*
- *AN-4148: Audible Noise Reduction Techniques for Fairchild Power Switch Fairchild Power Switch(FPS™) Applications*
- *AN-4150: Design Guidelines for Flyback Converters Using FSQ-Series Fairchild Power Switch (FPS™)*

Description

A Quasi-Resonant Converter (QRC) generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ-series is an integrated Pulse-Width Modulation (PWM) controller and SenseFET specifically designed for quasi-resonant operation and Alternating Valley Switching (AVS). The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for a loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSQ-series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for cost-effective designs of quasi-resonant switching flyback converters.

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Ordering Information

Product Number	PKG.[5]	Operating Temp.	Current Limit	$R_{DS(ON)}$ Max.	Maximum Output Power[1]				Replaces Devices
					230V_{AC}±15%[2]		85-265V_{AC}		
					Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]	
FSQ0765RQWDTU	TO-220F-6L	-25 to +85°C	3.5A	1.6Ω	80W	90W	48W	70W	FSCM0765R FSDM0765RB

Notes:

1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient.
5. For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html. Eco Status: RoHS.

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Application Diagram

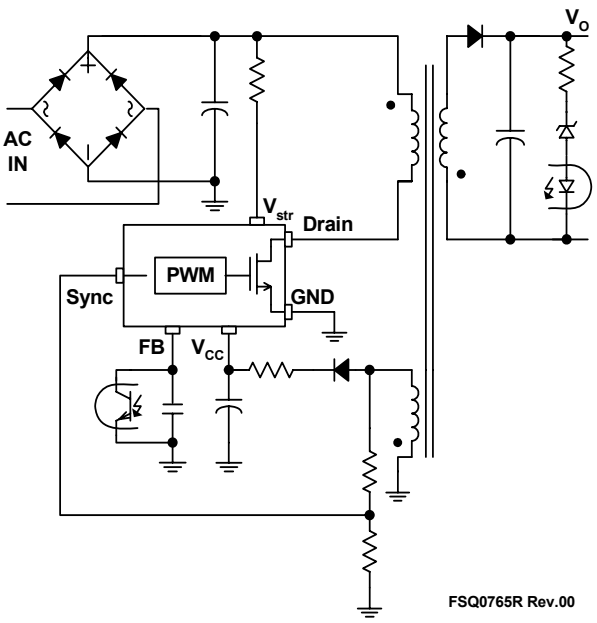

Figure 1. Typical Flyback Application

Internal Block Diagram

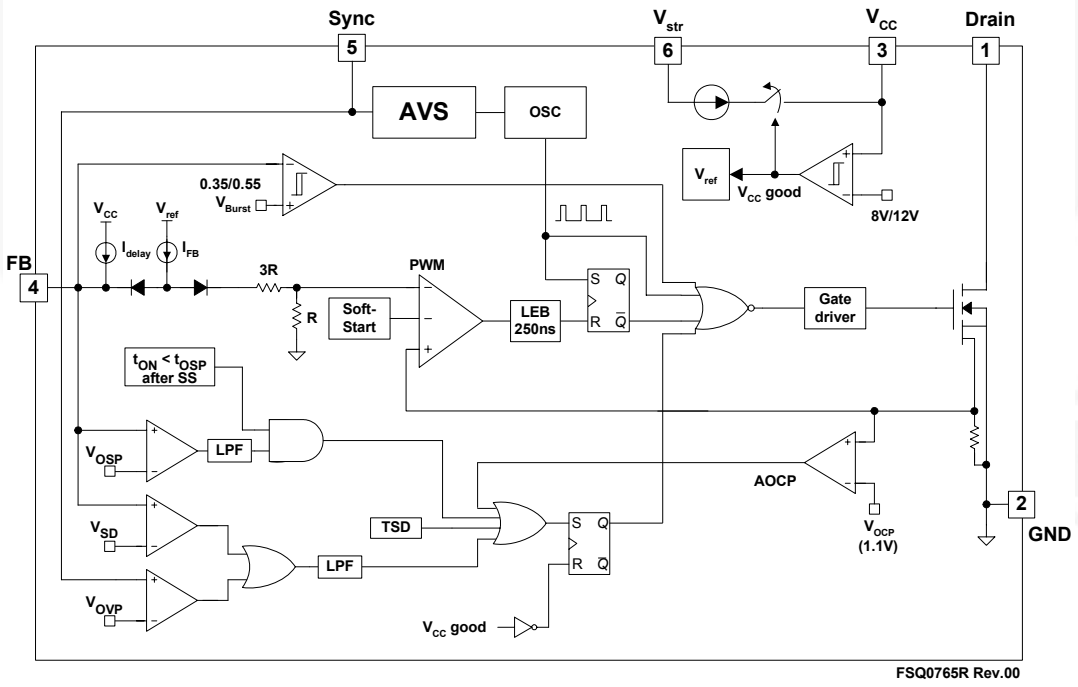

Figure 2. Internal Block Diagram

Pin Configuration

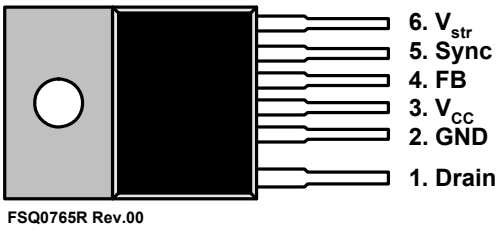

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.
2	GND	**Ground.** This pin is the control ground and the SenseFET source.
3	V_{CC}	**Power Supply.** This pin is the positive supply input. This pin provides internal operating current for both startup and steady-state operation.
4	FB	**Feedback.** This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the FPS.
5	Sync	**Sync.** This pin is internally connected to the sync-detect comparator for quasi-resonant switching. In normal quasi-resonant operation, the threshold of the sync comparator is 1.2V/1.0V.
6	V_{str}	**Startup.** This pin is connected directly, or through a resistor, to the high-voltage DC link. At start-up, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source is disabled. It is not recommended to connect V_{str} and Drain together.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C, unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{str}	V_{str} Pin Voltage		500		V
V_{DS}	Drain Pin Voltage		650		V
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		-0.3	13.0	V
V_{Sync}	Sync Pin Voltage		-0.3	13.0	V
I_{DM}	Drain Current Pulsed			14.4	A
I_D	Continuous Drain Current[6]	T_C = 25°C		3.6	A
		T_C = 100°C		2.28	
E_{AS}	Single Pulsed Avalanche Energy[7]			570	mJ
P_D	Total Power Dissipation(Tc=25°C)			45	W
T_J	Operating Junction Temperature		Internally limited		°C
T_A	Operating Ambient Temperature		-25	+85	°C
T_{STG}	Storage Temperature		-55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model	2		kV
		Charged Device Model	2		

Notes:

6. Repetitive rating: Pulse width limited by maximum junction temperature.
7. L=81mH, starting T_J=25°C.

Thermal Impedance

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance[8]	50	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance[9]	2.8	°C/W

Notes:

8. Free standing with no heat-sink under natural convection.
9. Infinite cooling condition - refer to the SEMI G30-88.

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Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SENSEFET SECTION							
BV_{DSS}	Drain Source Breakdown Voltage		V_{CC} = 0V, I_D = 100μA	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 520V, V_{GS} = 0V			300	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance		T_J = 25°C, I_D = 1.8A		1.3	1.6	Ω
C_{OSS}	Output Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		125		pF
$t_{d(on)}$	Turn-On Delay Time		V_{DD} = 325V, I_D = 6.5A		27		ns
t_r	Rise Time				102		ns
$t_{d(off)}$	Turn-Off Delay Time				63		ns
t_f	Fall Time				65		ns
CONTROL SECTION							
$t_{ON.MAX}$	Maximum On Time		T_J = 25°C	8.8	10.0	11.2	μs
t_B	Blanking Time		T_J = 25°C, V_{sync} = 5V	13.5	15.0	16.5	μs
t_W	Detection Time Window		T_J = 25°C, V_{sync} = 0V		6.0		μs
f_S	Initial Switching Frequency			59.6	66.7	75.8	kHz
Δf_S	Switching Frequency Variation[11]		-25°C < T_J < 85°C		±5	±10	%
t_{AVS}	AVS Triggering Threshold[11]	On Time	at V_{IN} = 240V_{DC}, Lm = 360μH (AVS triggered when V_{AVS}>spec & t_{AVS}<spec.)		4.0		μs
V_{AVS}		Feedback Voltage			1.2		V
t_{SW}	Switching Time Variance by AVS[11]		Sync = 500kHz sine input V_{FB} = 1.2V, t_{ON} = 4.0μs	13.5		20.5	μs
I_{FB}	Feedback Source Current		V_{FB} = 0V	700	900	1100	μA
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0V			0	%
V_{START}	UVLO Threshold Voltage			11	12	13	V
V_{STOP}			After turn-on	7	8	9	V
$t_{S/S}$	Internal Soft-Start Time		With free-running frequency		17.5		ms
BURST-MODE SECTION							
V_{BURH}	Burst-Mode Voltages		T_J = 25°C, t_{PD} = 200ns[10]	0.45	0.55	0.65	V
V_{BURL}				0.25	0.35	0.45	V
Hysteresis					200		mV

Note:

10. Propagation delay in the control IC.

Continued on the following page...

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Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
PROTECTION SECTION							
I_{LIMIT}	Peak Current Limit		T_J = 25°C, di/dt = 460mA/µs	3.08	3.50	3.92	A
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 15V	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5V	4	5	6	µA
t_{LEB}	Leading-Edge Blanking Time(11)				250		ns
t_{OSP}	Output Short Protection(11)	Threshold Time	T_J = 25°C OSP triggered when t_{ON}<t_{OSP} , V_{FB}>V_{OSP} & lasts longer than t_{OSP_FB}		1.2	1.4	µs
V_{OSP}		Threshold Feedback Voltage		1.8	2.0		V
t_{OSP_FB}		Feedback Blanking Time		2.0	2.5	3.0	µs
T_{SD}	Thermal Shutdown(11)	Shutdown Temperature		125	140	155	°C
Hys		Hysteresis			60		
SYNC SECTION							
V_{SH1}	Sync Threshold Voltage 1		V_{CC} = 15V, V_{FB} = 2V	1.0	1.2	1.4	V
V_{SL1}				0.8	1.0	1.2	
t_{sync}	Sync Delay Time(11)(12)				230		ns
V_{SH2}	Sync Threshold Voltage 2		V_{CC} = 15V, V_{FB} = 2V	4.3	4.7	5.1	V
V_{SL2}				4.0	4.4	4.8	
V_{CLAMP}	Low Clamp Voltage		I_{SYNC_MAX} = 800µA I_{SYNC_MIN} = 50µA	0.0	0.4	0.8	V
V_{OVP}	Over-Voltage Protection	Threshold Voltage	V_{CC} = 15V, V_{FB}=2V	7.4	8.0	8.6	V
t_{OVP}		Blanking Time(11)		1.0	1.7	2.4	µs
TOTAL DEVICE SECTION							
I_{OP}	Operating Supply Current (Control Part Only)		V_{CC} = 13V, V_{FB}=0V	1	3	5	mA
I_{START}	Start Current		V_{CC} = 10V (before V_{CC} reaches V_{START})	350	450	550	µA
I_{CH}	Startup Charging Current		V_{CC} = 0V, V_{STR} = minimum 50V	0.65	0.85	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage				26		V

Notes:

11. Guaranteed by design, but not tested in production.
12. Includes gate turn-on time.

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Comparison Between FSDM0x65RNB and FSQ-Series

Function	FSDM0x65RE	FSQ-Series	FSQ-Series Advantages
Operation Method	Constant Frequency PWM	Quasi-Resonant Operation	■ Improved efficiency by valley switching ■ Reduced EMI noise ■ Reduced components to detect valley point
EMI Reduction	Frequency Modulation	Reduce EMI Noise	■ Valley switching ■ Inherent frequency modulation ■ Alternate valley switching
Hybrid Control		CCM or AVS Based on Load and Input Condition	■ Improves efficiency by introducing hybrid control
Burst-Mode Operation	Burst-Mode Operation	Advanced Burst-Mode Operation	■ Improved standby power by AVS in burst-mode
Strong Protections	OLP, OVP	OLP, OVP, AOCP, OSP	■ Improved reliability through precise AOCP ■ Improved reliability through precise OSP
TSD	145°C without Hysteresis	140°C with 60°C Hysteresis	■ Stable and reliable TSD operation ■ Converter temperature range

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Typical Performance Characteristics

These characteristic graphs are normalized at T_A= 25°C.

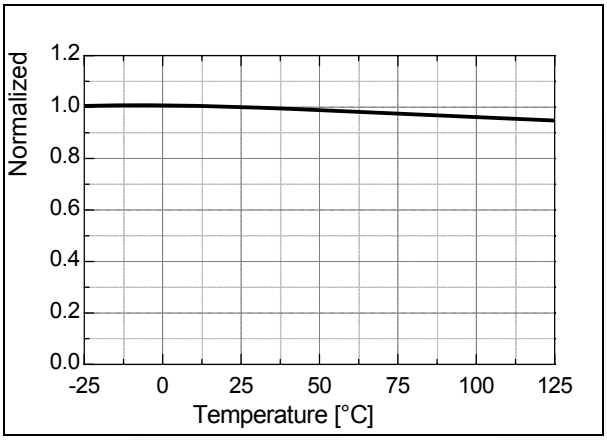

Figure 4. Operating Supply Current (I_{OP}) vs. T_A

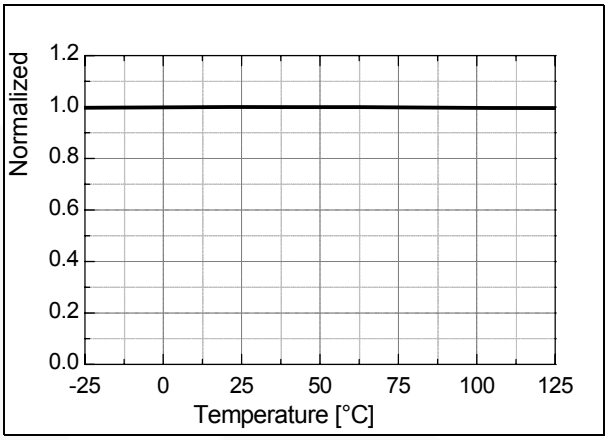

Figure 5. UVLO Start Threshold Voltage (V_{START}) vs. T_A

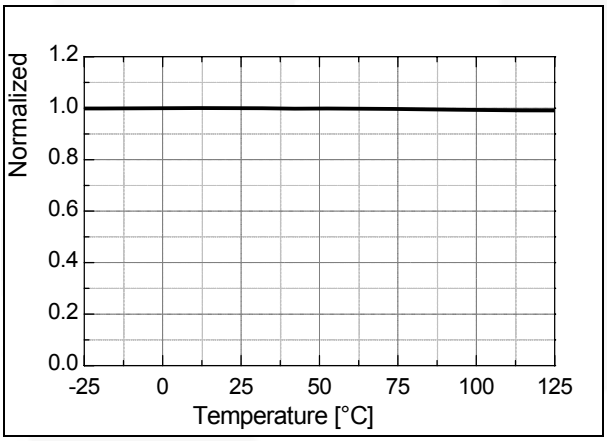

Figure 6. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

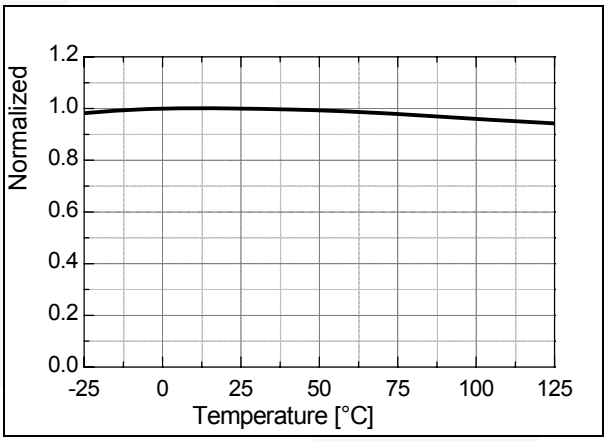

Figure 7. Startup Charging Current (I_{CH}) vs. T_A

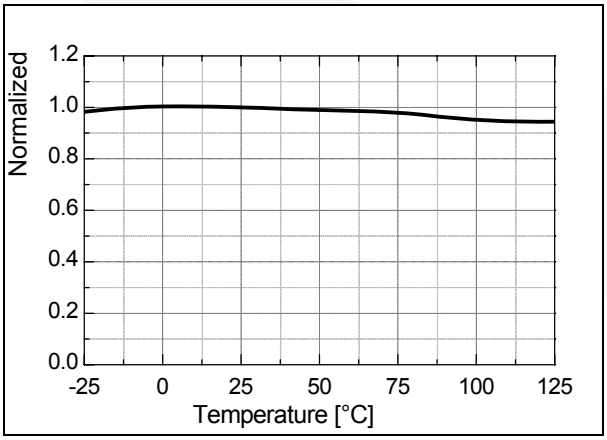

Figure 8. Initial Switching Frequency (f_{SW}) vs. T_A

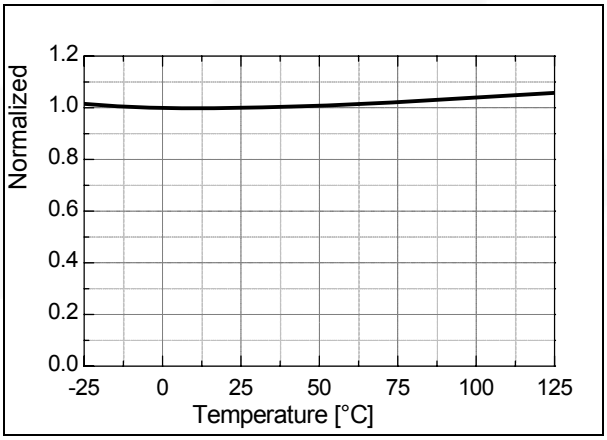

Figure 9. Maximum On Time ($t_{ON.MAX}$) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

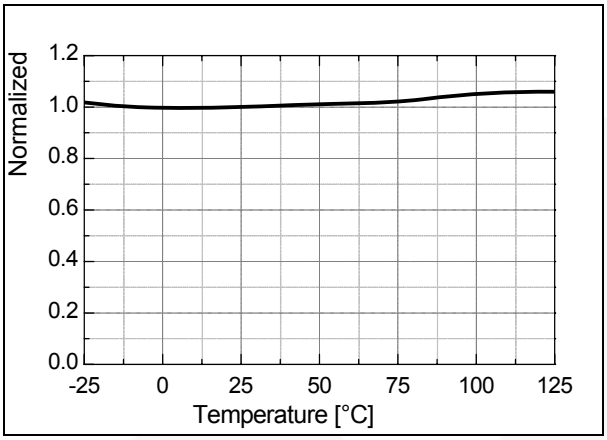

Figure 10. Blanking Time (t_B) vs. T_A

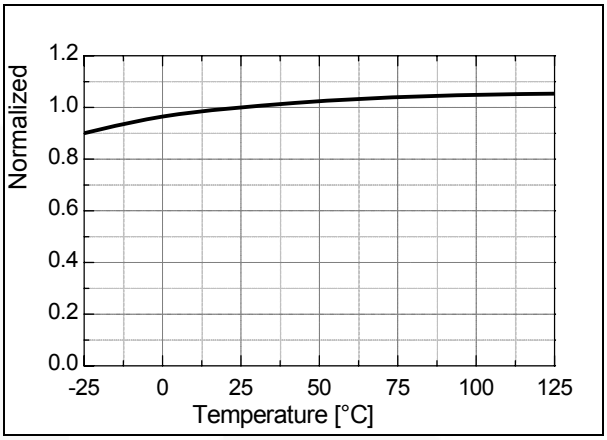

Figure 11. Feedback Source Current (I_{FB}) vs. T_A

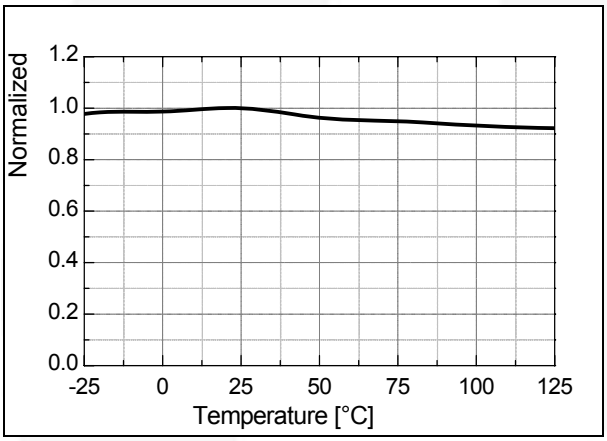

Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

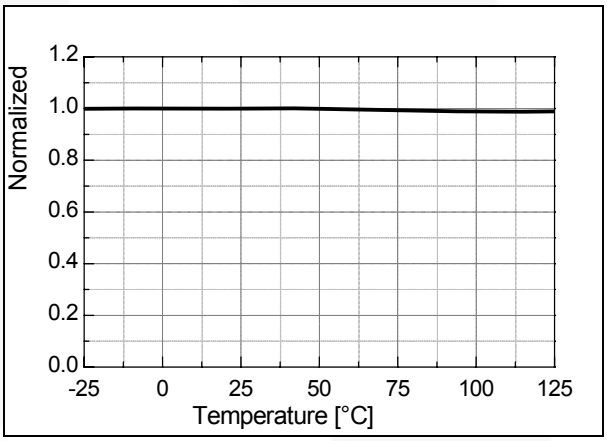

Figure 13. Burst-Mode High Threshold Voltage (V_{burh}) vs. T_A

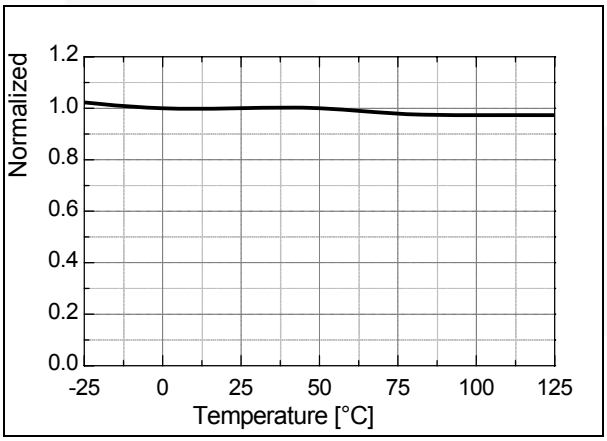

Figure 14. Burst-Mode Low Threshold Voltage (V_{burl}) vs. T_A

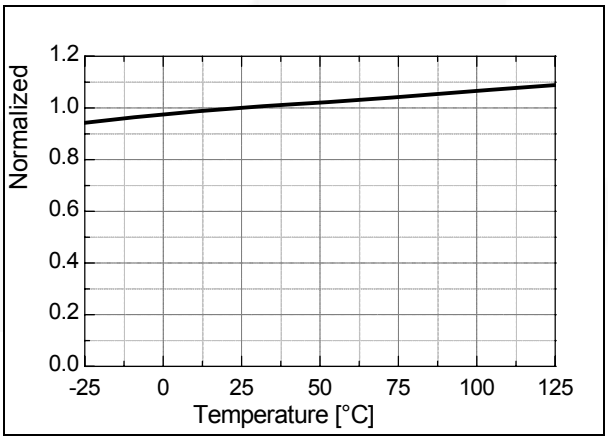

Figure 15. Peak Current Limit (I_{LIM}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

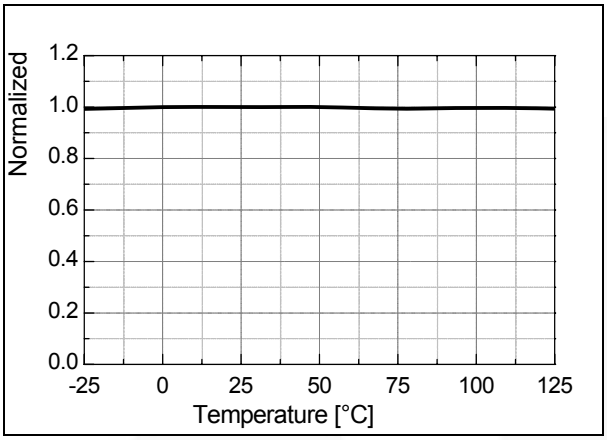

Figure 16. Sync High Threshold Voltage 1 (V_{SH1}) vs. T_A

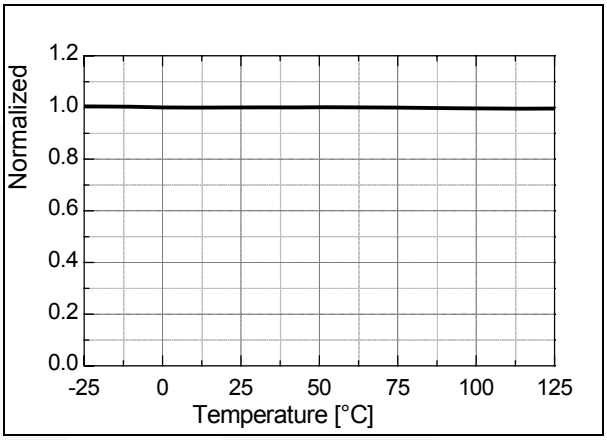

Figure 17. Sync Low Threshold Voltage 1 (V_{SL1}) vs. T_A

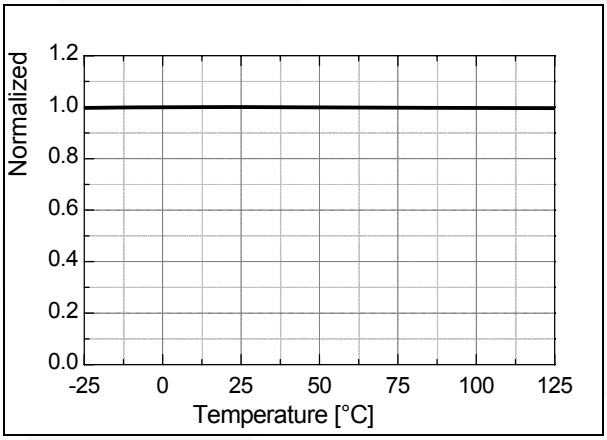

Figure 18. Shutdown Feedback Voltage (V_{SD}) vs. T_A

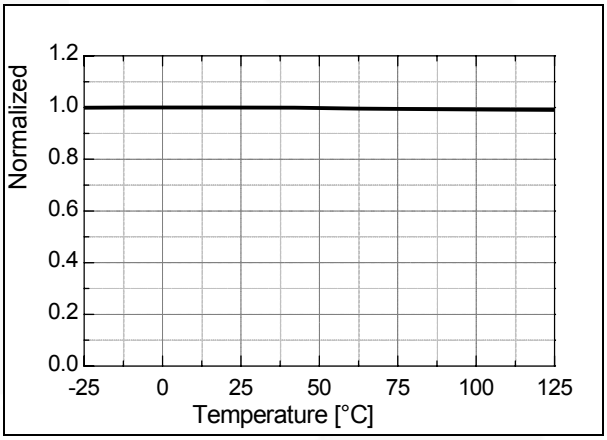

Figure 19. Over-Voltage Protection (V_{OV}) vs. T_A

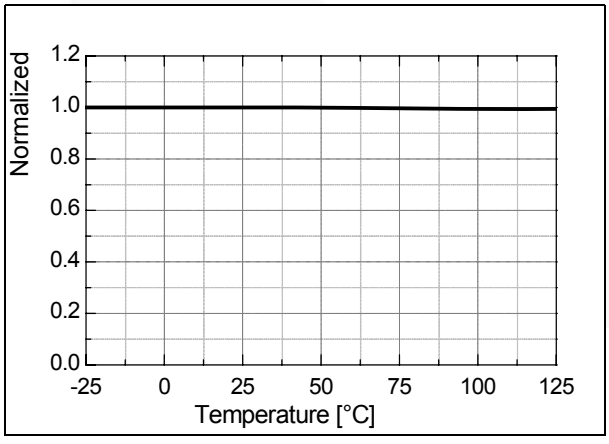

Figure 20. Sync High Threshold Voltage 2 (V_{SH2}) vs. T_A

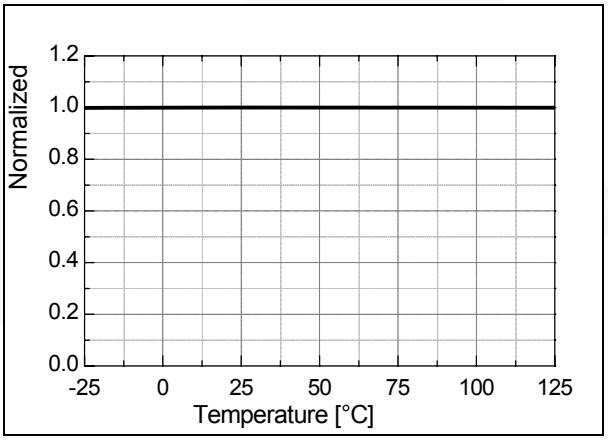

Figure 21. Sync Low Threshold Voltage 2 (V_{SL2}) vs. T_A

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Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 22. When V_{CC} reaches 12V, the FPS™ begins switching and the internal high-voltage current source is disabled. The FPS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

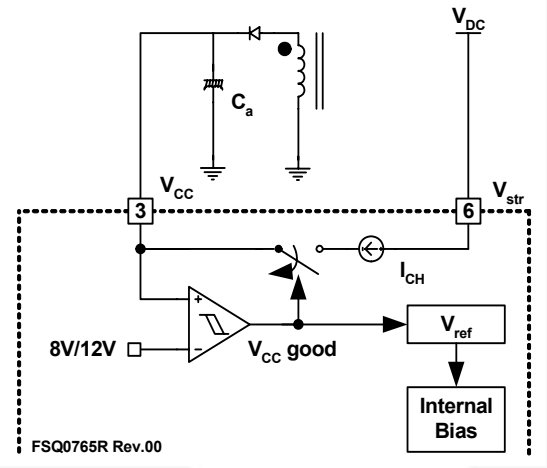

Figure 22. Startup Circuit

2. Feedback Control: FPS employs current-mode control, as shown in Figure 23. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 23. Assuming that the 0.9mA current source flows only through the internal resistor (3R + R = 2.8k), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{FB}*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current-mode PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

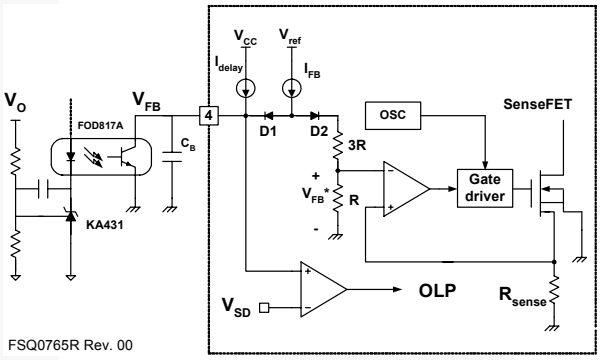

Figure 23. Pulse-Width-Modulation (PWM) Circuit

3. Synchronization: The FSQ-series employs a quasi-resonant switching technique to minimize the switching noise and loss. The basic waveforms of the quasi-resonant converter are shown in Figure 24. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, which is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 24.

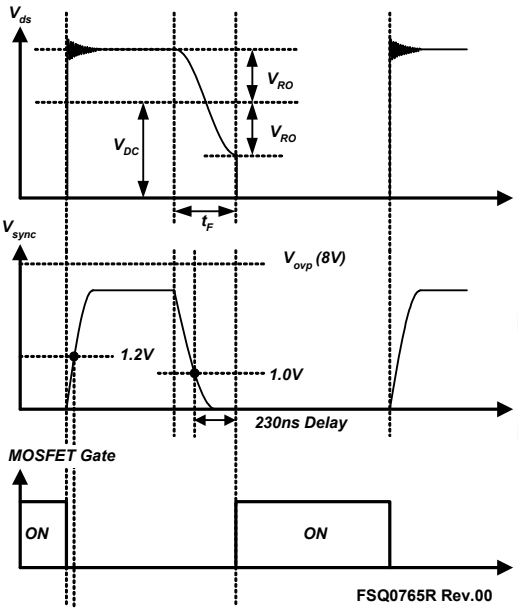

Figure 24. Quasi-Resonant Switching Waveforms

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The switching frequency is the combination of blank time (t_B) and detection time window (t_W). In case of a heavy load, the sync voltage remains flat after t_B and waits for valley detection during t_W. This leads to a low switching frequency not suitable for heavy loads. To correct this drawback, additional timing is used. The timing conditions are described in Figures 25, 26, and 27. When the V_{sync} remains flat higher than 4.4V at the end of t_B that is t_X, the next switching cycle starts after internal delay time from t_X. In the second case, the next switching occurs on the valley when the V_{sync} goes below 4.4V within t_B. Once V_{sync} detects the first valley within t_B, the other switching cycle follows classical QRC operation.

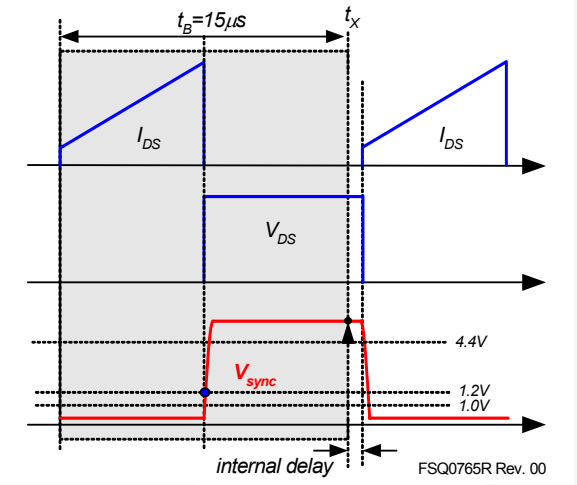

Figure 25. V_{sync} > 4.4V at t_X

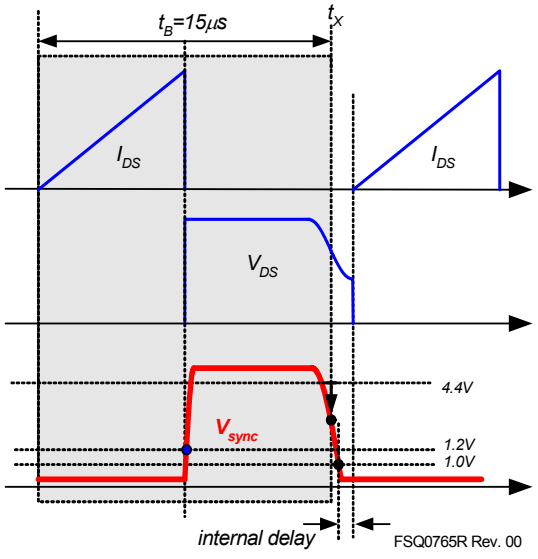

Figure 26. V_{sync} < 4.4V at t_X

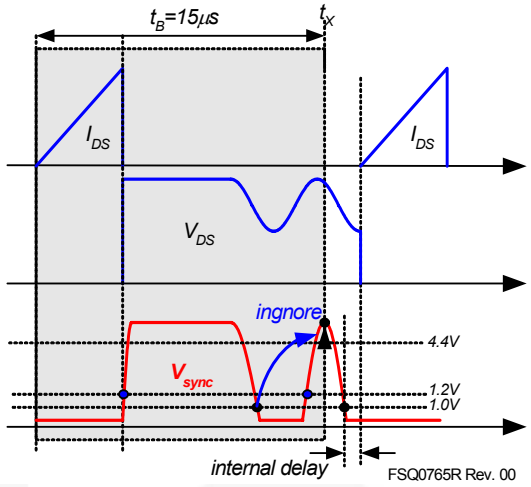

Figure 27. After V_{sync} Finds First Valley

4. Protection Circuits: The FSQ-series has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 8V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When the V_{CC} reaches the start voltage of 12V, normal operation resumes. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

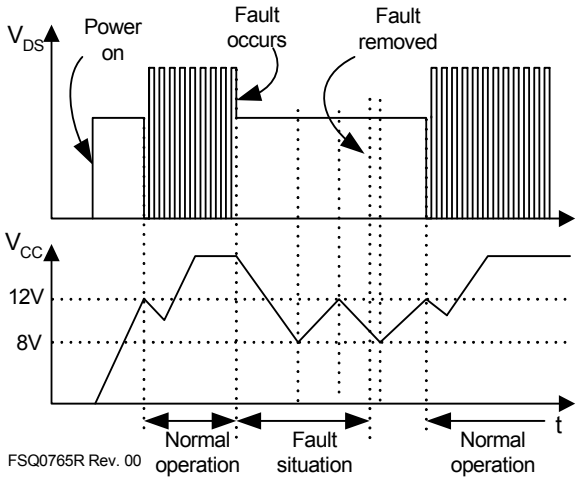

Figure 28. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.5V, D1 is blocked and the 5μA current source starts to charge CB slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 6V, when the switching operation is terminated, as shown in Figure 29. The delay time for shutdown is the time required to charge C_{FB} from 2.5V to 6V with 5μA. A 20 ~ 50ms delay time is typical for most applications.

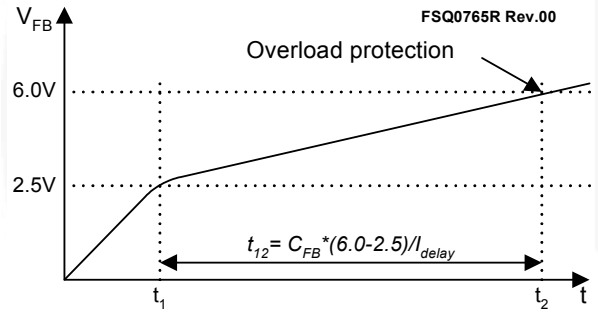

Figure 29. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FSQ-series has overload protection, it is not enough to protect the FSQ-series in that abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FSQ-series has an internal AOCP circuit shown in Figure 30. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

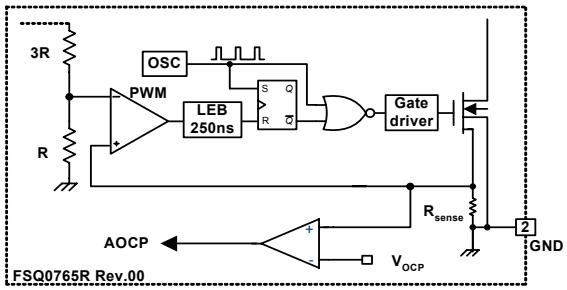

Figure 30. Abnormal Over-Current Protection

4.3 Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Such a steep current brings high voltage stress on the drain of SenseFET when turned off. To protect the device from such an abnormal condition, OSP is included in the FSQ-series. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2V and the SenseFET turn-on time is lower than 1.2μs, the FPS recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{start} again. An abnormal condition output short is shown in Figure 31.

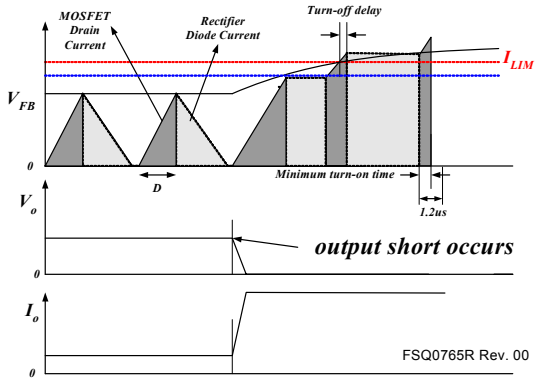

Figure 31. Output Short Waveforms

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ-series

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uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 8V, an OVP is triggered, shutting down the SMPS. To avoid undesired triggering of OVP during normal operation, there are two points to be considered, which are depicted in Figure 32. One is at the peak voltage of the sync signal should be designed below 6V and the other is that the spike of the sync pin should be as low as possible; not to get longer than t_{OVP} by decreasing the leakage inductance shown at V_{CC} winding coil.

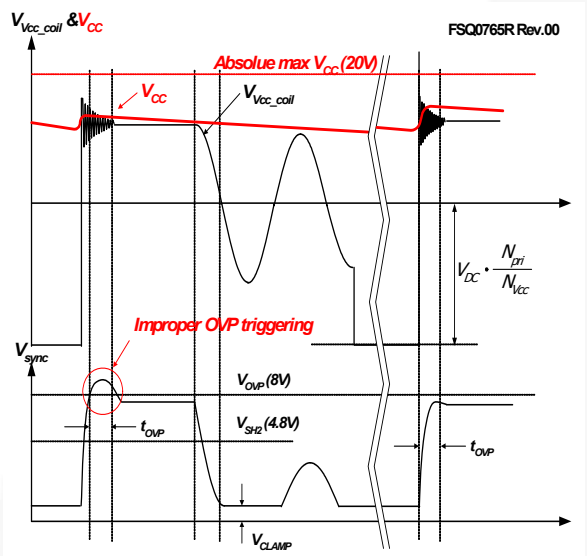

Figure 32. OVP Triggering

4.5 Thermal Shutdown with Hysteresis (TSD): The SenseFET and the control IC are built in one package. This allows the control IC to detect abnormally high temperature of the SenseFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers IC shutdown. The IC recovers its operation when the junction temperature decreases 60°C from TSD temperature and V_{CC} reaches startup voltage (V_{start}).

5. Soft-Start: The FPS has an internal soft-start circuit that increases PWM comparator inverting input voltage with the SenseFET current slowly after it starts up. The typical soft-start time is 17.5ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This mode helps prevent transformer saturation and reduces stress on the secondary diode during startup.

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 33, the device automatically enters burst-mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

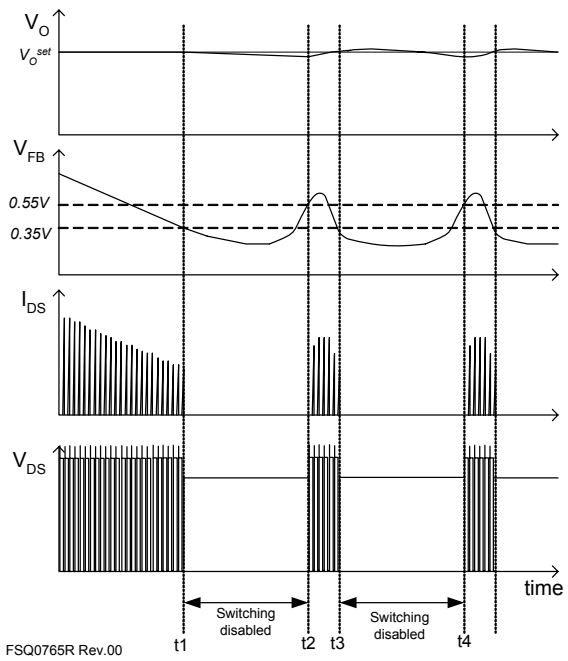

Figure 33. Waveforms of Burst Operation

7. Switching Frequency Limit: To minimize switching loss and Electromagnetic Interference (EMI), the MOSFET turns on when the drain voltage reaches its minimum value in quasi-resonant operation. However, this causes switching frequency to increases at light load conditions. As the load decreases or input voltage increases, the peak drain current diminishes and the switching frequency increases. This results in severe switching losses at light-load condition, as well as intermittent switching and audible noise. These problems create limitations for the quasi-resonant converter topology in a wide range of applications.

To overcome these problems, FSQ-series employs a frequency-limit function, as shown in Figures 34 and 35. Once the SenseFET is turned on, the next turn-on is prohibited during the blanking time (t_B). After the blanking time, the controller finds the valley within the detection time window (t_W) and turns on the MOSFET, as shown in Figures 34 and Figure 35 (Cases A, B, and C).

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If no valley is found during t_W, the internal SenseFET is forced to turn on at the end of t_W (Case D). Therefore, the devices have a minimum switching frequency of 48kHz and a maximum switching frequency of 67kHz.

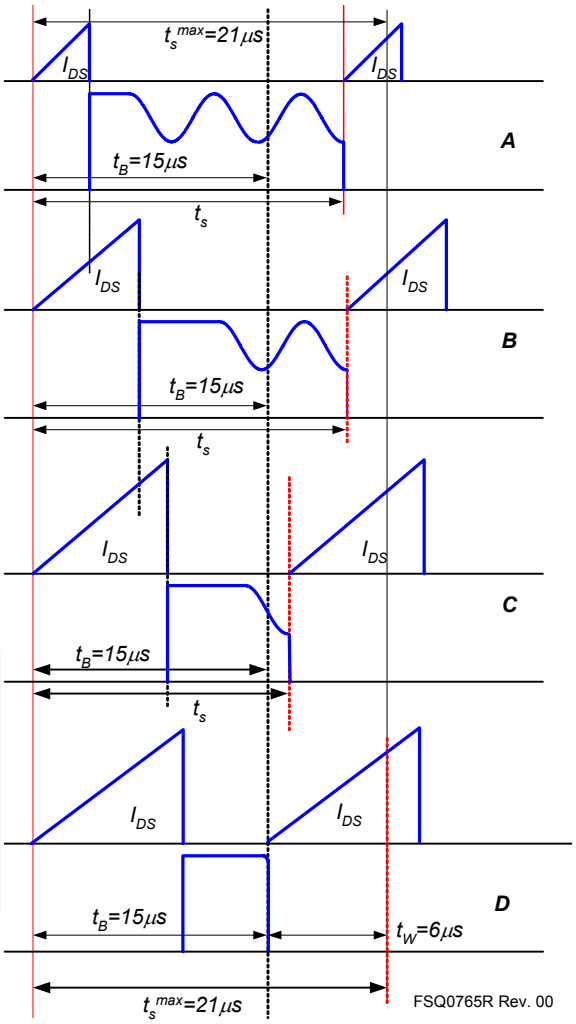

Figure 34. QRC Operation with Limited Frequency

8. AVS (Alternating Valley Switching): Due to the quasi-resonant operation with limited frequency, the switching frequency varies depending on input voltage, load transition, and so on. At high input voltage, the switching on time is relatively small compared to low input voltage. The input voltage variance is small and the switching frequency modulation width becomes small. To improve the EMI performance, AVS is enabled when input voltage is high and the switching on time is small.

Internally, quasi-resonant operation is divided into two categories; one is first-valley switching and the other is second-valley switching after blanking time. In AVS, two successive occurrences of first-valley switching and the other two successive occurrences of second-valley switching is alternatively selected to maximize frequency modulation. As depicted in Figure 35, the switching frequency hops when the input voltage is high. The internal timing diagram of AVS is described in Figure 36.

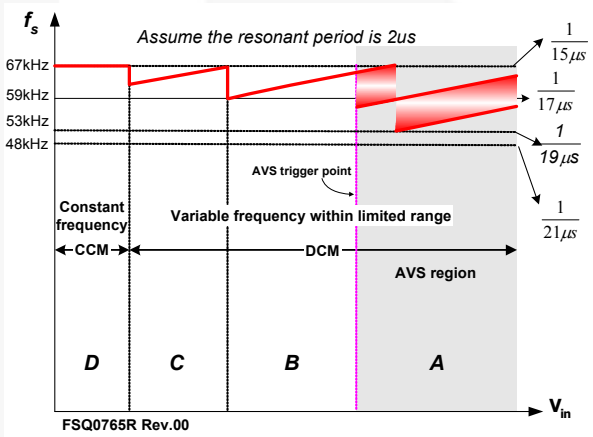

Figure 35. Switching Frequency Range

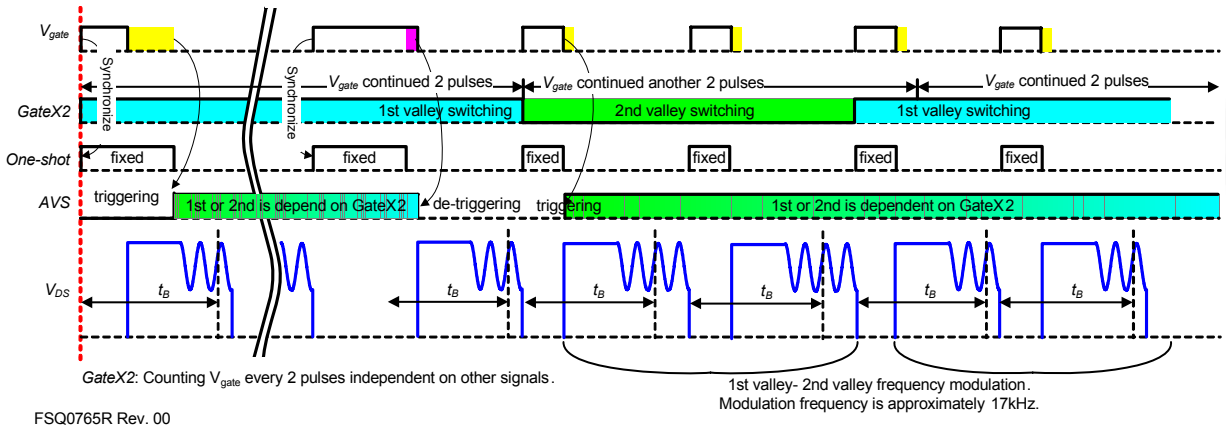

Figure 36. Alternating Valley Switching (AVS)

PCB Layout Guide

Due to the combined scheme, FPS shows better noise immunity than conventional PWM controller and MOSFET discrete solution. Further more are internal drain current sense eliminates the possibility of noise generation caused by a sensing resistor. There are some recommendations for PCB layout to enhance noise immunity and suppress natural noise inevitable in power-handling components.

There are typically two grounds in the conventional SMPS: power ground and signal ground. The power ground is the ground for primary input voltage and power, while the signal ground is ground for PWM controller. In FPS, those two grounds share the same pin, GND. Normally the separate grounds do not share the same trace and meet only at one point, the GND pin. More, wider patterns for both grounds are good for large currents by decreasing resistance.

Capacitors at the VCC and FB pins should be as close as possible to the corresponding pins to avoid noise from the switching device. Sometimes Mylar® or ceramic capacitors with electrolytic for V_{CC} are better for smooth operation. The ground of these capacitors needs to connect to the signal ground (not power ground).

The cathode of the snubber diode should be close to the drain pin to minimize stray inductance. The Y-capacitor between primary and secondary should be directly connected to the power ground of DC link to maximize surge immunity.

Because the voltage range of feedback and sync line is small, it is affected by the noise of the drain pin. Those traces should not draw across or close to the drain line.

When the heat sink is connected to the ground, it should be connected to the power ground. If possible, avoid using jumper wires for power ground and drain.

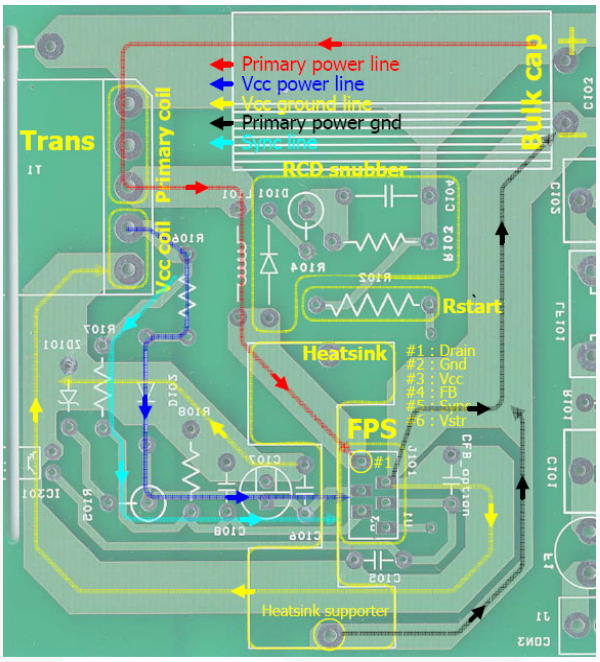

Figure 37. Recommended PCB Layout

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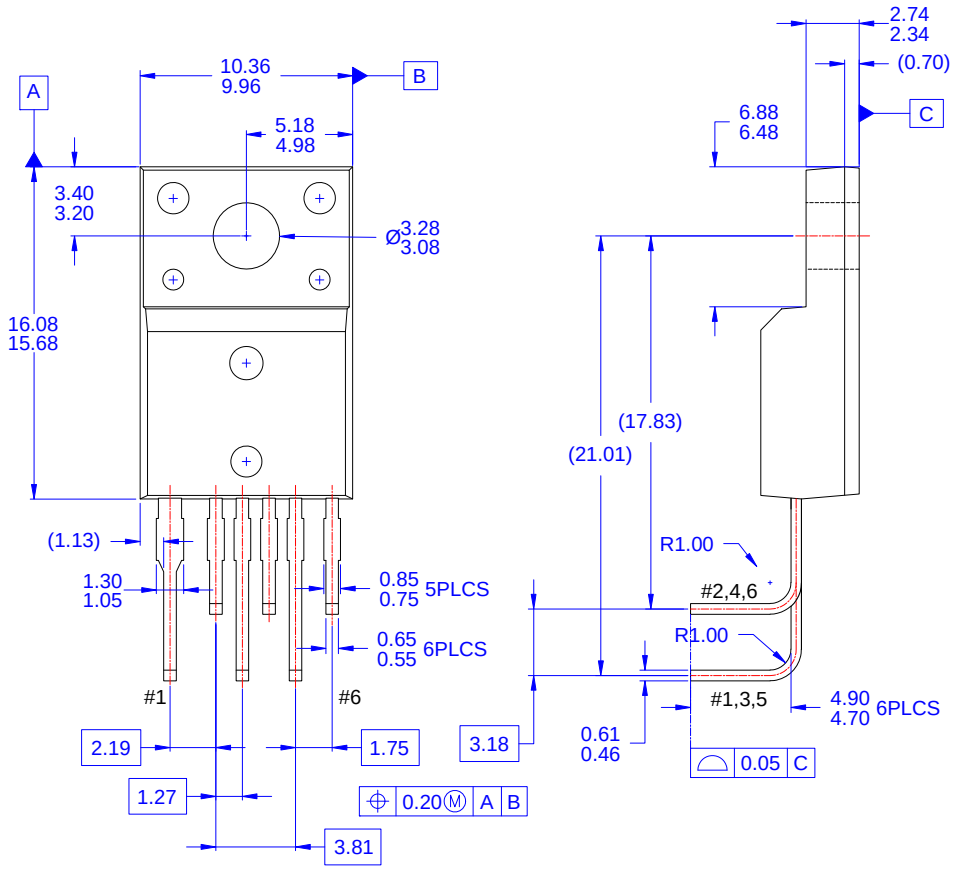

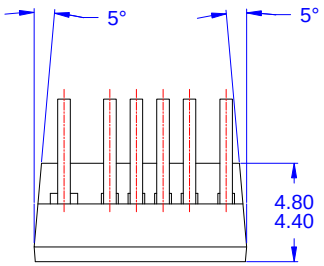

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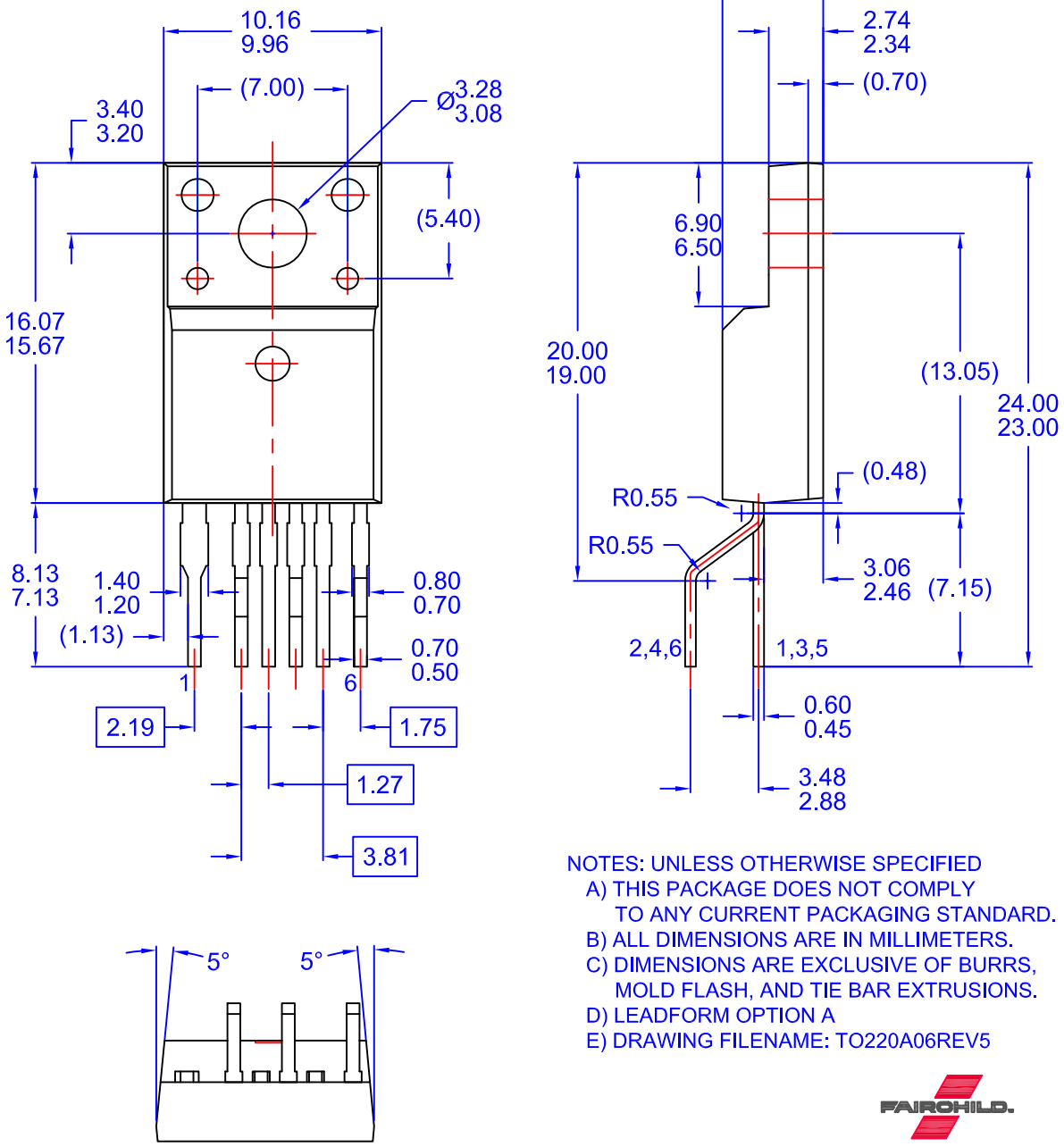

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