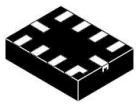
Low-Voltage, Dual-Supply, 2-Bit, Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-State Outputs

FXL2T245



UQFN10 (MICROPAK™), 1.6 x 2.1, 0.5P
CASE 523AZ

MARKING DIAGRAM

XC = Specific Device Code
&K = 2-Digits Lot Run Traceability Code
&2 = 2-Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

General Description

The FXL2T245 is a configurable, dual-voltage-supply translator designed for uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

The device remains in 3-state until both V_{CC}s reach active levels, allowing either V_{CC} to be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The Transmit / Receive (T/$\overline{R}$) input determines the direction of data flow through the device. The $\overline{OE}$ input, when HIGH, disables both the A and B ports by placing them in a 3-state condition. The FXL2T245 is designed so control pins T/$\overline{R}$ and $\overline{OE}$ are supplied by V_{CCA}.

Features

- Bi-Directional Interface between any 2 Levels from 1.1 V to 3.6 V
- Fully Configurable, Inputs Track V_{CC} Level
- Non-Preferential Power-up Sequencing; either V_{CC} maybe Powered-up First
- Outputs Remain in 3-State until Active V_{CC} Level is Reached
- Outputs Switch to 3-State if either V_{CC} is at GND
- Power-Off Protection
- Control Inputs (T/R, OE) Levels are Referenced to V_{CCA} Voltage
- Packaged in 10-Lead MicroPak (1.6 mm x 2.1 mm) Package
- ESD Protection Exceeds:
  - 4 kV HBM ESD JESD22−A114 & Mil Std 883e 3015.7)
  - 8 kV HBM I/O to GND ESD (per JESD22−A114 & Mil Std 883e 3015.7)
  - 1 kV CDM ESD (per ESD STM 5.3)
  - 200 V MM ESD (per JESD22−A115 & ESD STM5.2)

PIN CONFIGURATION

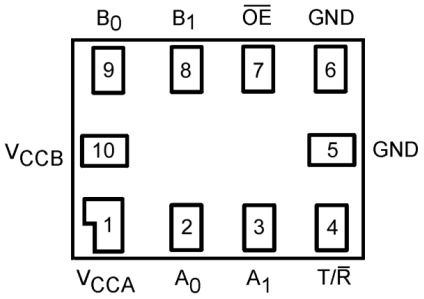


Figure 1. Pin Assignments

PIN DESCRIPTION

Pin #	Pin Name	Description
1	V_{CCA}	Side A Power Supply
2	A_0	Side A Inputs or 3-State Outputs
3	A_1	Side A Inputs or 3-State Outputs
4	T/$\overline{R}$	Transmit/Receive Input
5, 6	GND	Ground
7	$\overline{O/E}$	Output Enable Input
8	B_1	Side B Inputs or 3-State Outputs
9	B_0	Side B Inputs or 3-State Outputs
10	V_{CCB}	Side B Power Supply

TRUTH TABLE

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
LOW	LOW	Bus B Data to Bus A
LOW	HIGH	Bus A Data to Bus B

1. LOW = low voltage level.
2. HIGH = high voltage level.

FUNCTIONAL DESCRIPTION

Power-Up / Power-Down Sequencing

Due to the chip design, the FXL2T245 translator offers the advantage of either V_{CC} being powered up first. When either V_{CC} is at 0 V, outputs are in a high-impedance state. The control inputs (T/$\overline{R}$ and $\overline{OE}$) are designed to track the V_{CCA} supply. A pull-up resistor tying $\overline{OE}$ to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the $\overline{OE}$ driver.

The recommended power-up sequence is:

1. Apply power to either V_{CC}.
2. Apply power to the T/$\overline{R}$ input (logic HIGH for A-to-B operation; logic LOW for B-to-A operation) and to the respective data inputs (A port or B port). This may occur at the same time as step 1.
3. Apply power to the other V_{CC}.
4. Drive the $\overline{OE}$ input LOW to enable the device.

The recommended power−down sequence is:

1. Drive $\overline{OE}$ input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from the other V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	Supply Voltage			−0.5	4.6	V
V_{CCB}				−0.5	4.6	
V_I	DC Input Voltage	I/O Port A		−0.5	4.6	V
		I/O Port B		−0.5	4.6	
		Control Inputs (T/$\overline{R}$, $\overline{OE}$)		−0.5	4.6	
V_O	Output Voltage (Note 3)	Output 3-State		−0.5	4.6	V
		Output Active (An)		−0.5 to V_{CCA}	0.5	
		Output Active (Bn)		−0.5 to V_{CCB}	0.5	
I_{IK}	DC Input Diode Current	V_I < 0 V		−	−50	mA
I_{OK}	DC Output Diode Current	V_O < 0 V		−	−50	mA
		V_O > V_{CC}		−	+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current			−	±50	mA
I_{CC}	DC VCC or Ground Current per Supply Pin			−	±100	mA
T_{STG}	Storage Temperature Range			−65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114, Mil Std 883e 3015.7	All Pins	−	4	kV
			I/O to GND	−	8	
		Charged Device Model, JESD22−C101, STM 5.3		−	1	
		Machine Model, JESD22−A115, STM 5.2		−	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. I_O Absolute Maximum Rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	Power Supply	Operating V_{CCA} or V_{CCB}		1.1	3.6	V
V_I	Input Voltage	Port A		0	3.6	V
		Port B		0	3.6	
		Control Inputs (T/$\overline{R}$, $\overline{OE}$)		0	V_{CCA}	
I_{OH}/I_{OL}	Output Current	V_{CC}	3.0 V to 3.6 V	−	±24	mA
			2.3 V to 2.7 V	−	±18	
			1.65 V to 1.95 V	−	±6	
			1.40 V to 1.65 V	−	±2	
			1.1 V to 1.4 V	−	±0.5	
T_A	Operating Temperature, Free Air			−40	+85	°C
$\Delta V/\Delta t$	Minimum Input Edge Rate	$V_{CCA/B}$ = 1.1 V to 3.6 V		−	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. All unused inputs and I/O pins must be held at V_{CCI} or GND.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CCO} (V)	V_{CCI} (V)	Min	Max	Unit
V_{IH}	HIGH Level Input (Note 5)	Data Inputs A_n, B_n	1.10 to 3.60	2.70 to 3.60	2.00	−	V
				2.30 to 2.70	1.60	−	
				1.65 to 2.30	0.65 x V_{CCI}	−	
				1.40 to 1.65	0.65 x V_{CCI}	−	
				1.10 to 1.40	0.90 x V_{CCI}	−	
		Control Pins /$\overline{OE}$, T/$\overline{R}$ (Referenced to V_{CCA})		2.70 to 3.60	2.00	−	
				2.30 to 2.70	1.60	−	
				1.65 to 2.30	0.65 x V_{CCA}	−	
				1.40 to 1.65	0.65 x V_{CCA}	−	
				1.10 to 1.40	0.90 x V_{CCA}	−	
V_{IL}	LOW Level Input (Note 5)	Data Inputs A_n, B_n	1.10 to 3.60	2.70 to 3.60	−	0.80	V
				2.30 to 2.70	−	0.70	
				1.65 to 2.30	−	0.35 x V_{CCI}	
				1.40 to 1.65	−	0.35 x V_{CCI}	
				1.10 to 1.40	−	0.10 x V_{CCI}	
		Control Pins /$\overline{OE}$, T/$\overline{R}$ (Referenced to V_{CCA})		2.70 to 3.60	−	0.80	
				2.30 to 2.70	−	0.70	
				1.65 to 2.30	−	0.35 x V_{CCI}	
				1.40 to 1.65	−	0.35 x V_{CCI}	
				1.10 to 1.40	−	0.10 x V_{CCI}	
V_{OH}	HIGH Level Output (Note 6)	I_{OH} = −100 μA	1.10 to 3.60	1.10 to 3.60	V_{CC0} − 0.20	−	V
		I_{OH} = −12 mA	2.70	2.70	2.20	−	
		I_{OH} = −18 mA	3.00	3.00	2.40	−	
		I_{OH} = −24 mA	3.00	3.00	2.20	−	
		I_{OH} = −6 mA	2.30	2.30	2.00	−	
		I_{OH} = −12 mA	2.30	2.30	1.80	−	
		I_{OH} = −18 mA	2.30	2.30	1.70	−	
		I_{OH} = −6 mA	1.65	1.65	1.25	−	
		I_{OH} = −2 mA	1.40	1.40	1.05	−	
		I_{OH} = −0.5 mA	1.10	1.10	0.75 x V_{CC0}	−	
V_{OL}	LOW Level Output (Note 6)	I_{OL} = 100 μA	1.10 to 3.60	1.10 to 3.60	−	0.20	V
		I_{OL} = 12 mA	2.70	2.70	−	0.40	
		I_{OL} = 18 mA	3.00	3.00	−	0.40	
		I_{OL} = 24 mA	3.00	3.00	−	0.55	
		I_{OL} = 12 mA	2.30	2.30	−	0.40	
		I_{OL} = 18 mA	2.30	2.30	−	0.60	
		I_{OL} = 6 mA	1.65	1.65	−	0.30	
		I_{OL} = 2 mA	1.40	1.40	−	0.35	
		I_{OL} = 0.5 mA	1.10	1.10	−	0.30 x V_{CC0}	
I_L	Input Leakage Current, Control Pins	V_I = V_{CCA} or GND	3.60	1.10 to 3.60	−	±1.0	μA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V_{CCO} (V)	V_{CCI} (V)	Min	Max	Unit
I_{OFF}	Power Off Leakage Current	A_n, V_I or V_O = 0 V to 3.6 V	3.60	0	−	±10	μA
		B_n, V_I or V_O = 0 V to 3.6 V	0	3.60	−	±10	
I_{OZ}	3-State Output Leakage ($0 \le V_O \le 3.6$ V, $V_I = V_{IH}$ or V_{IL})	A_n, B_n, /OE = V_{IH}	3.60	3.60	−	±10	μA
		B_n, /OE = Don't Care (Note 7)	3.60	0	−	±10	
		A_n, /OE = Don't Care (Note 7)	0	3.60	−	±10	
$I_{CCA/B}$	Quiescent Supply Current (Note 8)	$V_I = V_{CCI}$ or GND; I_O = 0	1.10 to 3.60	1.10 to 3.60	−	20	μA
I_{CCZ}			1.10 to 3.60	1.10 to 3.60	−	20	μA
I_{CCA}		$V_I = V_{CCA}$ or GND; I_O = 0	1.10 to 3.60	0	−	−10	μA
			0	1.10 to 3.60	−	10	
I_{CCB}		$V_I = V_{CCB}$ or GND; I_O = 0	0	1.10 to 3.60	−	−10	μA
			1.10 to 3.60	0	−	10	
$\Delta I_{CCA/B}$	Increase in I_{CC} per Input; Other Inputs at V_{CC} or GND	V_{IH} = 3.0 V	3.60	3.60	−	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. V_{CCI} = the V_{CC} associated with the data input under test.
6. V_{CCO} = the V_{CC} associated with the output under test.
7. Don't care = any valid logic level.
8. Reflects current per supply, V_{CCA} or V_{CCB}.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = −40 °C to +85 °C										Unit
		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Typ	
V_{CCA} = 3.0 V to 3.6 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
t_{PZH}, t_{PZL}	Output Enable /OE to B	0.5	4.0	0.7	4.4	1.0	5.9	1.0	6.4	1.5	17.0	ns
	Output Enable /OE to A	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	
t_{PHZ}, t_{PLZ}	Output Disable /OE to B	0.2	3.8	0.2	4.0	0.7	4.8	1.5	6.2	2.0	17.0	ns
	Output Disable /OE to A	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	
V_{CCA} = 2.3 V to 2.7 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
t_{PZH}, t_{PZL}	Output Enable /OE to B	0.6	4.2	0.8	4.6	1.0	6.0	1.0	6.8	1.5	17.0	ns
	Output Enable /OE to A	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	
t_{PHZ}, t_{PLZ}	Output Disable /OE to B	0.2	4.1	0.2	4.3	0.7	4.8	1.5	6.7	2.0	17.0	ns
	Output Disable /OE to A	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
V_{CCA} = 1.65 V to 1.95 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
t_{PZH}, t_{PZL}	Output Enable /OE to B	0.6	5.2	0.8	5.4	1.2	6.9	1.2	7.2	1.5	18.0	ns
	Output Enable /OE to A	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	
t_{PHZ}, t_{PLZ}	Output Disable /OE to B	0.2	5.1	0.2	5.2	0.8	5.2	1.5	7.0	2.0	17.0	ns
	Output Disable /OE to A	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	
V_{CCA} = 1.4 V to 1.6 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
t_{PZH}, t_{PZL}	Output Enable /OE to B	1.1	7.5	1.1	7.6	1.3	7.7	1.4	7.9	2.0	20.0	ns
	Output Enable /OE to A	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	
t_{PHZ}, t_{PLZ}	Output Disable /OE to B	0.4	6.1	0.4	6.2	0.9	6.2	1.5	7.5	2.0	18.0	ns
	Output Disable /OE to A	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	
V_{CCA} = 1.1 V to 1.3 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
t_{PZH}, t_{PZL}	Output Enable /OE to B	1.0	12.0	1.0	9.0	2.0	10.0	2.0	11.0	2.0	24.0	ns
	Output Enable /OE to A	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	
t_{PHZ}, t_{PLZ}	Output Disable /OE to B	1.0	15.0	0.7	7.0	1.0	8.0	2.0	10.0	2.0	20.0	ns
	Output Disable /OE to A	2.0	15.0	2.0	12.0	2.0	12.0	2.0	12.0	2.0	12.0	

CAPACITANCE

Symbol	Parameter	Conditions	T_A = +25 °C	Unit
			Typical	
C_{IN}	Input Capacitance (Pins O/E, TR)	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	4	pF
$C_{I/O}$	Input/Output Capacitance A_n, B_n Ports	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	5	pF
C_{PD}	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	20	pF

AC LOADINGS AND WAVEFORMS

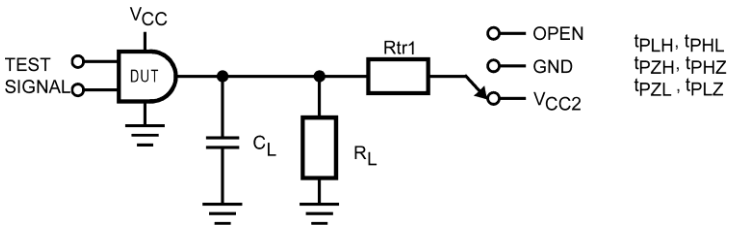
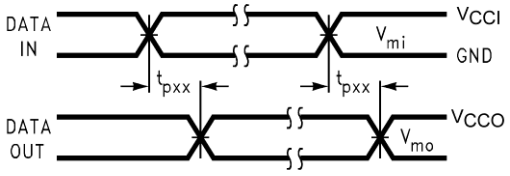


Figure 2. AC Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PLZ}, t_{PZL}	V_{CC0} · 2 at V_{CCO} = 3.3 ±0.3 V, 2.5 V ±0.2 V, 1.8 V ±0.15 V, 1.5 V ±0.1 V, 1.2 V ±0.1 V
t_{PHZ}, t_{PZH}	GND

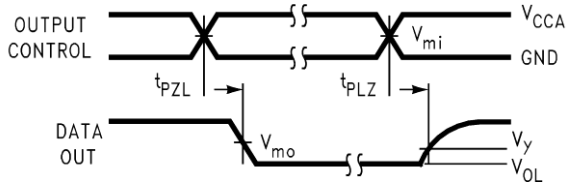
Table 1. AC LOAD TABLE

V_{CC0}	C_L	R_L	Rtr1
1.2 V ±0.1 V	15 pF	2 kΩ	2 kΩ
1.5 V ±0.1 V	15 pF	2 kΩ	2 kΩ
1.8 V ±0.15 V	15 pF	2 kΩ	2 kΩ
2.5 V ±0.2 V	15 pF	2 kΩ	2 kΩ
3.3 V ±0.3 V	15 pF	2 kΩ	2 kΩ



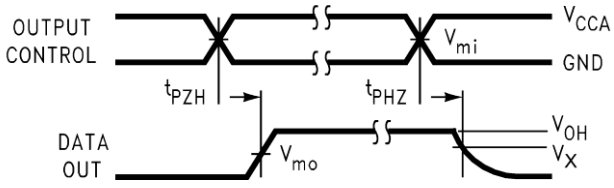
NOTES:
9. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
10. Input $t_R - t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.

Figure 3. Waveform for Inverting and Non-Inverting Functions



NOTES:
11. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
12. Input $t_R - t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.

Figure 4. 3-State Output Low Enable and Disable for Low Voltage Logic



NOTES:
13. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
14. Input $t_R - t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.

Figure 5. 3-State Output High Enable and Disable for Low Voltage Logic

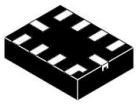
Symbol	V_{CC}				
	3.3 V ±0.3 V	**2.5 V ±0.2 V**	**1.8 V ±0.15 V**	**1.5 V ±0.1 V**	**1.2 V ±0.1 V**
V_{MI}	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2
V_{MO}	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2
V_X	V_{OH} − 0.3 V	V_{OH} – 0.15 V	V_{OH} – 0.15 V	V_{OH} – 0.1 V	V_{OH} – 0.1 V
V_Y	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V	V_{OL} + 0.1 V	V_{OL} + 0.1 V

15. For V_{MI} V_{CCO} = V_{CCA} for control pins T/$\overline{R}$ and $\overline{OE}$ or V_{CCA} / 2.

ORDERING INFORMATION

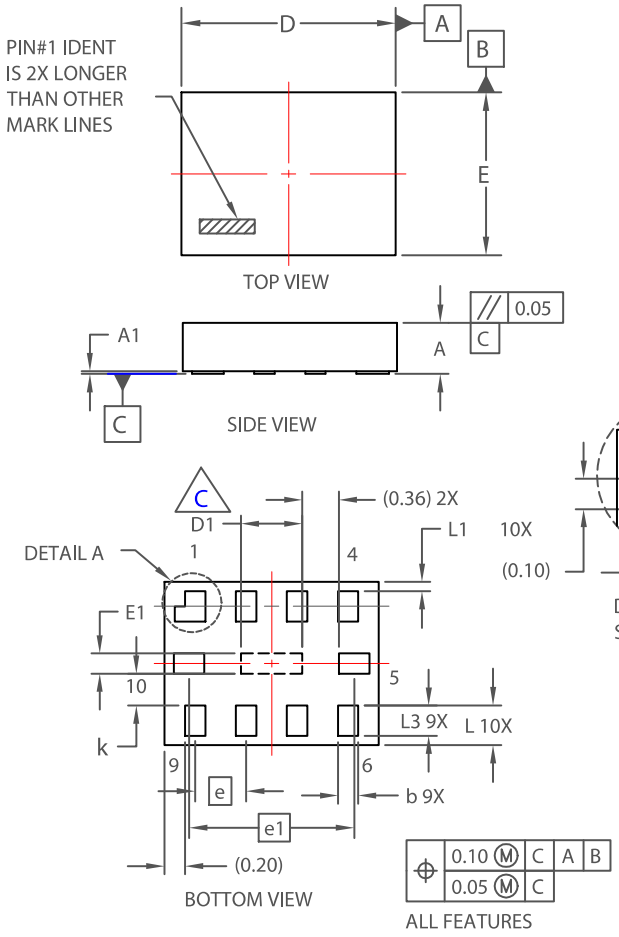
Part Number	Operating Temperature Range	Package Description	Shipping†
FXL2T245L10X	−40 °C to +85 °C	10−Lead, MicroPak, JEDEC MO255, 1.6 x 2.1 mm (Pb-Free, Halide Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



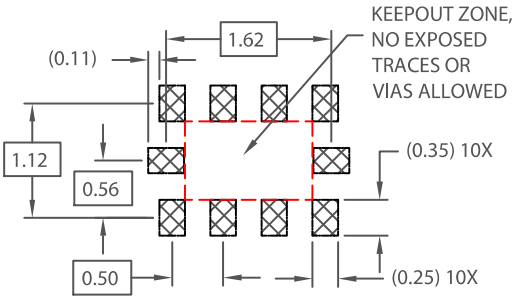
UQFN10 (MICROPAK™), 1.6X2.1, 0.5P
CASE 523AZ
ISSUE A

DATE 11 DEC 2019



NOTES:
A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.
D. DIMENSIONS WITHIN ( ) ARE UNCONTROLLED.

DIM	MIN.	NOM.	MAX.
A	0.50	0.55	0.65
A1	0.00	0.025	0.05
b	0.15	0.20	0.25
D	2.00	2.10	2.20
D1	0.55	0.60	0.65
E	1.50	1.60	1.70
E1	0.15	0.20	0.25
e	0.50 BSC		
e1	1.62 BSC		
k	0.20	--	--
L	0.25	0.30	0.42
L1	0.00	0.09	0.15
L3	0.25	0.30	0.35



RECOMMENDED
MOUNTING FOOTPRINT *

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**UQFN10 (MICROPAK™), 1.6X2.1, 0.5P**	**PAGE 1 OF 1**

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