

# Low-Voltage, Dual-Supply, 2-Bit, Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-State Outputs

## FXL2T245

### General Description

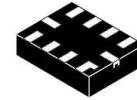
The FXL2T245 is a configurable, dual-voltage-supply translator designed for uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the  $V_{CCA}$  level and the B port tracks the  $V_{CCB}$  level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

The device remains in 3-state until both  $V_{CC}$ s reach active levels, allowing either  $V_{CC}$  to be powered-up first. Internal power-down control circuits place the device in 3-state if either  $V_{CC}$  is removed.

The Transmit / Receive ( $T/\bar{R}$ ) input determines the direction of data flow through the device. The  $\overline{OE}$  input, when HIGH, disables both the A and B ports by placing them in a 3-state condition. The FXL2T245 is designed so control pins  $T/\bar{R}$  and  $\overline{OE}$  are supplied by  $V_{CCA}$ .

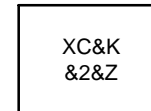
### Features

- Bi-Directional Interface between any 2 Levels from 1.1 V to 3.6 V
- Fully Configurable, Inputs Track  $V_{CC}$  Level
- Non-Preferential Power-up Sequencing; either  $V_{CC}$  maybe Powered-up First
- Outputs Remain in 3-State until Active  $V_{CC}$  Level is Reached
- Outputs Switch to 3-State if either  $V_{CC}$  is at GND
- Power-Off Protection
- Control Inputs ( $T/R$ ,  $OE$ ) Levels are Referenced to  $V_{CCA}$  Voltage
- Packaged in 10-Lead MicroPak (1.6 mm x 2.1 mm) Package
- ESD Protection Exceeds:
  - ◆ 4 kV HBM ESD JESD22–A114 & Mil Std 883e 3015.7)
  - ◆ 8 kV HBM I/O to GND ESD (per JESD22–A114 & Mil Std 883e 3015.7)
  - ◆ 1 kV CDM ESD (per ESD STM 5.3)
  - ◆ 200 V MM ESD (per JESD22–A115 & ESD STM5.2)



UQFN10 (MICROPAK™), 1.6 x 2.1, 0.5P  
CASE 523AZ

### MARKING DIAGRAM



XC = Specific Device Code  
 &K = 2-Digits Lot Run Traceability Code  
 &2 = 2-Digit Date Code  
 &Z = Assembly Plant Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# FXL2T245

## PIN CONFIGURATION

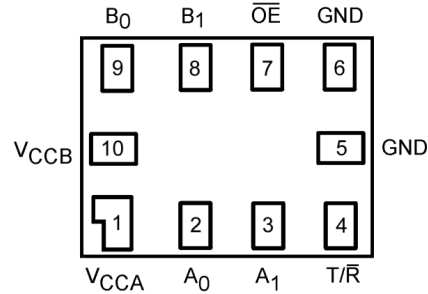


Figure 1. Pin Assignments

## PIN DESCRIPTION

Pin #	Pin Name	Description
1	V <sub>CCA</sub>	Side A Power Supply
2	A <sub>0</sub>	Side A Inputs or 3-State Outputs
3	A <sub>1</sub>	Side A Inputs or 3-State Outputs
4	T/ $\overline{R}$	Transmit/Receive Input
5, 6	GND	Ground
7	$\overline{OE}$	Output Enable Input
8	B <sub>1</sub>	Side B Inputs or 3-State Outputs
9	B <sub>0</sub>	Side B Inputs or 3-State Outputs
10	V <sub>CCB</sub>	Side B Power Supply

## TRUTH TABLE

Inputs		Outputs
$\overline{OE}$	T/ $\overline{R}$	
LOW	LOW	Bus B Data to Bus A
LOW	HIGH	Bus A Data to Bus B

1. LOW = low voltage level.
2. HIGH = high voltage level.

## FUNCTIONAL DESCRIPTION

### Power-Up / Power-Down Sequencing

Due to the chip design, the FXL2T245 translator offers the advantage of either V<sub>CC</sub> being powered up first. When either V<sub>CC</sub> is at 0 V, outputs are in a high-impedance state. The control inputs (T/ $\overline{R}$  and  $\overline{OE}$ ) are designed to track the V<sub>CCA</sub> supply. A pull-up resistor tying  $\overline{OE}$  to V<sub>CCA</sub> should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the  $\overline{OE}$  driver.

The recommended power-up sequence is:

1. Apply power to either V<sub>CC</sub>.
2. Apply power to the T/ $\overline{R}$  input (logic HIGH for A-to-B operation; logic LOW for B-to-A operation) and to the respective data inputs (A port or B port). This may occur at the same time as step 1.
3. Apply power to the other V<sub>CC</sub>.
4. Drive the  $\overline{OE}$  input LOW to enable the device.

The recommended power-down sequence is:

1. Drive  $\overline{OE}$  input HIGH to disable the device.
2. Remove power from either V<sub>CC</sub>.
3. Remove power from the other V<sub>CC</sub>.

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CCA</sub>	Supply Voltage			−0.5	4.6	V
V <sub>CCB</sub>				−0.5	4.6	
V <sub>I</sub>	DC Input Voltage	I/O Port A		−0.5	4.6	V
		I/O Port B		−0.5	4.6	
		Control Inputs (T/R, $\overline{OE}$ )		−0.5	4.6	
V <sub>O</sub>	Output Voltage (Note 3)	Output 3-State		−0.5	4.6	V
		Output Active (An)		−0.5 to V <sub>CCA</sub>	0.5	
		Output Active (Bn)		−0.5 to V <sub>CCB</sub>	0.5	
I <sub>IK</sub>	DC Input Diode Current	V <sub>I</sub> < 0 V		−	−50	mA
I <sub>OK</sub>	DC Output Diode Current	V <sub>O</sub> < 0 V		−	−50	mA
		V <sub>O</sub> > V <sub>CC</sub>		−	+50	
I <sub>OH</sub> /I <sub>OL</sub>	DC Output Source/Sink Current			−	±50	mA
I <sub>CC</sub>	DC VCC or Ground Current per Supply Pin			−	±100	mA
T <sub>STG</sub>	Storage Temperature Range			−65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22–A114, Mil Std 883e 3015.7	All Pins	−	4	kV
			I/O to GND	−	8	
		Charged Device Model, JESD22–C101, STM 5.3		−	1	V
		Machine Model, JESD22–A115, STM 5.2		−	200	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3.  $I_O$  Absolute Maximum Rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	Power Supply	Operating V <sub>CCA</sub> or V <sub>CCB</sub>		1.1	3.6	V
V <sub>I</sub>	Input Voltage	Port A		0	3.6	V
		Port B		0	3.6	
		Control Inputs (T/ $\overline{R}$ , $\overline{OE}$ )		0	V <sub>CCA</sub>	
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub>	3.0 V to 3.6 V	–	±24	mA
			2.3 V to 2.7 V	–	±18	
			1.65 V to 1.95 V	–	±6	
			1.40 V to 1.65 V	–	±2	
			1.1 V to 1.4 V	–	±0.5	
T <sub>A</sub>	Operating Temperature, Free Air			–40	+85	°C
ΔV/Δt	Minimum Input Edge Rate	V <sub>CCA/B</sub> = 1.1 V to 3.6 V		–	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. All unused inputs and I/O pins must be held at  $V_{CCI}$  or GND.

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## ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC0</sub> (V)	V <sub>CCI</sub> (V)	Min	Max	Unit
V <sub>IH</sub>	HIGH Level Input (Note 5)	Data Inputs A <sub>n</sub> , B <sub>n</sub>	1.10 to 3.60	2.70 to 3.60	2.00	–	V
				2.30 to 2.70	1.60	–	
				1.65 to 2.30	0.65 x V <sub>CCI</sub>	–	
				1.40 to 1.65	0.65 x V <sub>CCI</sub>	–	
				1.10 to 1.40	0.90 x V <sub>CCI</sub>	–	
		Control Pins / $\overline{OE}$ , T/ $\overline{R}$ (Referenced to V <sub>CCA</sub> )		2.70 to 3.60	2.00	–	
				2.30 to 2.70	1.60	–	
				1.65 to 2.30	0.65 x V <sub>CCA</sub>	–	
				1.40 to 1.65	0.65 x V <sub>CCA</sub>	–	
				1.10 to 1.40	0.90 x V <sub>CCA</sub>	–	
V <sub>IL</sub>	LOW Level Input (Note 5)	Data Inputs A <sub>n</sub> , B <sub>n</sub>	1.10 to 3.60	2.70 to 3.60	–	0.80	V
				2.30 to 2.70	–	0.70	
				1.65 to 2.30	–	0.35 x V <sub>CCI</sub>	
				1.40 to 1.65	–	0.35 x V <sub>CCI</sub>	
				1.10 to 1.40	–	0.10 x V <sub>CCI</sub>	
		Control Pins / $\overline{OE}$ , T/ $\overline{R}$ (Referenced to V <sub>CCA</sub> )		2.70 to 3.60	–	0.80	
				2.30 to 2.70	–	0.70	
				1.65 to 2.30	–	0.35 x V <sub>CCI</sub>	
				1.40 to 1.65	–	0.35 x V <sub>CCI</sub>	
				1.10 to 1.40	–	0.10 x V <sub>CCI</sub>	
V <sub>OH</sub>	HIGH Level Output (Note 6)	I <sub>OH</sub> = –100 μA	1.10 to 3.60	1.10 to 3.60	V <sub>CC0</sub> – 0.20	–	V
		I <sub>OH</sub> = –12 mA	2.70	2.70	2.20	–	
		I <sub>OH</sub> = –18 mA	3.00	3.00	2.40	–	
		I <sub>OH</sub> = –24 mA	3.00	3.00	2.20	–	
		I <sub>OH</sub> = –6 mA	2.30	2.30	2.00	–	
		I <sub>OH</sub> = –12 mA	2.30	2.30	1.80	–	
		I <sub>OH</sub> = –18 mA	2.30	2.30	1.70	–	
		I <sub>OH</sub> = –6 mA	1.65	1.65	1.25	–	
		I <sub>OH</sub> = –2 mA	1.40	1.40	1.05	–	
		I <sub>OH</sub> = –0.5 mA	1.10	1.10	0.75 x V <sub>CC0</sub>	–	
V <sub>OL</sub>	LOW Level Output (Note 6)	I <sub>OL</sub> = 100 μA	1.10 to 3.60	1.10 to 3.60	–	0.20	V
		I <sub>OL</sub> = 12 mA	2.70	2.70	–	0.40	
		I <sub>OL</sub> = 18 mA	3.00	3.00	–	0.40	
		I <sub>OL</sub> = 24 mA	3.00	3.00	–	0.55	
		I <sub>OL</sub> = 12 mA	2.30	2.30	–	0.40	
		I <sub>OL</sub> = 18 mA	2.30	2.30	–	0.60	
		I <sub>OL</sub> = 6 mA	1.65	1.65	–	0.30	
		I <sub>OL</sub> = 2 mA	1.40	1.40	–	0.35	
		I <sub>OL</sub> = 0.5 mA	1.10	1.10	–	0.30 x V <sub>CC0</sub>	
I <sub>L</sub>	Input Leakage Current, Control Pins	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.60	1.10 to 3.60	–	±1.0	μA

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## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V <sub>CCO</sub> (V)	V <sub>CCI</sub> (V)	Min	Max	Unit
I <sub>OFF</sub>	Power Off Leakage Current	A <sub>n</sub> , V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	3.60	0	–	±10	μA
		B <sub>n</sub> , V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0	3.60	–	±10	
I <sub>OZ</sub>	3-State Output Leakage (0 ≤ V <sub>O</sub> ≤ 3.6 V, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	A <sub>n</sub> , B <sub>n</sub> , /OE = V <sub>IH</sub>	3.60	3.60	–	±10	μA
		B <sub>n</sub> , /OE = Don't Care (Note 7)	3.60	0	–	±10	
		A <sub>n</sub> , /OE = Don't Care (Note 7)	0	3.60	–	±10	
I <sub>CCA/B</sub>	Quiescent Supply Current (Note 8)	V <sub>I</sub> = V <sub>CCI</sub> or GND; I <sub>O</sub> = 0	1.10 to 3.60	1.10 to 3.60	–	20	μA
I <sub>CCZ</sub>			1.10 to 3.60	1.10 to 3.60	–	20	μA
I <sub>CCA</sub>		V <sub>I</sub> =V <sub>CCA</sub> or GND; I <sub>O</sub> = 0	1.10 to 3.60	0	–	–10	μA
			0	1.10 to 3.60	–	10	
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCB</sub> or GND; I <sub>O</sub> = 0	0	1.10 to 3.60	–	–10	μA
			1.10 to 3.60	0	–	10	
ΔI <sub>CCA/B</sub>	Increase in I <sub>CC</sub> per Input; Other Inputs at V <sub>CC</sub> or GND	V <sub>IH</sub> = 3.0 V	3.60	3.60	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. V<sub>CCI</sub> = the V<sub>CC</sub> associated with the data input under test.

6. V<sub>CCO</sub> = the V<sub>CC</sub> associated with the output under test.

7. Don't care = any valid logic level.

8. Reflects current per supply, V<sub>CCA</sub> or V<sub>CCB</sub>.

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = −40 °C to +85 °C										Unit
		V <sub>CCB</sub> = 3.0 V to 3.6 V		V <sub>CCB</sub> = 2.3 V to 2.7 V		V <sub>CCB</sub> = 1.65 V to 1.95 V		V <sub>CCB</sub> = 1.4 V to 1.6 V		V <sub>CCB</sub> = 1.1 V to 1.3 V		
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Typ	

### $V_{CCA} = 3.0\text{ V to }3.6\text{ V}$

$t_{PLH}, t_{PHL}$	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
$t_{PZH}, t_{PZL}$	Output Enable /OE to B	0.5	4.0	0.7	4.4	1.0	5.9	1.0	6.4	1.5	17.0	ns
	Output Enable /OE to A	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	
$t_{PHZ}, t_{PLZ}$	Output Disable /OE to B	0.2	3.8	0.2	4.0	0.7	4.8	1.5	6.2	2.0	17.0	ns
	Output Disable /OE to A	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	

### $V_{CCA} = 2.3\text{ V to }2.7\text{ V}$

$t_{PLH}, t_{PHL}$	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
$t_{PZH}, t_{PZL}$	Output Enable /OE to B	0.6	4.2	0.8	4.6	1.0	6.0	1.0	6.8	1.5	17.0	ns
	Output Enable /OE to A	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	
$t_{PHZ}, t_{PLZ}$	Output Disable /OE to B	0.2	4.1	0.2	4.3	0.7	4.8	1.5	6.7	2.0	17.0	ns
	Output Disable /OE to A	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	

### $V_{CCA} = 1.65\text{ V to }1.95\text{ V}$

$t_{PLH}, t_{PHL}$	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
$t_{PZH}, t_{PZL}$	Output Enable /OE to B	0.6	5.2	0.8	5.4	1.2	6.9	1.2	7.2	1.5	18.0	ns
	Output Enable /OE to A	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	
$t_{PHZ}, t_{PLZ}$	Output Disable /OE to B	0.2	5.1	0.2	5.2	0.8	5.2	1.5	7.0	2.0	17.0	ns
	Output Disable /OE to A	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	

### $V_{CCA} = 1.4\text{ V to }1.6\text{ V}$

$t_{PLH}, t_{PHL}$	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
$t_{PZH}, t_{PZL}$	Output Enable /OE to B	1.1	7.5	1.1	7.6	1.3	7.7	1.4	7.9	2.0	20.0	ns
	Output Enable /OE to A	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	
$t_{PHZ}, t_{PLZ}$	Output Disable /OE to B	0.4	6.1	0.4	6.2	0.9	6.2	1.5	7.5	2.0	18.0	ns
	Output Disable /OE to A	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	

### $V_{CCA} = 1.1\text{ V to }1.3\text{ V}$

$t_{PLH}, t_{PHL}$	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
$t_{PZH}, t_{PZL}$	Output Enable /OE to B	1.0	12.0	1.0	9.0	2.0	10.0	2.0	11.0	2.0	24.0	ns
	Output Enable /OE to A	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	
$t_{PHZ}, t_{PLZ}$	Output Disable /OE to B	1.0	15.0	0.7	7.0	1.0	8.0	2.0	10.0	2.0	20.0	ns
	Output Disable /OE to A	2.0	15.0	2.0	12.0	2.0	12.0	2.0	12.0	2.0	12.0	

## CAPACITANCE

Symbol	Parameter	Conditions	$T_A = +25\text{ }^{\circ}\text{C}$	Unit
			Typical	
$C_{IN}$	Input Capacitance (Pins O/E, TR)	$V_{CCA} = V_{CCB} = 3.3\text{ V}, V_I = 0\text{ V}$ or $V_{CCA/B}$	4	pF
$C_{I/O}$	Input/Output Capacitance $A_n, B_n$ Ports	$V_{CCA} = V_{CCB} = 3.3\text{ V}, V_I = 0\text{ V}$ or $V_{CCA/B}$	5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3\text{ V}, V_I = 0\text{ V}$ or $V_{CC}, f = 10\text{ MHz}$	20	pF

# AC LOADINGS AND WAVEFORMS

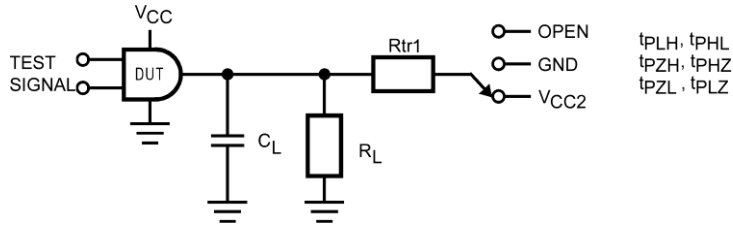
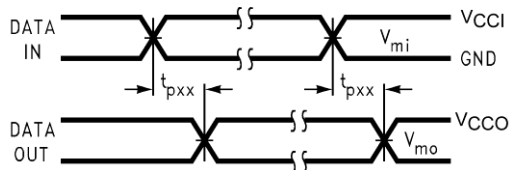


Figure 2. AC Test Circuit

Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PLZ}$ , $t_{PZL}$	$V_{CC0} \cdot 2$ at $V_{CC0} = 3.3 \pm 0.3 \text{ V}$ , $2.5 \text{ V} \pm 0.2 \text{ V}$ , $1.8 \text{ V} \pm 0.15 \text{ V}$ , $1.5 \text{ V} \pm 0.1 \text{ V}$ , $1.2 \text{ V} \pm 0.1 \text{ V}$
$t_{PHZ}$ , $t_{PZH}$	GND

Table 1. AC LOAD TABLE

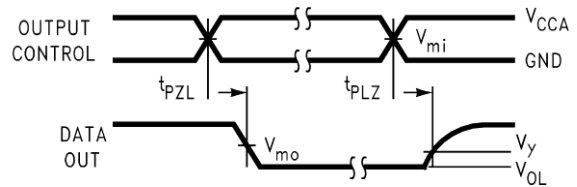
$V_{CC0}$	$C_L$	$R_L$	$R_{tr1}$
$1.2 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k $\Omega$	2 k $\Omega$
$1.5 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k $\Omega$	2 k $\Omega$
$1.8 \text{ V} \pm 0.15 \text{ V}$	15 pF	2 k $\Omega$	2 k $\Omega$
$2.5 \text{ V} \pm 0.2 \text{ V}$	15 pF	2 k $\Omega$	2 k $\Omega$
$3.3 \text{ V} \pm 0.3 \text{ V}$	15 pF	2 k $\Omega$	2 k $\Omega$



NOTES:

9. Input  $t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%.
10. Input  $t_R - t_F = 2.5 \text{ ns}$ , 10% to 90%, at  $V_I = 3.0 \text{ V}$  to  $3.6 \text{ V}$  only.

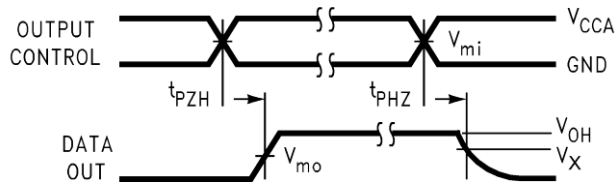
Figure 3. Waveform for Inverting and Non-Inverting Functions



NOTES:

11. Input  $t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%.
12. Input  $t_R - t_F = 2.5 \text{ ns}$ , 10% to 90%, at  $V_I = 3.0 \text{ V}$  to  $3.6 \text{ V}$  only.

Figure 4. 3-State Output Low Enable and Disable for Low Voltage Logic



NOTES:

13. Input  $t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%.
14. Input  $t_R - t_F = 2.5 \text{ ns}$ , 10% to 90%, at  $V_I = 3.0 \text{ V}$  to  $3.6 \text{ V}$  only.

Figure 5. 3-State Output High Enable and Disable for Low Voltage Logic

## FXL2T245

Symbol	$V_{CC}$				
	3.3 V $\pm 0.3$ V	2.5 V $\pm 0.2$ V	1.8 V $\pm 0.15$ V	1.5 V $\pm 0.1$ V	1.2 V $\pm 0.1$ V
$V_{MI}$	$V_{CCI} / 2$	$V_{CCI} / 2$	$V_{CCI} / 2$	$V_{CCI} / 2$	$V_{CCI} / 2$
$V_{MO}$	$V_{CCO} / 2$	$V_{CCO} / 2$	$V_{CCO} / 2$	$V_{CCO} / 2$	$V_{CCO} / 2$
$V_X$	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.1$ V	$V_{OH} - 0.1$ V
$V_Y$	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.1$ V	$V_{OL} + 0.1$ V

15. For  $V_{MI}$   $V_{CCO} = V_{CCA}$  for control pins  $T/\bar{R}$  and  $\bar{OE}$  or  $V_{CCA} / 2$ .

### ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Description	Shipping <sup>†</sup>
FXL2T245L10X	-40 °C to +85 °C	10-Lead, MicroPak, JEDEC MO255, 1.6 x 2.1 mm (Pb-Free, Halide Free)	5000 / Tape & Reel

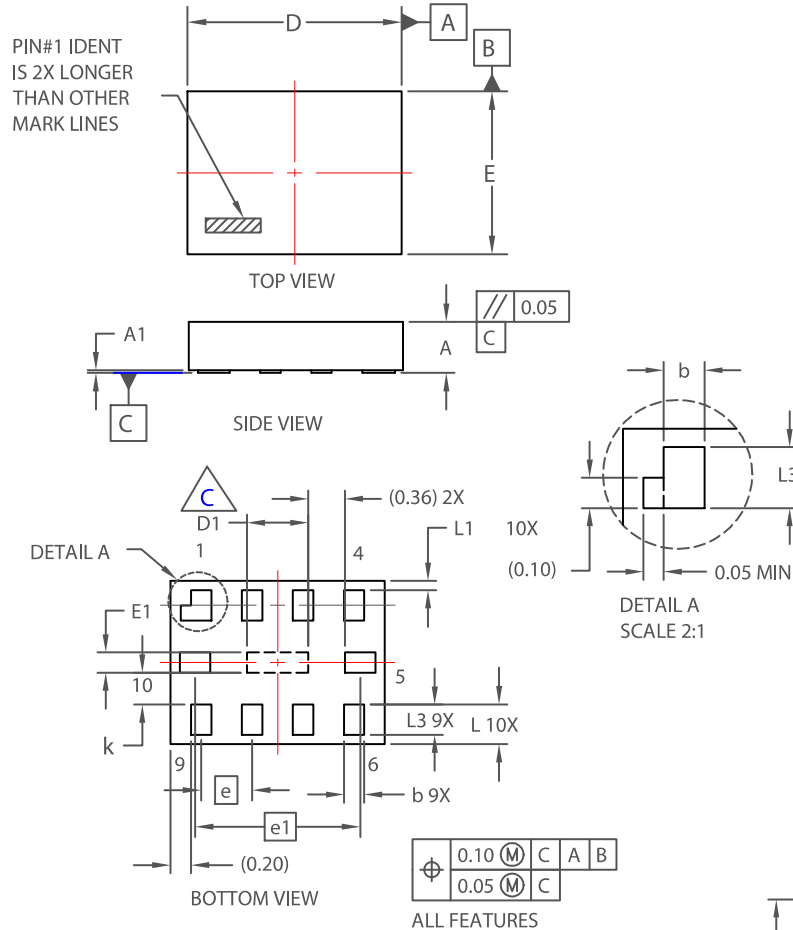
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





**UQFN10 (MICROPAK™), 1.6X2.1, 0.5P**  
CASE 523AZ  
ISSUE A

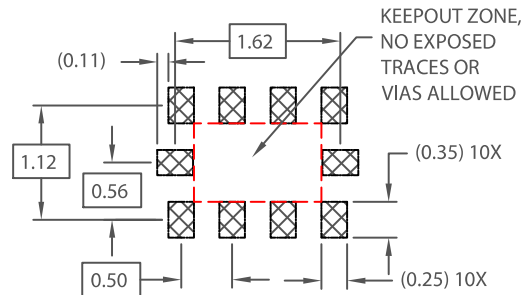
DATE 11 DEC 2019



NOTES:

- A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD.  
B. DIMENSIONS ARE IN MILLIMETERS.  
C. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.  
D. DIMENSIONS WITHIN ( ) ARE UNCONTROLLED.

DIM	MIN.	NOM.	MAX.
A	0.50	0.55	0.65
A1	0.00	0.025	0.05
b	0.15	0.20	0.25
D	2.00	2.10	2.20
D1	0.55	0.60	0.65
E	1.50	1.60	1.70
E1	0.15	0.20	0.25
e	0.50 BSC		
e1	1.62 BSC		
k	0.20	--	--
L	0.25	0.30	0.42
L1	0.00	0.09	0.15
L3	0.25	0.30	0.35



**RECOMMENDED  
MOUNTING FOOTPRINT \***

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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