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## IRLS640A

### N-Channel Logic Level A-FET

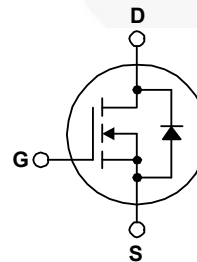
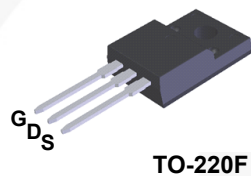
200 V, 9.8 A, 180 mΩ

#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

#### Features

- 9.8 A, 200 V,  $R_{DS(on)} = 180 \text{ m}\Omega @ V_{GS} = 5 \text{ V}$
- Low Gate Charge (Typ. 40 nC)
- Low Crss (Typ. 95 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- Logic-Level Gate Drive



#### Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	200	V
$I_D$	Continuous Drain Current ( $T_C=25^\circ\text{C}$ )	9.8	A
	Continuous Drain Current ( $T_C=100^\circ\text{C}$ )	6.2	
$I_{DM}$	Drain Current-Pulsed <sup>①</sup>	63	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy <sup>②</sup>	64	mJ
$I_{AR}$	Avalanche Current <sup>①</sup>	18	A
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>③</sup>	5	V/ns
$P_D$	Total Power Dissipation ( $T_C=25^\circ\text{C}$ )	40	W
	Linear Derating Factor	0.32	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	- 55 to +150	°C
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

#### Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	3.13	°C/W
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
IRLS640A	IRLS640A	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	200	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.17	--	V/ $^\circ\text{C}$	$I_D=250\mu A$ <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu A$	$V_{DS}=200V$
		--	--	100		$V_{DS}=160V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.18	$\Omega$	$V_{GS}=5V, I_D=4.9A$ ④
$g_{fs}$	Forward Transconductance	--	13.3	--	S	$V_{DS}=40V, I_D=4.9A$ ④
$C_{iss}$	Input Capacitance	--	1310	1705	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	--	200	250		
$C_{rss}$	Reverse Transfer Capacitance	--	95	120		
$t_{d(on)}$	Turn-On Delay Time	--	11	30	ns	$V_{DD}=100V, I_D=18A,$ $R_G=4.6\Omega$ <b>See Fig 13</b> ④ ⑤
$t_r$	Rise Time	--	8	25		
$t_{d(off)}$	Turn-Off Delay Time	--	46	100		
$t_f$	Fall Time	--	15	40		
$Q_g$	Total Gate Charge	--	40	56	nC	$V_{DS}=160V, V_{GS}=5V,$ $I_D=18A$ <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
$Q_{gs}$	Gate-Source Charge	--	6.8	--		
$Q_{gd}$	Gate-Drain("Miller") Charge	--	18.6	--		

## Source-Drain Diode Ratings and Characteristics

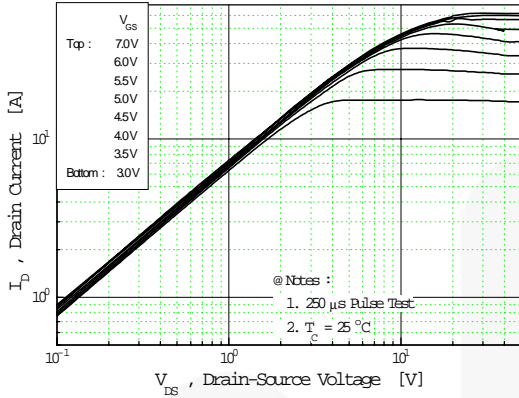
Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current	--	--	18	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	--	--	63		
$V_{SD}$	Diode Forward Voltage ④	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=9.8A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	224	--	ns	$T_J=25^\circ\text{C}, I_F=18A$
$Q_{rr}$	Reverse Recovery Charge	--	1.55	--	$\mu C$	$di_F/dt=100A/\mu s$ ④

### Notes ;

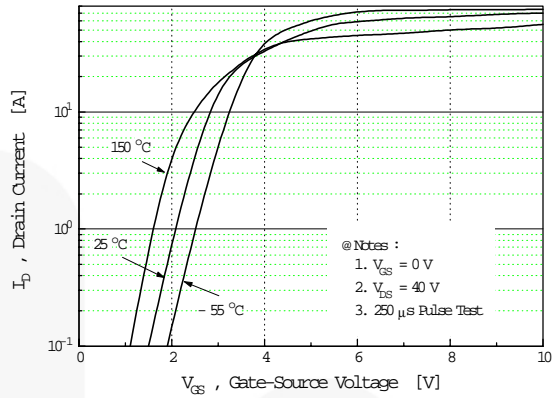
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=1\text{mH}, I_{AS}=9.8A, V_{DD}=50V, R_G=27\Omega$ , Starting  $T_J=25^\circ\text{C}$
- ③  $I_{SD}\leq 18A, di/dt\leq 260A/\mu s, V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width =  $250\mu s$ , Duty Cycle  $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

## Typical Characteristics

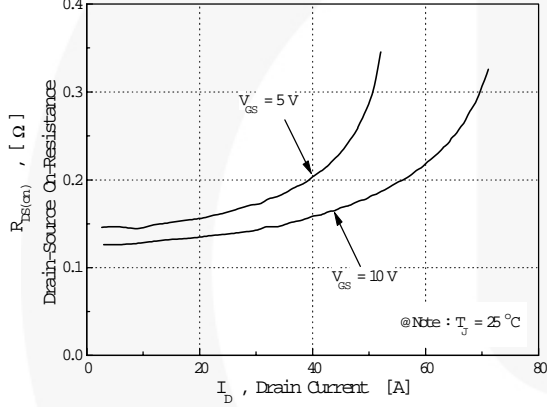
**Fig 1. Output Characteristics**



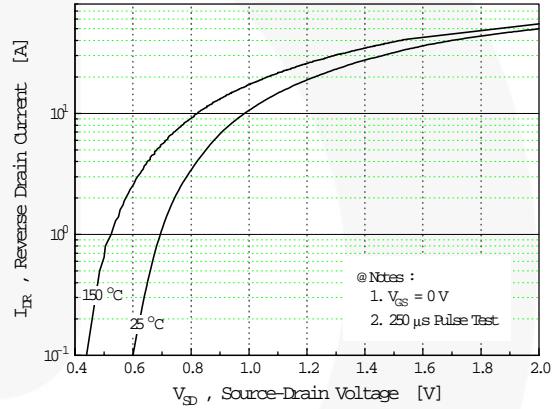
**Fig 2. Transfer Characteristics**



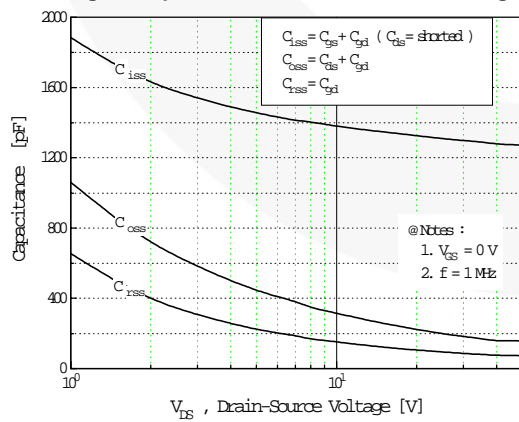
**Fig 3. On-Resistance vs. Drain Current**



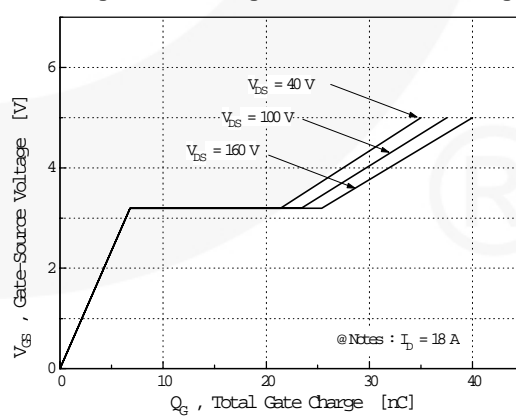
**Fig 4. Source-Drain Diode Forward Voltage**



**Fig 5. Capacitance vs. Drain-Source Voltage**



**Fig 6. Gate Charge vs. Gate-Source Voltage**



Typical Characteristics (continued)

Fig 7. Breakdown Voltage vs. Temperature

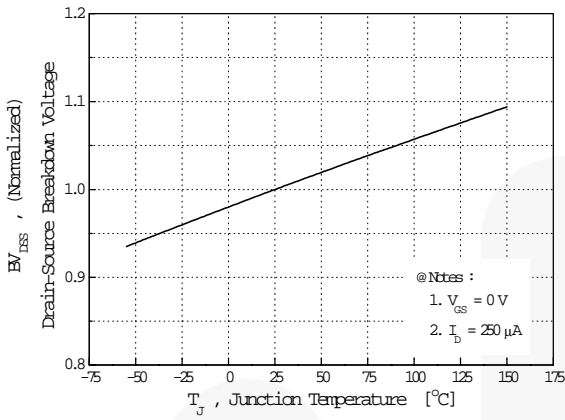


Fig 8. On-Resistance vs. Temperature

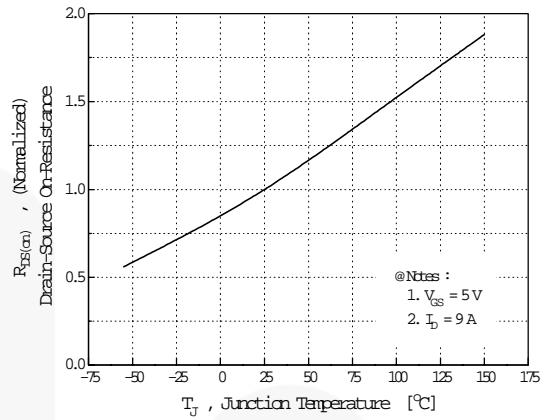


Fig 9. Max. Safe Operating Area

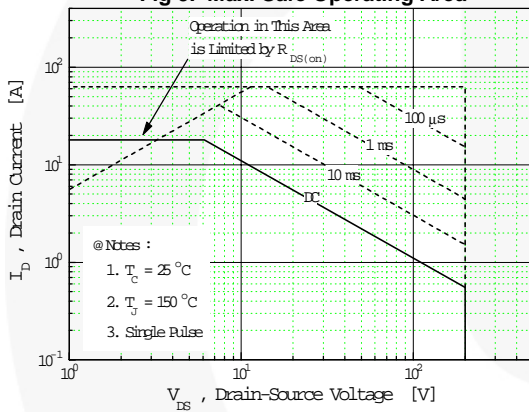


Fig 10. Max. Drain Current vs. Case Temperature

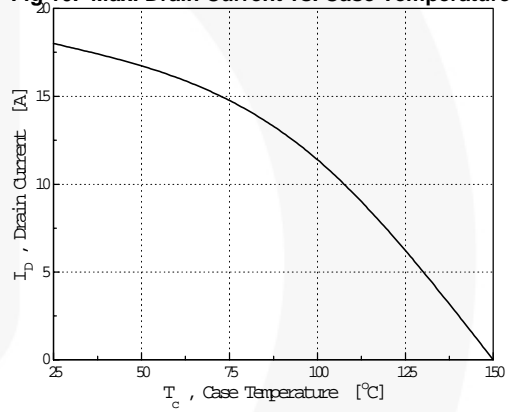


Fig 11. Thermal Response

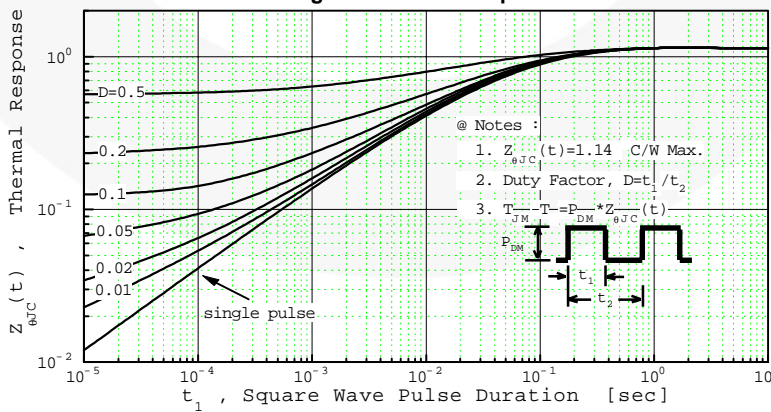




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

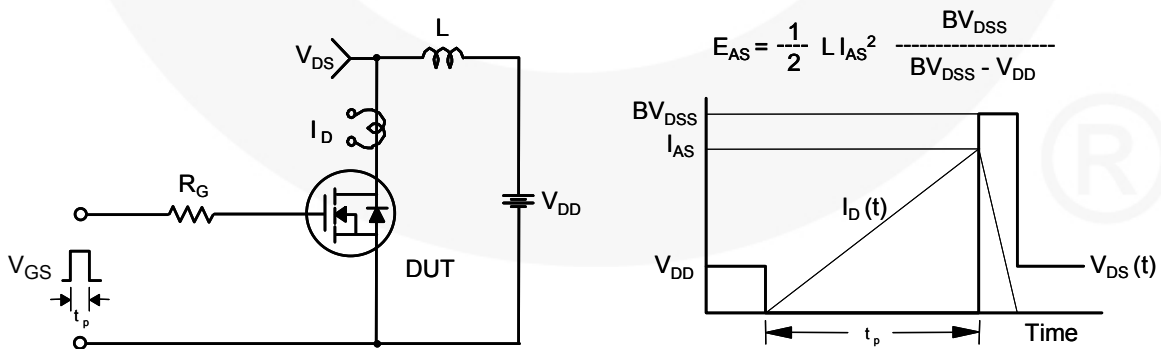
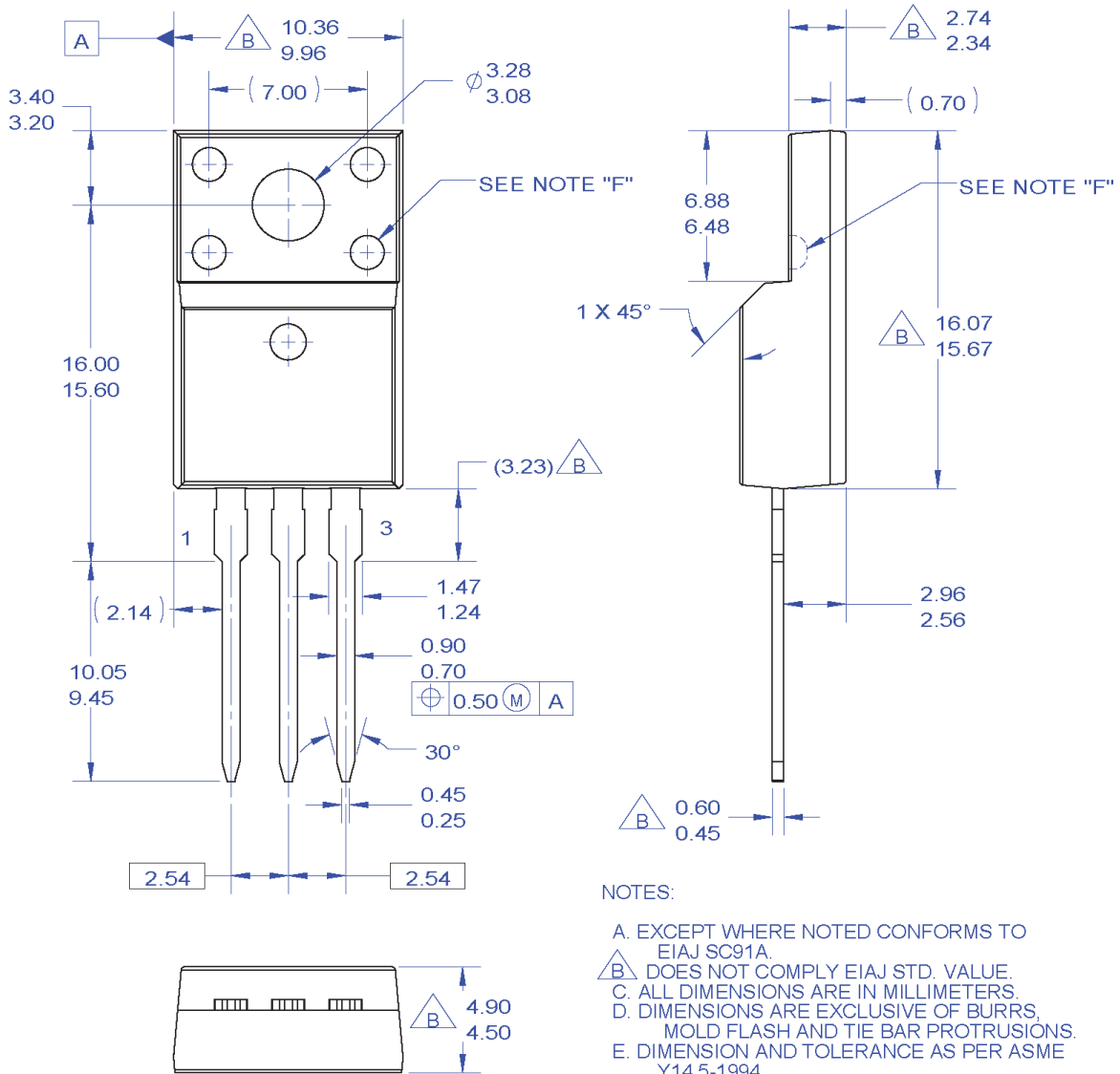


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

**Mechanical Dimensions**



**NOTES:**

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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