

# AF Control LSI

## LC898249AXH

### Overview

This LSI is Closed-Auto Focus control LSI equipped with hall sensor. It consists of 1 system of feedback circuit and constant current driver. It has also a built-in EEPROM and temperature sensor.

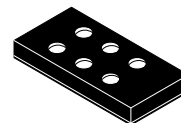
### Features

- Built-in Equalizer Circuit Using Digital Operation
  - ◆ AF Control Equalizer Circuit
  - ◆ Any Coefficient can be Specified by 2-wire Serial I/F (TWIF)
- 2-wire Serial Interface  
(The Communication Protocol is Compatible with I<sup>2</sup>C)
  - ◆ 4 Selectable Slave Addresses
    - 50h(W)/51h(R), 53h(R)
    - 74h(W)/75h(R), 77h(R)
    - E8h(W)/E9h(R), EBh(R)
    - E4h(W)/E5h(R), E7h(R) factory-configured
- Right Side Addresses are Used at the Access of Built-in EEPROM
- Built-in A/D Converter
- Built-in D/A Converter
  - ◆ Hall Offset
  - ◆ Constant Current Bias
- Built-in Hall Sensor
  - ◆ Si Hall Sensor
- Built-in EEPROM
  - ◆ 64 Byte (16 Byte / Page)
- Built-in OSC
- Built-in Constant Current Driver
  - ◆ 150 mA
- Package
  - ◆ WLCSP 6-pin (2 x 3 Pin), Thickness Max 0.29 mm, with Backside Coat
- Supply Voltage
  - ◆ VDD (2.6 V to 3.3 V)
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant



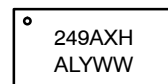
**ON Semiconductor®**

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**WLCSP6, 0.86x1.75x0.265  
CASE 567XD**

### MARKING DIAGRAM



249AXH = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
LC898249AXHTBG	WLCSP6	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

Pin Name	Description
I	Input
P	Power Supply, GND
NC	Not Connect
O	Output
B	Bidirection

- 2-wire serial interface
  - SCL I 2-wire serial interface clock pin
  - SDA B 2-wire serial interface data pin
- Driver interface
  - OUT1 O Driver output (to Actuator)
  - OUT2 O Driver output (to Actuator)
- Power supply pin
  - VDD P Power Supply
  - VSS P GND

*\*Process when pins are not used*

PIN TYPE “O” – Ensure that it is set to OPEN.

PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused.  
(Please contact ON Semiconductor for more information about selection of VDD or VSS.)

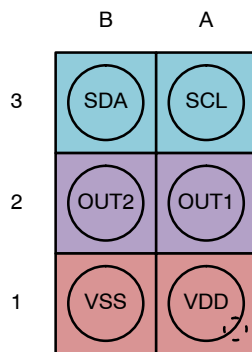
PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

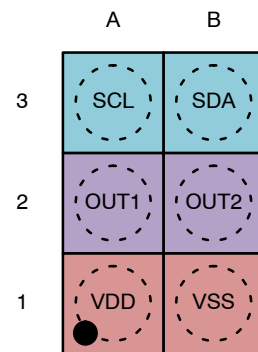
PIN LAYOUT

Table 2. PIN LAYOUT

Circuit Name	Number of PINs
Driver	2
Power	2
Logic	2



BOTTOM VIEW

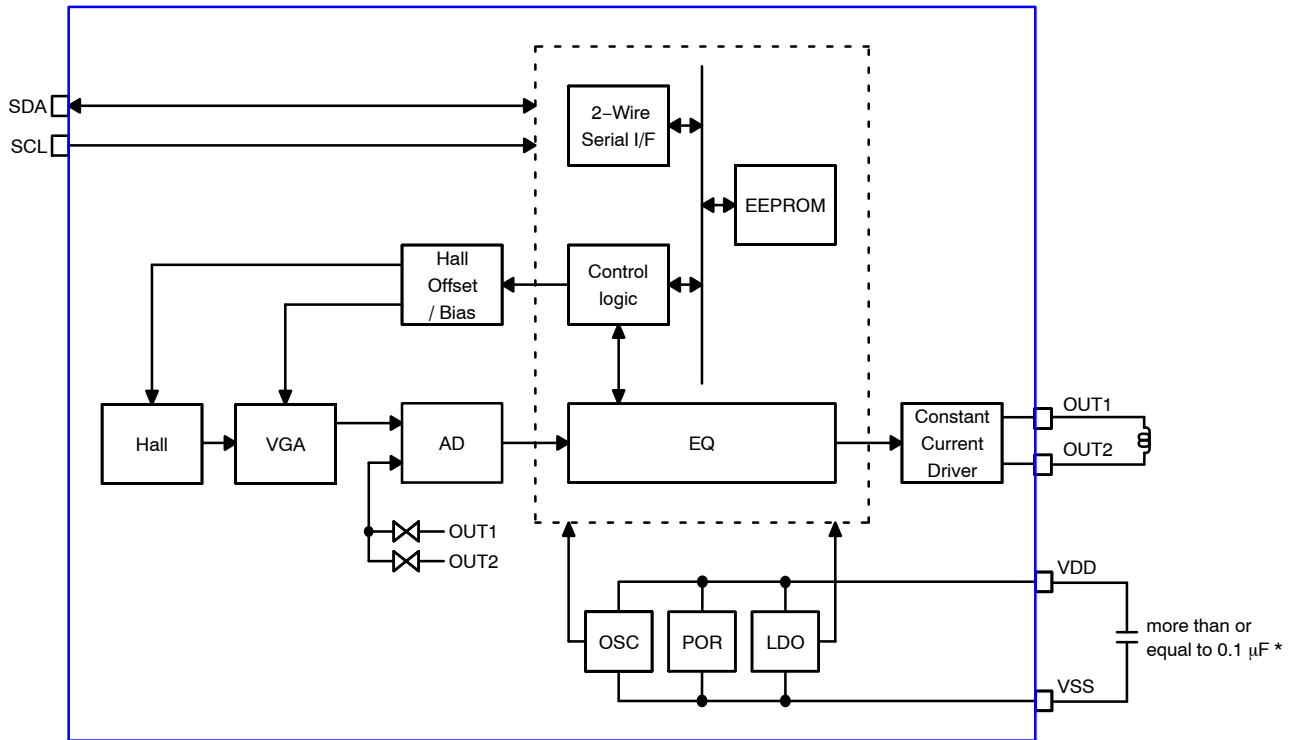


TOP VIEW

Figure 1. Pin Layout

# LC898249AXH

## BLOCK DIAGRAM



\*Consider capacitance of capacitor between VDD and VSS. According to power source environment, attach an additional capacitor in camera module.

Figure 2. Block Diagram

HALL ELEMENT POSITION

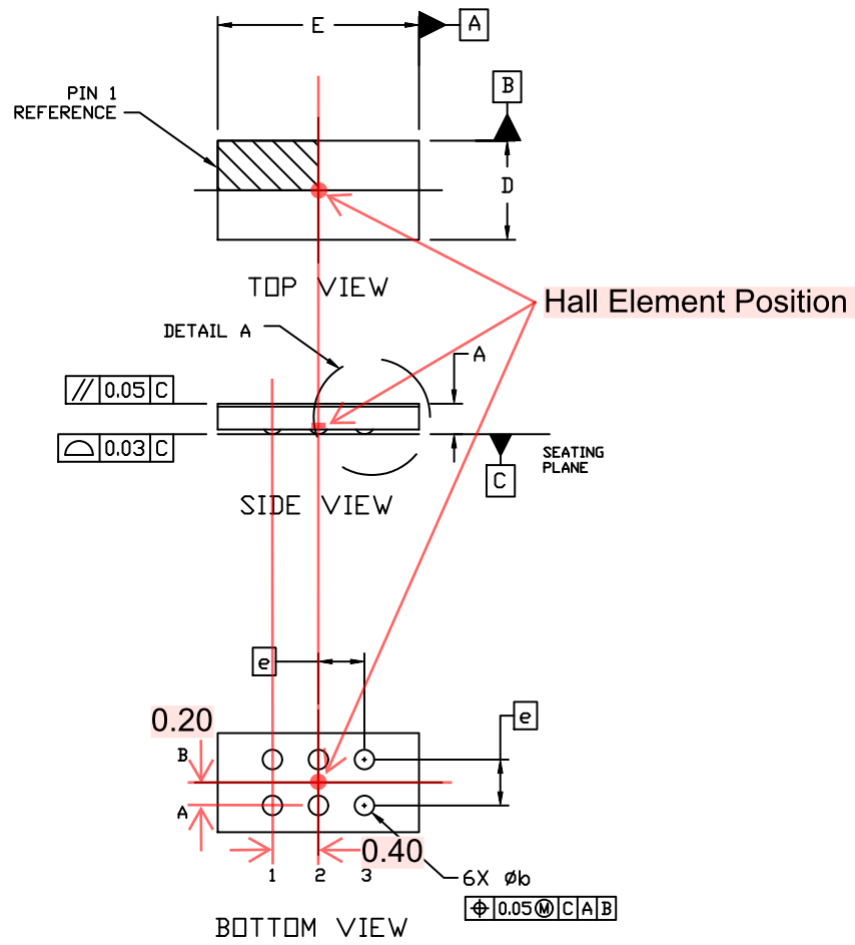


Figure 3. Hall Element Position

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## ELECTRICAL CHARACTERISTICS

**Table 3. ABSOLUTE MAXIMUM RATINGS** (VSS = 0 V)

Symbol	Item	Condition	Rating	Unit
V <sub>DD33</sub> max	Supply voltage	Ta ≤ 25°C	−0.3~4.6	V
V <sub>I33</sub> , V <sub>O33</sub>	Input/output voltage	Ta ≤ 25°C	−0.3~V <sub>DD33</sub> + 0.3	V
Tstg	Storage ambient temperature		−55~125	°C
Topr	Operating ambient temperature		−30~70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. ACCEPTABLE OPERATION RANGE** (Ta = −30~70°C, VSS = 0 V, 3 V power supply (VDD))

Symbol	Item	Min	Typ	Max	Unit
V <sub>DD33</sub>	Supply voltage	2.6	2.8	3.3	V
V <sub>IN</sub>	Input voltage range	0	–	V <sub>DD33</sub>	V

**Table 5. DC CHARACTERISTICS** (Input / output level at VSS = 0 V, VDD = 2.6 V~3.3V, Ta = −30~70°C)

Symbol	Item	Condition	Min	Typ	Max	Unit	Applicable Pins
V <sub>IH</sub>	High-level input voltage	CMOS compliant schmitt	1.4	–	–	V	SCL, SDA
V <sub>IL</sub>	Low-level input voltage		–	–	0.4	V	
V <sub>OL</sub>	Low-level output voltage	IOL = 2 mA	–	–	0.2	V	SDA

**Table 6. DRIVER OUTPUT (OUT1, OUT2)** (VSS = 0 V, VDD = 2.8 V, Ta = 25°C)

Symbol	Item	Condition	Min	Typ	Max	Unit	Applicable Pins
I <sub>full</sub>	Maximum current		142.5	150	157.5	mA	OUT1, OUT2

**Table 7. NON-VOLATILE MEMORY CHARACTERISTICS**

Symbol	Item	Condition	Min	Typ	Max	Unit	Applicable Circuit
EN	Endurance		–	–	1000	Cycles	EEPROM
RT	Data retention		10	–	–	Years	
tWT	Write time		–	–	20	ms	

## AC CHARACTERISTICS

### VDD Supply Timing

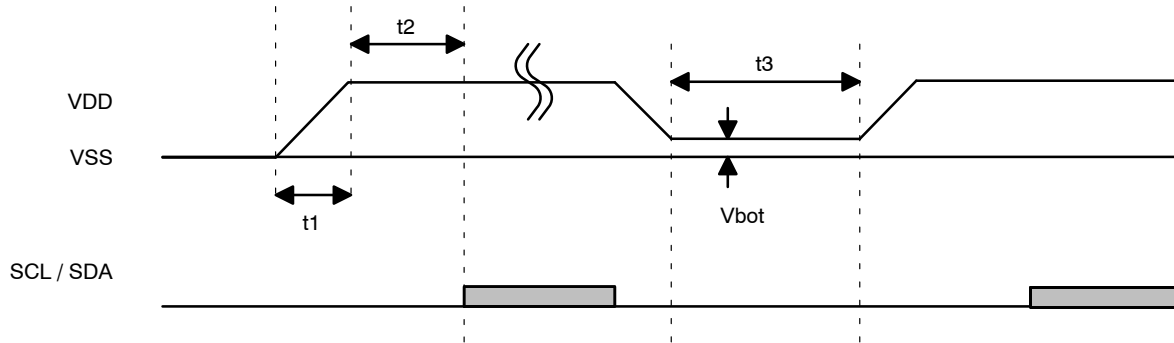


Figure 4. VDD Supply Timing

It is available to use 2-wire serial interface 5ms later for Power On Reset of VDD.

Table 8. VDD SUPPLY TIMING

Symbol	Item	Min	Typ	Max	Unit
t1	VDD turn on time	–	–	3	ms
t2	2-wire serial interface start time from VDD on	5	–	–	ms
t3	VDD off time	100	–	–	ms
Vbot	Bottom Voltage	–	–	0.1	V

### AC Specification

Figure 5 shows interface timing definition and Table 9 shows electric characteristics.

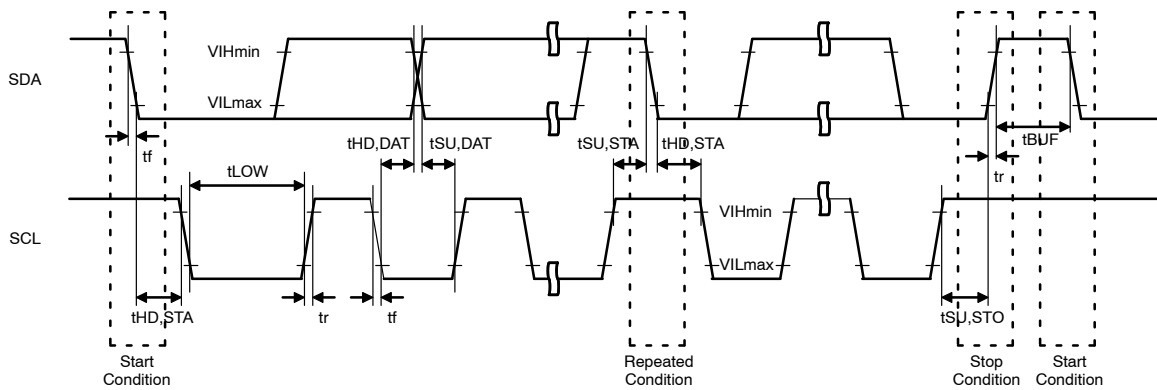


Figure 5. 2-wire Serial Interface Timing Definition

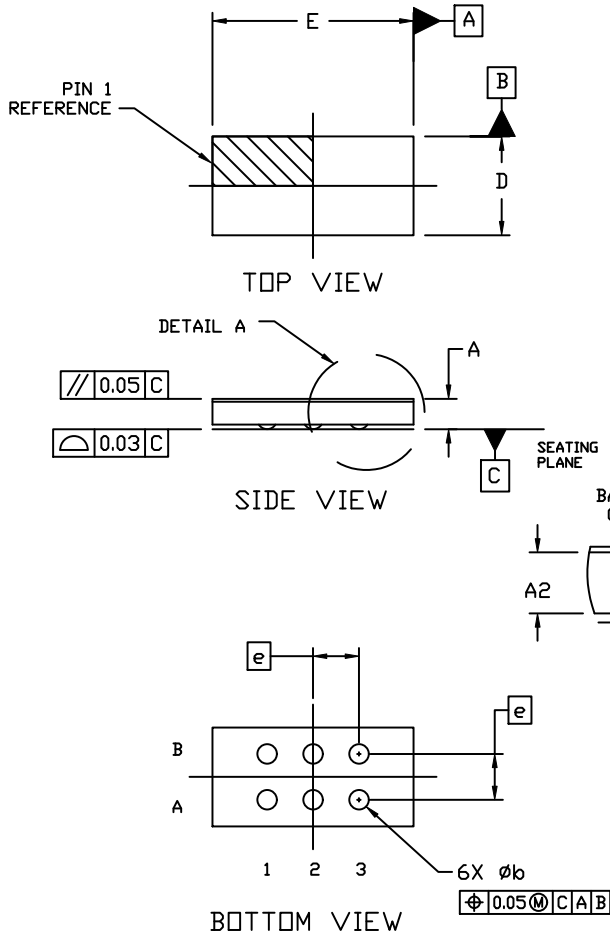
**Table 9. ELECTRICAL CHARACTERISTICS FOR 2-WIRE SERIAL INTERFACE (AC CHARACTERISTICS)**

Symbol	Item	Pin Name	Fast-mode			Fast-mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
F <sub>SCL</sub>	SCL clock frequency	SCL	–	–	400	–	–	1000	kHz
t <sub>HD,STA</sub>	START condition hold time	SCL SDA	0.6	–	–	0.26	–	–	μs
t <sub>LOW</sub>	SCL clock Low period	SCL	1.3	–	–	0.5	–	–	μs
t <sub>HIGH</sub>	SCL clock High period	SCL	0.6	–	–	0.26	–	–	μs
t <sub>SU,STA</sub>	Setup time for repetition START condition	SCL SDA	0.6	–	–	0.26	–	–	μs
t <sub>HD,DAT</sub>	Data hold time	SCL SDA	0 (Note 1)	–	0.9	0 (Note 1)	–	–	μs
t <sub>SU,DAT</sub>	Data setup time	SCL SDA	100	–	–	50	–	–	ns
t <sub>r</sub>	SDA, SCL rising time	SCL SDA	–	–	300	–	–	120	ns
t <sub>f</sub>	SDA, SCL falling time	SCL SDA	–	–	300	–	–	120	ns
t <sub>SU,STO</sub>	STOP condition setup time	SCL SDA	0.6	–	–	0.26	–	–	μs
t <sub>BUF</sub>	Bus free time between STOP and START	SCL SDA	1.3	–	–	0.5	–	–	μs

1. This LSI is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

**WLCSP6, 0.86x1.75x0.265**  
CASE 567XD  
ISSUE O

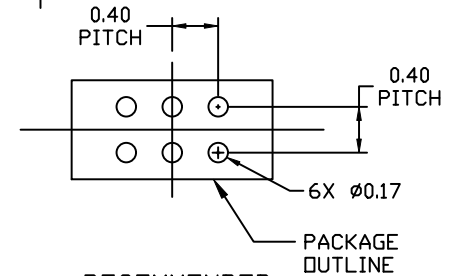
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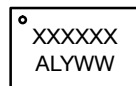
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION  $b$  IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.24	0.265	0.29
A1	0.04 REF		
A2	0.20 REF		
A3	0.025 REF		
$b$	0.12	0.17	0.22
D	0.81	0.86	0.91
E	1.70	1.75	1.80
$e$	0.40 BSC		


**RECOMMENDED MOUNTING FOOTPRINT\***

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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