# MBRB3030CTLG, NRVBB3030CTLG

# Switch-mode Power Rectifier

These state−of−the−art devices use the Schottky Barrier principle with a proprietary barrier metal.

### Features

- Dual Diode Construction, May be Paralleled for Higher Current Output
- Guard−Ring for Stress Protection
- Low Forward Voltage Drop
- 125°C Operating Junction Temperature
- Maximum Die Size
- Short Heat Sink Tab Manufactured − Not Sheared!
- AEC−Q101 Qualified and PPAP Capable
- NRVBB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- All Packages are Pb−Free*

### Mechanical Characteristics

- Case: Epoxy, Molded, Epoxy Meets UL 94 V−0
- Weight: 1.7 Grams (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Device Meets MSL1 Requirements
- ESD Ratings:
  - Machine Model = C (> 400 V)
  - Human Body Model = 3B (> 8000 V)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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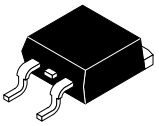
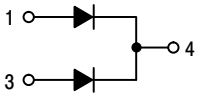
**http://onsemi.com**

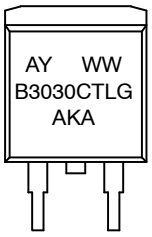
## SCHOTTKY BARRIER RECTIFIER 30 AMPERES, 30 VOLTS



**D²PAK**
**CASE 418B**
**PLASTIC**




### MARKING DIAGRAM




| | |
|---|---|
| A | = Assembly Location |
| Y | = Year |
| WW | = Work Week |
| B3030CTL | = Device Code |
| G | = Pb−Free Package |
| AKA | = Diode Polarity |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MBRB3030CTLG | D²PAK (Pb−Free) | 50 Units / Rail |
| NRVBB3030CTLG | D²PAK (Pb−Free) | 50 Units / Rail |
| NRVBB3030CTLT4G | D²PAK (Pb−Free) | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>Working Peak Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_{RWM}$<br>$V_R$ | 30 | V |
| Average Rectified Forward Current<br>(At Rated $V_R$, $T_C$ = 115°C) Per Device | $I_O$ | 15<br>30 | A |
| Peak Repetitive Forward Current<br>(At Rated $V_R$, Square Wave, 20 kHz, $T_C$ = 115°C) | $I_{FRM}$ | 30 | A |
| Non−Repetitive Peak Surge Current<br>(Surge Applied at Rated Load Conditions Halfwave, Single Phase, 60 Hz) | $I_{FSM}$ | 300 | A |
| Peak Repetitive Reverse Surge Current (1.0 μs, 1.0 kHz) | $I_{RRM}$ | 2.0 | A |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | −55 to +125 | °C |
| Voltage Rate of Change<br>(Rated $V_R$, $T_J$ = 25°C) | dV/dt | 10,000 | V/μs |
| Reverse Energy, Unclamped Inductive Surge ($T_J$ = 25°C, L = 3.0 mH) | $E_{AS}$ | 224.5 | mJ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## THERMAL CHARACTERISTICS (All device data is “Per Leg” except where noted.)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Ambient (Note 1) | $R_{\theta JA}$ | 50 | °C/W |
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 1.0 | °C/W |

1. Mounted using minimum recommended pad size on FR−4 board.

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Maximum Instantaneous Forward Voltage (Note 2)<br>($I_F$ = 15 A, $T_J$ = 25°C)<br>($I_F$ = 30 A, $T_J$ = 25°C) | $V_F$ | 0.44<br>0.51 | V |
| Maximum Instantaneous Reverse Current (Note 2)<br>(Rated $V_R$, $T_J$ = 25°C)<br>(Rated $V_R$, $T_J$ = 125°C) | $I_R$ | 2.0<br>195 | mA |

2. Pulse Test: Pulse Width = 250 μs, Duty Cycle ≤ 2.0%.

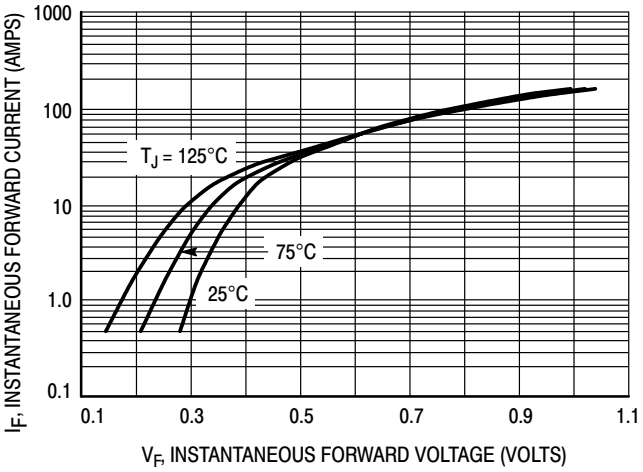



**Figure 1. Typical Forward Voltage**

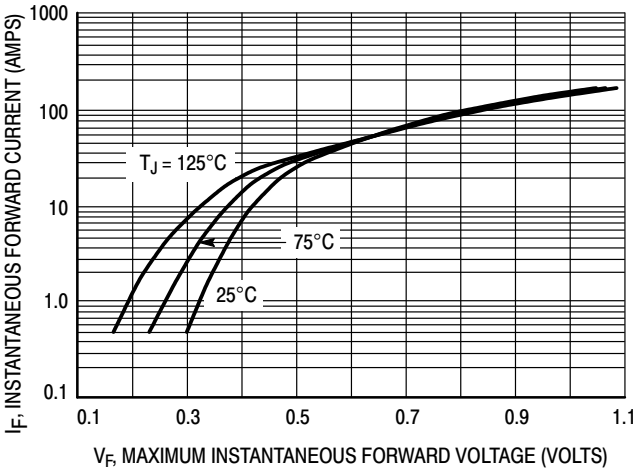



**Figure 2. Maximum Forward Voltage**

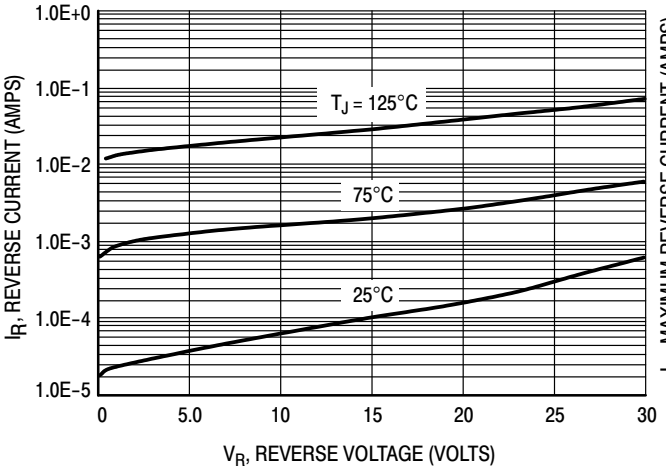



**Figure 3. Typical Reverse Current**

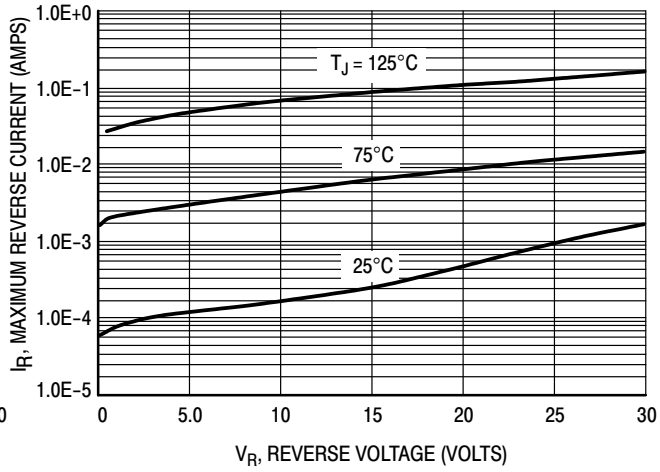



**Figure 4. Maximum Reverse Current**

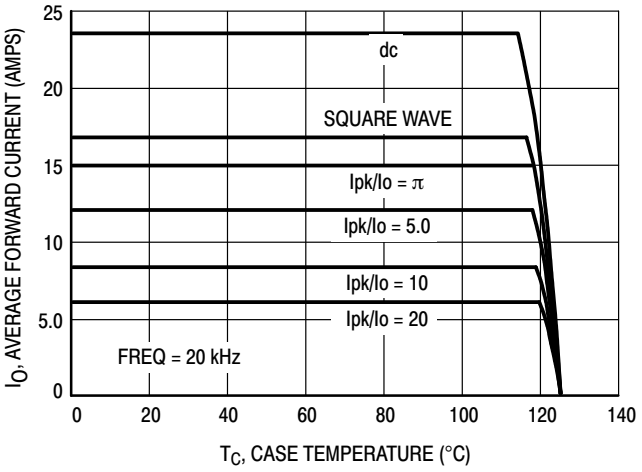



**Figure 5. Current Derating**

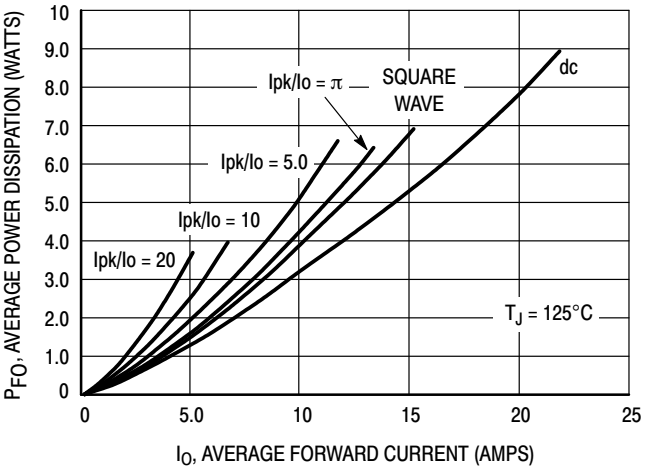



**Figure 6. Forward Power Dissipation**

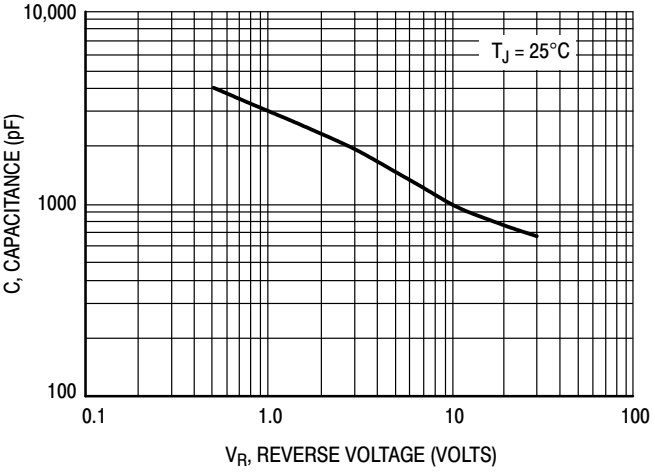



**Figure 7. Typical Capacitance**

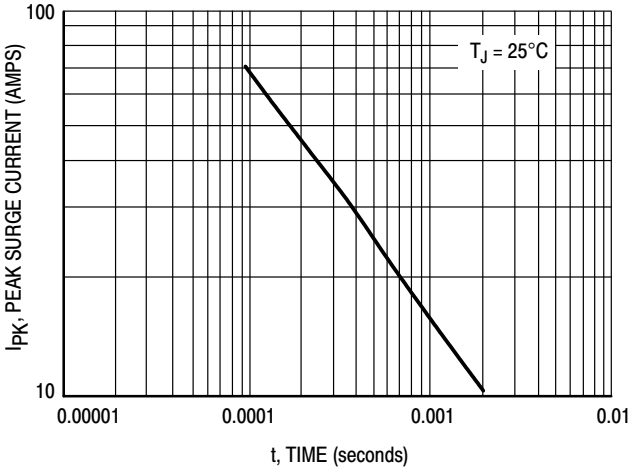



**Figure 8. Typical Unclamped Inductive Surge**

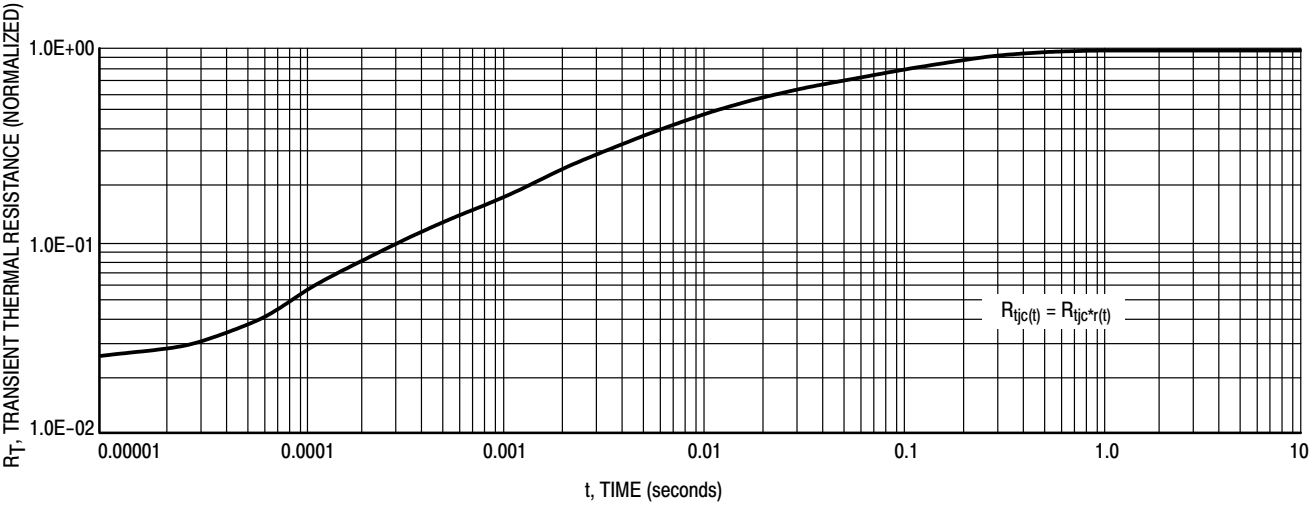



**Figure 9. Typical Thermal Response**

# Modeling Reverse Energy Characteristics of Power Rectifiers


## ABSTRACT

Power semiconductor rectifiers are used in a variety of applications where the reverse energy requirements often vary dramatically based on the operating conditions of the application circuit. A characterization method was devised using the Unclamped Inductive Surge (UIS) test technique. By testing at only a few different operating conditions (i.e. different inductor sizes) a safe operating range can be established for a device. A relationship between peak avalanche current and inductor discharge time was established. Using this relationship and circuit parameters, the part applicability can be determined. This technique offers a power supply designer the total operating conditions for a device as opposed to the present single−data−point approach.


## INTRODUCTION

In today's modern power supplies, converters and other switching circuitry, large voltage spikes due to parasitic inductance can propagate throughout the circuit, resulting in catastrophic device failures. Concurrent with this, in an effort to provide low−loss power rectifiers, i.e., devices with lower forward voltage drops, Schottky technology is being applied to devices used in this switching power circuitry. This technology lends itself to lower reverse breakdown voltages. This combination of high voltage spikes and low reverse breakdown voltage devices can lead to reverse energy destruction of power rectifiers in their applications. This phenomena, however, is not limited to just Schottky technology.

In order to meet the challenges of these situations, power semiconductor manufacturers attempt to characterize their devices with respect to reverse energy robustness. The typical reverse energy specification, if provided at all, is usually given as energy−to−failure (mJ) with a particular inductor specified for the UIS test circuit. Sometimes the peak reverse test current is also specified. Practically all reverse energy characterizations are performed using the UIS test circuit shown in Figure 10. Typical UIS voltage and current waveforms are shown in Figure 11.

In order to provide the designer with a more extensive characterization than the above mentioned one−point approach, a more comprehensive method for characterizing these devices was developed. A designer can use the given information to determine the appropriateness and safe operating area (SOA) of the selected device.

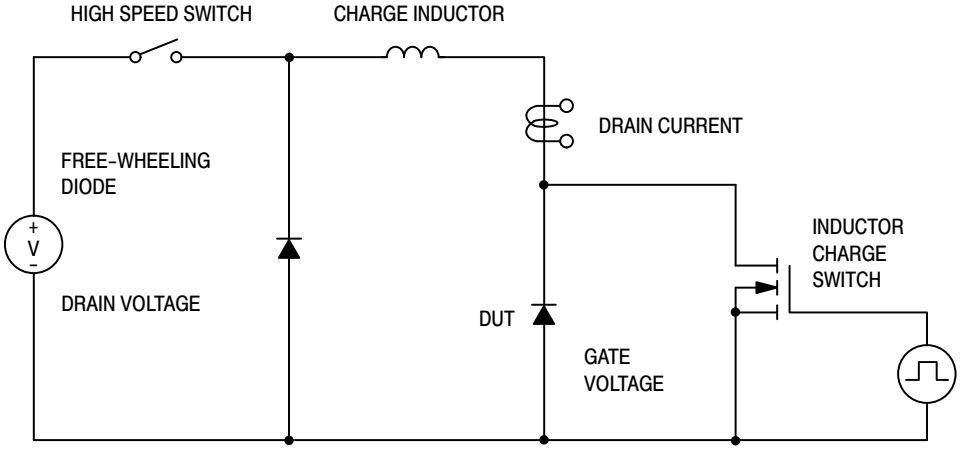



**Figure 10. Simplified UIS Test Circuit**

### Suggested Method of Characterization

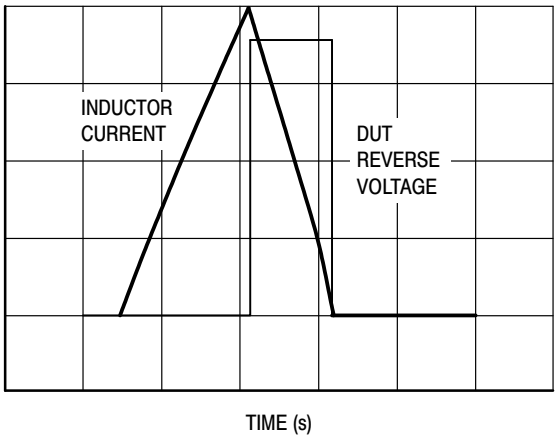



**Figure 11. Typical Voltage and Current UIS Waveforms**

Utilizing the UIS test circuit in Figure 10, devices are tested to failure using inductors ranging in value from 0.01 to 159 mH. The reverse voltage and current waveforms are acquired to determine the exact energy seen by the device and the inductive current decay time. At least 4 distinct inductors and 5 to 10 devices per inductor are used to generate the characteristic current versus time relationship. This relationship when coupled with the application circuit conditions, defines the SOA of the device uniquely for this application.

### Example Application

The device used for this example was an MBR3035CT, which is a 30 A (15 A per side) forward current, 35 V reverse breakdown voltage rectifier. All parts were tested to destruction at 25°C. The inductors used for the characterization were 10, 3.0, 1.0 and 0.3 mH. The data recorded from the testing were peak reverse current (Ip), peak reverse breakdown voltage (BVR), maximum withstand energy, inductance and inductor discharge time (see Table 1). A plot of the Peak Reverse Current versus Time at device destruction, as shown in Figure 12, was generated. The area under the curve is the region of lower reverse energy or lower stress on the device. This area is known as the safe operating area or SOA.

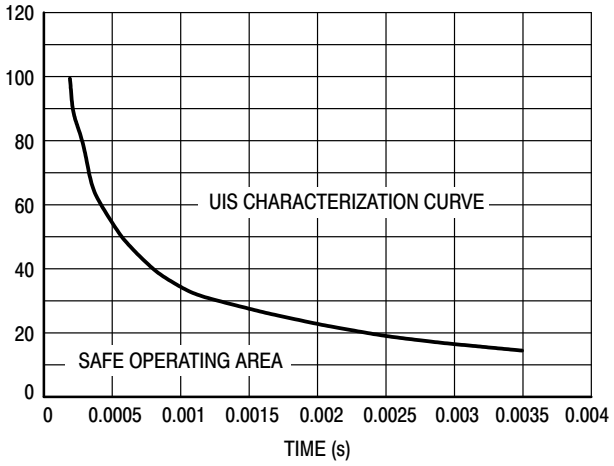



**Figure 12. Peak Reverse Current versus Time for DUT**

**Table 1. UIS Test Data**

| PART NO. | $I_P$ (A) | $B_{VR}$ (V) | ENERGY (mJ) | L (mH) | TIME (μs) |
|---|---|---|---|---|---|
| 1 | 46.6 | 65.2 | 998.3 | 1 | 715 |
| 2 | 41.7 | 63.4 | 870.2 | 1 | 657 |
| 3 | 46.0 | 66.0 | 1038.9 | 1 | 697 |
| 4 | 42.7 | 64.8 | 904.2 | 1 | 659 |
| 5 | 44.9 | 64.8 | 997.3 | 1 | 693 |
| 6 | 44.1 | 64.1 | 865.0 | 1 | 687 |
| 7 | 26.5 | 63.1 | 1022.6 | 3 | 1261 |
| 8 | 26.4 | 62.8 | 1024.9 | 3 | 1262 |
| 9 | 24.4 | 62.2 | 872.0 | 3 | 1178 |
| 10 | 27.6 | 62.9 | 1091.0 | 3 | 1316 |
| 11 | 27.7 | 63.2 | 1102.4 | 3 | 1314 |
| 12 | 17.9 | 62.6 | 1428.6 | 10 | 2851 |
| 13 | 18.9 | 62.1 | 1547.4 | 10 | 3038 |
| 14 | 18.8 | 60.7 | 1521.1 | 10 | 3092 |
| 15 | 19.0 | 62.6 | 1566.2 | 10 | 3037 |
| 16 | 74.2 | 69.1 | 768.4 | 0.3 | 322 |
| 17 | 77.3 | 69.6 | 815.4 | 0.3 | 333 |
| 18 | 75.2 | 68.9 | 791.7 | 0.3 | 328 |
| 19 | 77.3 | 69.6 | 842.6 | 0.3 | 333 |
| 20 | 73.8 | 69.1 | 752.4 | 0.3 | 321 |
| 21 | 75.6 | 69.2 | 823.2 | 0.3 | 328 |
| 22 | 74.7 | 68.6 | 747.5 | 0.3 | 327 |
| 23 | 78.4 | 70.3 | 834.0 | 0.3 | 335 |
| 24 | 70.5 | 66.6 | 678.4 | 0.3 | 317 |
| 25 | 78.3 | 69.4 | 817.3 | 0.3 | 339 |

The procedure to determine if a rectifier is appropriate, from a reverse energy standpoint, to be used in the application circuit is as follows:

a. Obtain “Peak Reverse Current versus Time” curve from data book.
b. Determine steady state operating voltage (OV) of circuit.
c. Determine parasitic inductance (L) of circuit section of interest.
d. Obtain rated breakdown voltage (BVR) of rectifier from data book.
e. From the following relationships,

$$V = L \cdot \frac{d}{dt} i(t) \qquad I = \frac{(BVR - OV) \cdot t}{L}$$

a “designer” I versus t curve is plotted alongside the device characteristic plot.
f. The point where the two curves intersect is the current level where the devices will start to fail. A peak inductor current below this intersection should be chosen for safe operating.

As an example, the values were chosen as L = 200 μH, OV = 12 V and BVR = 35 V.

Figure 13 illustrates the example. Note the UIS characterization curve, the parasitic inductor current curve and the safe operating region as indicated.

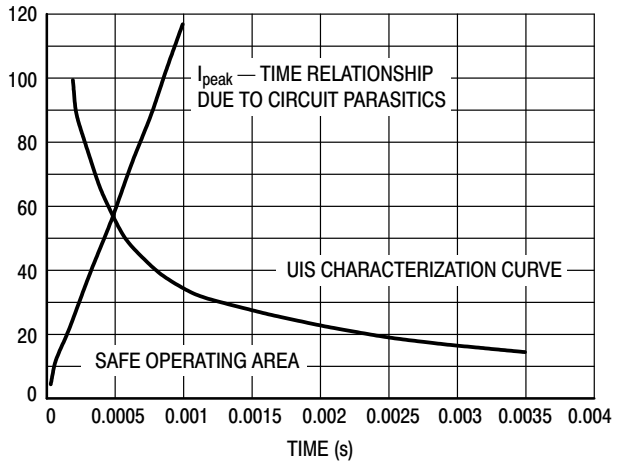


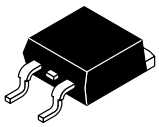

**Figure 13. DUT Peak Reverse and Circuit Parasitic Inductance Current versus Time**

## SUMMARY

Traditionally, power rectifier users have been supplied with single−data−point reverse−energy characteristics by the supplier’s device data sheet; however, as has been shown here and in previous work, the reverse withstand energy can vary significantly depending on the application. What was done in this work was to create a characterization scheme by which the designer can overlay or map their particular requirements onto the part capability and determine quite accurately if the chosen device is applicable. This characterization technique is very robust due to its statistical approach, and with proper guardbanding (6σ) can be used to give worst−case device performance for the entire product line. A “typical” characteristic curve is probably the most applicable for designers allowing them to design in their own margins.

## References

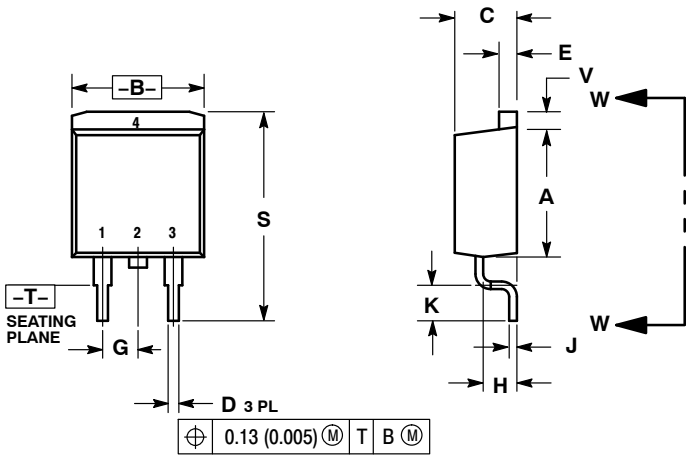
1. Borras, R., Aliosi, P., Shumate, D., 1993, “Avalanche Capability of Today’s Power Semiconductors, “Proceedings, European Power Electronic Conference,” 1993, Brighton, England
2. Pshaenich, A., 1985, “Characterizing Overvoltage Transient Suppressors,” Powerconversion International, June/July



**SCALE 1:1**

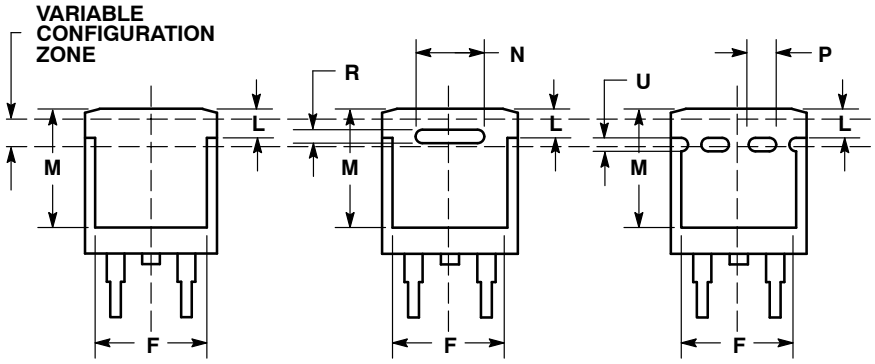
**D²PAK 3**
CASE 418B–04
ISSUE L

DATE 17 FEB 2015




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.340 | 0.380 | 8.64 | 9.65 |
| B | 0.380 | 0.405 | 9.65 | 10.29 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.020 | 0.035 | 0.51 | 0.89 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.310 | 0.350 | 7.87 | 8.89 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.080 | 0.110 | 2.03 | 2.79 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.090 | 0.110 | 2.29 | 2.79 |
| L | 0.052 | 0.072 | 1.32 | 1.83 |
| M | 0.280 | 0.320 | 7.11 | 8.13 |
| N | 0.197 REF | | 5.00 REF | |
| P | 0.079 REF | | 2.00 REF | |
| R | 0.039 REF | | 0.99 REF | |
| S | 0.575 | 0.625 | 14.60 | 15.88 |
| V | 0.045 | 0.055 | 1.14 | 1.40 |




VIEW W–W 1 | VIEW W–W 2 | VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**



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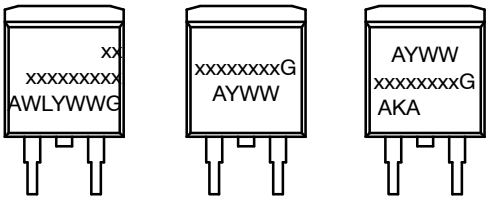
**D²PAK 3**
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

## GENERIC MARKING DIAGRAM*

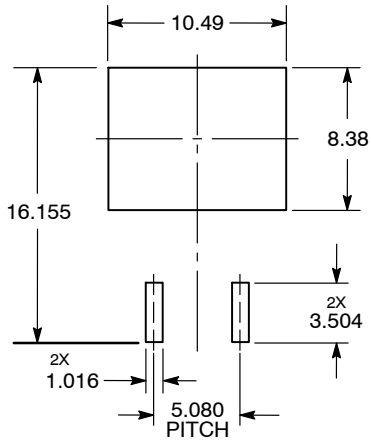



**IC** **Standard** **Rectifier**

| | |
|---|---|
| xx | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |
| AKA | = Polarity Indicator |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

## SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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