

# MC100EL38

## 5 V ECL ÷2, ÷4/6 Clock Generation Chip

### Description

The MC100EL38 is a low skew  $\pm 2$ ,  $\pm 4/6$  clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase\_Out output will go HIGH for one clock cycle whenever the  $\pm 2$  and the  $\pm 4/6$  outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

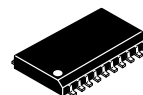
Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the  $\pm 2$  and the  $\pm 4/6$  outputs of a single device.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection:
  - ♦ 2 kV Human Body Model
  - ♦ 100 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:
  - ♦  $V_{CC} = 4.2 \text{ V to } 5.7 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
  - ♦  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -4.2 \text{ V to } -5.7 \text{ V}$
- Internal 75 k $\Omega$  Input Pulldown Resistors on CLK,  $\overline{\text{EN}}$ , MR, and DIVSEL
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test



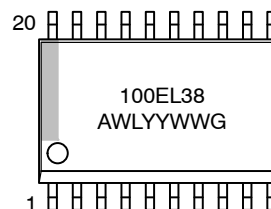
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SOIC-20 WB  
DW SUFFIX  
CASE 751D-05

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*For additional marking information, refer to Application Note [AND8002/D](#).

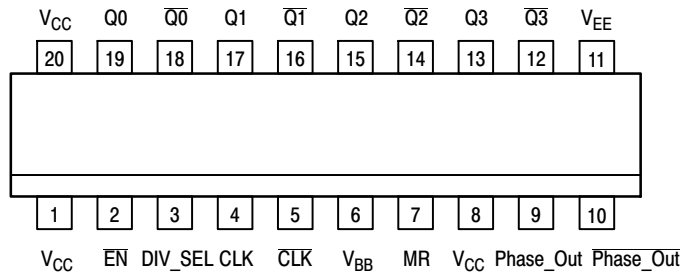
### ORDERING INFORMATION

Device	Package	Shipping†
MC100EL38DWR2G	SOIC-20 WB (Pb-Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

- Moisture Sensitivity Level: 3 (Pb-Free)
  - ♦ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating:
  - ♦ UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 388 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

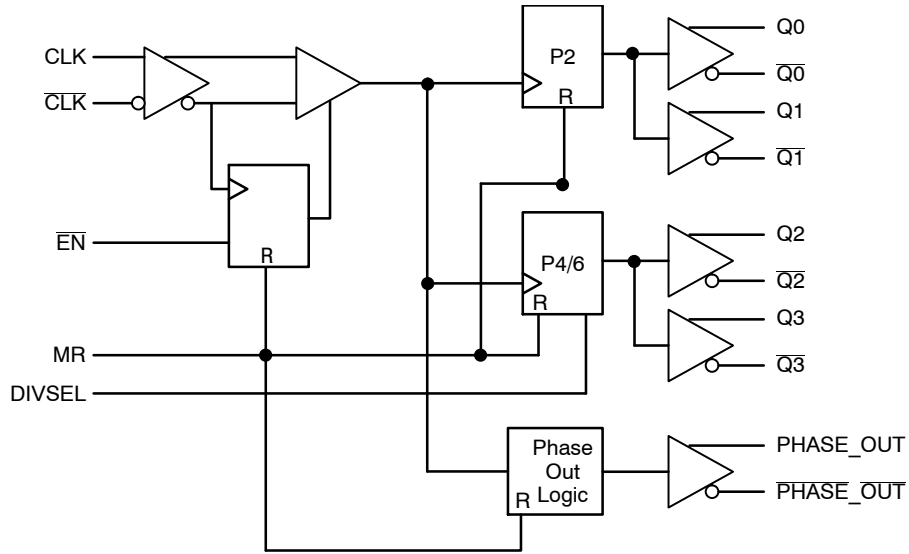
# MC100EL38



\* All V<sub>CC</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Pinout Assignment (Top View)**



**Figure 2. Logic Diagram**

**Table 1. PIN DESCRIPTION**

Pin	Function
CLK, $\overline{\text{CLK}}$	ECL Diff Clock Inputs
Q <sub>0</sub> , Q <sub>1</sub> ; $\overline{\text{Q}}_0$ , $\overline{\text{Q}}_1$	ECL Diff $\pm 2$ Outputs
Q <sub>2</sub> , Q <sub>3</sub> ; $\overline{\text{Q}}_2$ , $\overline{\text{Q}}_3$	ECL Diff $\pm 4/6$ Outputs
$\overline{\text{EN}}$	ECL Sync Enable Input
MR	ECL Master Reset Input
DIVSEL	ECL Frequency Select Input
Phase_Out, $\overline{\text{Phase\_Out}}$	ECL Phase Sync Diff. Signal Output
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

**Table 2. FUNCTION TABLE**

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q <sub>0-3</sub>
X	X	H	Reset Q <sub>0-3</sub>

Z = Low-to-High Transition  
 ZZ = High-to-Low Transition  
 X = Don't Care

DIVSEL	Q <sub>2</sub> , Q <sub>3</sub> OUTPUTS
L	Divide by 4
H	Divide by 6

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB	90 60	$^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder (Pb-Free)	<2 to 3 sec @ 260 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. 100EL SERIES PECL DC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40 $^{\circ}\text{C}$			25 $^{\circ}\text{C}$			85 $^{\circ}\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	60		50	60		54	65	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
$V_{BB}$	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	1.65		4.45	1.65		4.45	1.65		4.45	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

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**Table 5. 100EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	60		50	60		54	65	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	-3.35		-0.55	-3.35		-0.55	-3.35		-0.55	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ;  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and 1 V.

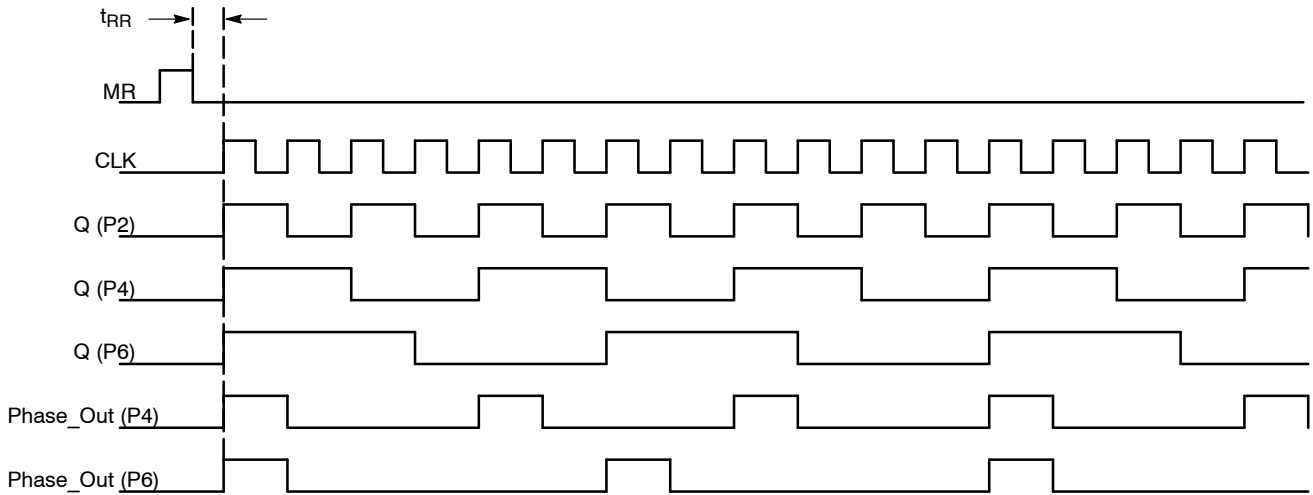
**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output CLK $\rightarrow$ Q (Differential) CLK $\rightarrow$ Q (Single-Ended) CLK $\rightarrow$ Phase_Out (Differential) CLK $\rightarrow$ Phase_Out (Single-Ended) MR $\rightarrow$ Q	810 710 800 750 510		1010 1010 1000 1050 810	850 750 840 790 540		1050 1050 1040 1090 840	900 800 890 840 570		1100 1100 1090 1140 870	ps
$t_{SKEW}$	Within-Device Skew (Note 2) $Q_0 - Q_3$ All			50 75			50 75			50 75	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
	Part-to-Part $Q_0 - Q_3$ (Differential) All			200 240			200 240			200 240	
$t_S$	Setup Time EN $\rightarrow$ CLK DIVSEL $\rightarrow$ CLK		150			150			150		ps
$t_H$	Hold Time CLK $\rightarrow$ EN CLK $\rightarrow$ Div_Sel		150 200			150 200			150 200		ps
$V_{PP}$	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
$t_{RR}$	Reset Recovery Time			100			100			100	ps
$t_{PW}$	Minimum Pulse Width										ps
	CLK MR	800 700			800 700			800 700			
$t_r, t_f$	Output Rise/Fall Times Q (20% - 80%)	280		550	280		550	280		550	ps

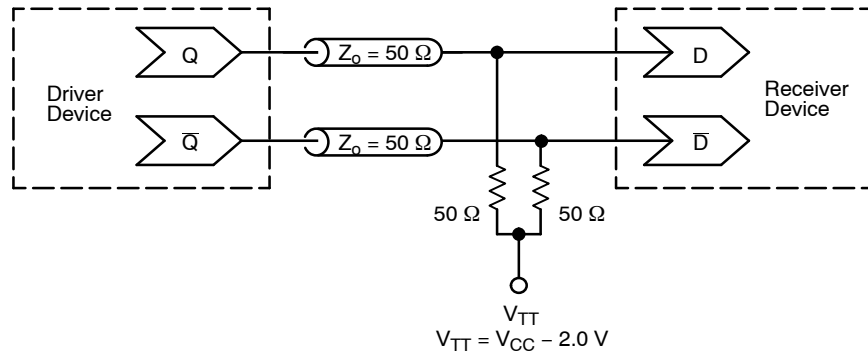
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Skew is measured between outputs under identical transitions.
3.  $V_{PP(min)}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

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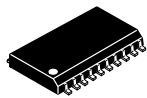
**Figure 3. Timing Diagram**



**Figure 4. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## Resource Reference of Application Notes

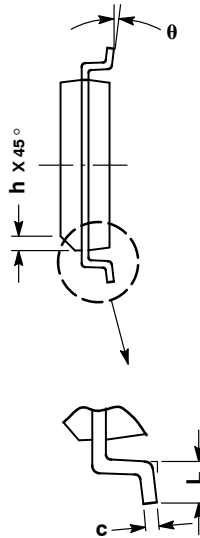
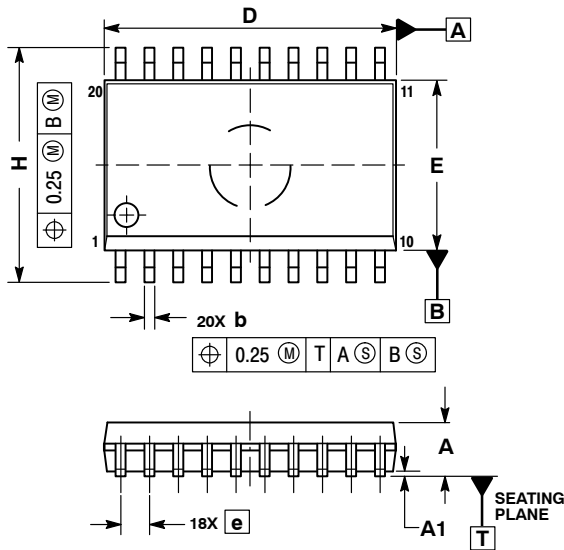
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



SCALE 1:1

SOIC-20 WB  
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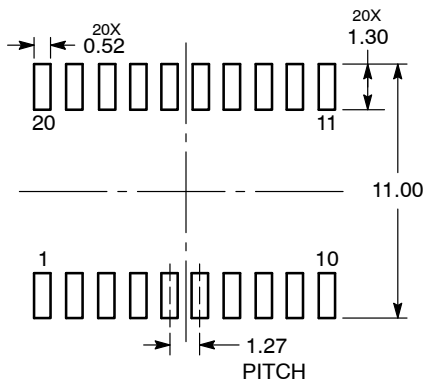


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

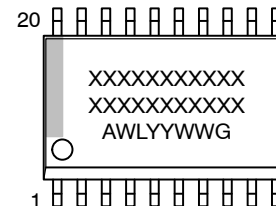
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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