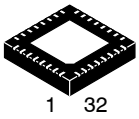
3.3 V/5 V 8-Bit CMOS/ECL/TTL Data Input Parallel/Serial Converter

MC100EP446

LQFP−32
FA SUFFIX
CASE 561AB



QFN32
MN SUFFIX
CASE 488AM

Description

The MC100EP446 is an integrated 8−bit parallel to serial data converter. The device is designed with unique circuit topology to operate for NRZ data rates up to 3.2 Gb/s. The conversion sequence from parallel data into a serial data stream is from bit D0 to D7. The parallel input pins D0−D7 are configurable to be threshold controlled by CMOS, ECL, or TTL level signals. The serial data rate output can be selected at internal clock data rate or twice the internal clock data rate using the CKSEL pin.

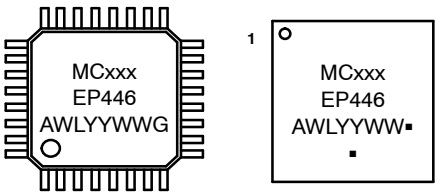
Control pins are provided to reset (SYNC) and disable internal clock circuitry (CKEN). In either CKSEL modes, the internal flip−flops are triggered on the rising edge for CLK and the multiplexers are switched on the falling edge of CLK, therefore, all associated specification limits are referenced to the negative edge of the clock input. Additionally, V_{BB} pin is provided for single−ended input condition.

The 100 Series devices contain temperature compensation network.

Features

- 3.2 Gb/s Typical Data Rate Capability
- Differential Clock and Serial Outputs
- V_{BB} Output for Single-ended Input Applications
- Asynchronous Data Reset (SYNC)
- PECL Mode Operating Range:
  V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Parallel Interface Can Support PECL, TTL or CMOS
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAM



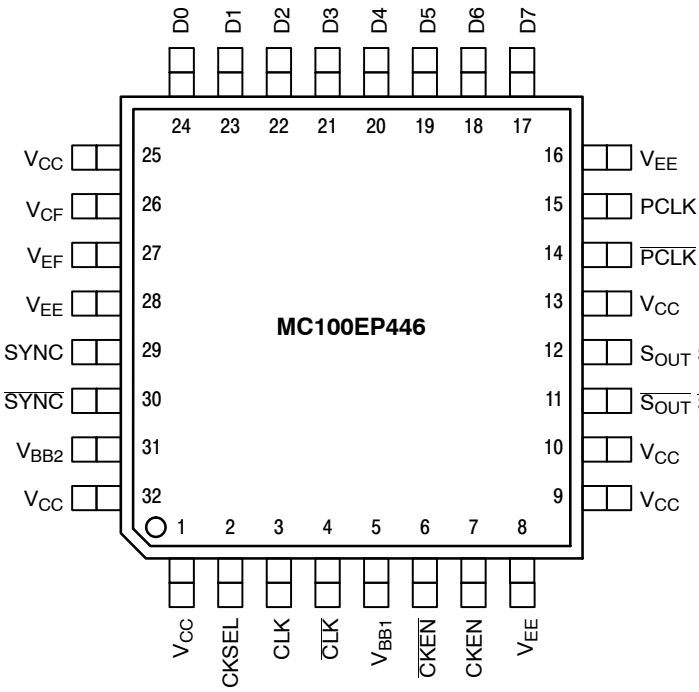
xxx	= 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP−32 Pinout (Top View)

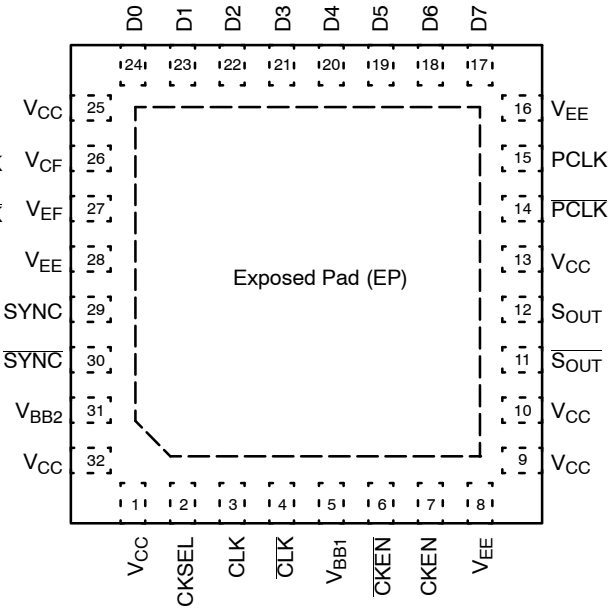


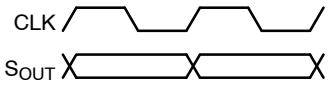
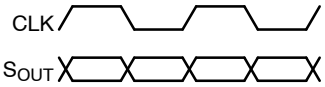
Figure 2. QFN−32 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0*−D7*	ECL, CMOS, or TTL Parallel Data Input
S_{OUT}, $\overline{S_{OUT}}$	ECL Differential Serial Data Output
CLK*, $\overline{CLK}$*	ECL Differential Clock Input
PCLK, $\overline{PCLK}$	ECL Differential Parallel Clock Output
SYNC*, $\overline{SYNC}$**	ECL Conversion Synchronizing Differential Input (Reset)***
CKSEL*	ECL Clock Input Selector
CKEN*, $\overline{CKEN}$*	ECL Clock Enable Differential Input
V_{CF}	ECL, CMOS, or TTL Input Selector
V_{EF}	ECL Reference Mode Connection
V_{BB1}, V_{BB2}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.
**Pins will default HIGH when left open.
***The rising edge of SYNC will asynchronously reset the internal circuitry. The falling edge of the SYNC followed by the falling edge of CLK initiates the conversion process synchronously on the next rising edge of CLK.

Table 2. TRUTH TABLE

Pin	Function	
	HIGH	LOW
CKSEL	S_{OUT}: PCLK = 8:1 CLK: S_{OUT} = 1:1 	S_{OUT}: PCLK = 8:1 CLK: S_{OUT} = 1:2 
CKEN	Synchronously Disables Normal Parallel to Serial Conversion	Synchronously Enables Normal Parallel to Serial Conversion
SYNC	Asynchronously Resets Internal Flip−Flops*	Synchronous Enable

*The rising edge of SYNC will asynchronously reset the internal circuitry. The falling edge of the SYNC followed by the falling edge of CLK initiates the conversion process synchronously on the next rising edge of CLK.

Table 3. INPUT VOLTAGE LEVEL SELECTION TABLE

Input Function	Connect To V_{CF} Pin
ECL Mode	V_{EF} Pin
CMOS Mode	No Connect
TTL Mode*	1.5 V ± 100 mV

*For TTL Mode, if no external voltage can be provided, the reference voltage can be provided by connecting the appropriate resistor between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT OPERATING VOLTAGE TABLE

Power Supply (V_{CC},V_{EE})	Data Inputs (D [0:7])			
	CMOS	TTL	PECL	NECL
PECL	√	√	√	N/A
NECL	N/A	N/A	N/A	√

Power Supply	Resistor Value 10% (Tolerance)
3.3 V	1.5 kΩ
5.0 V	500 Ω

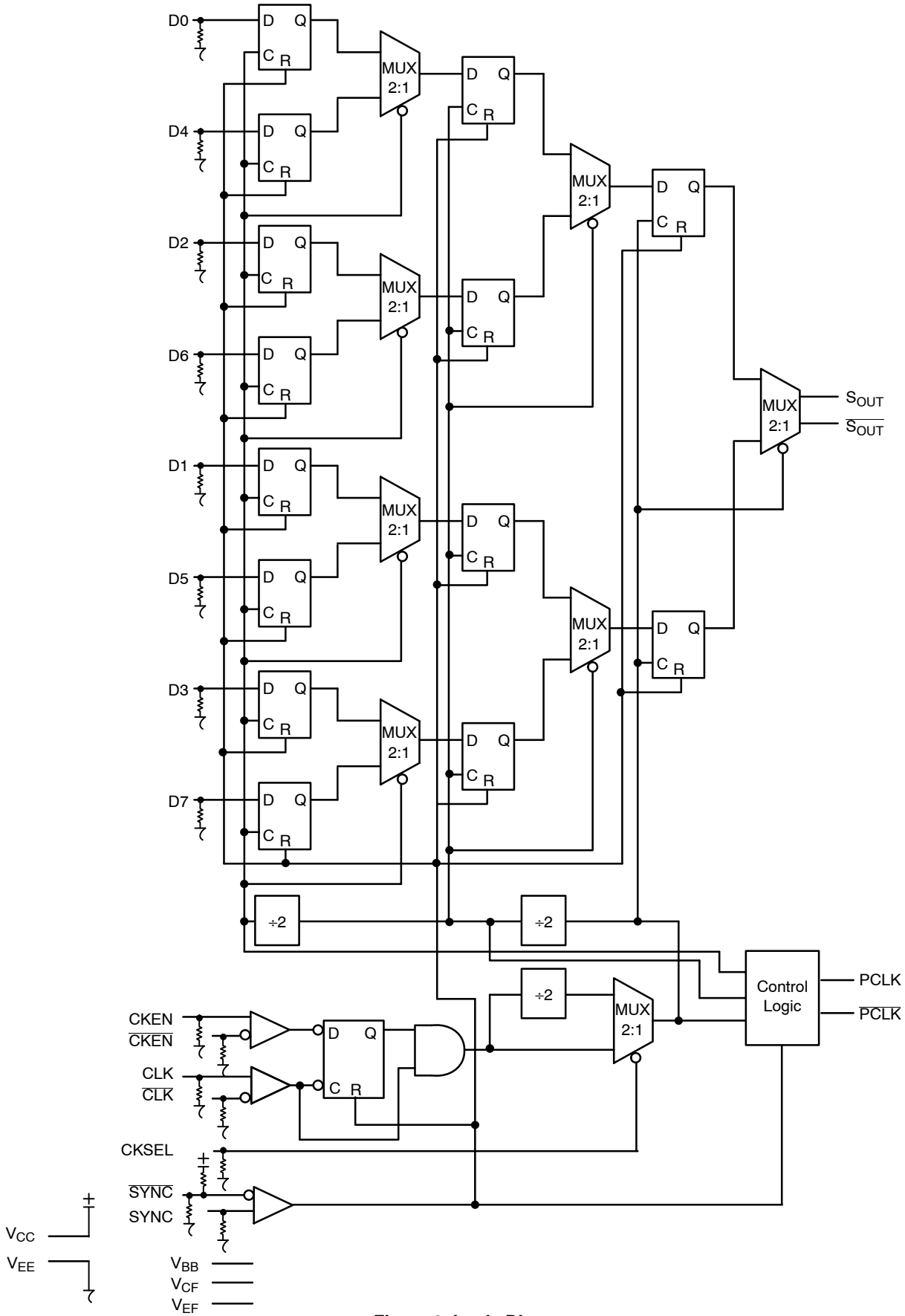


Figure 3. Logic Diagram

Table 5. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	LQFP−32 QFN−32	Level 2 −	Level 2 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		962 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 6. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	LQFP−32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder Pb−Free	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 7. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
V_{OH}	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 3)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single−Ended) CMOS PECL TTL	 2000 2075 2000		 3300 3300 3300	 2000 2075 2000		 3300 3300 3300	 2000 2075 2000		 3300 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) CMOS PECL TTL	 0 1305 0		 800 1675 800	 0 1305 0		 800 1675 800	 0 1305 0		 800 1675 800	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
3. All loading with 50 Ω to V_{CC} − 2.0 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. 100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
V_{OH}	Output HIGH Voltage (Note 6)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 6)	3005	3180	3305	3005	3180	3305	3005	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single−Ended) CMOS PECL TTL	 3500 3775 2000		 5000 5000 5000	 3500 3775 2000		 5000 5000 5000	 3500 3775 2000		 5000 5000 5000	mV
V_{IL}	Input LOW Voltage (Single−Ended) CMOS PECL TTL	 0 3005 0		 1500 3375 800	 0 3005 0		 1500 3375 800	 0 3005 0		 1500 3375 800	mV
V_{BB}	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
6. All loading with 50 Ω to V_{CC} − 2.0 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 8)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	90	110	130	90	110	130	95	115	135	mA
V_{OH}	Output HIGH Voltage (Note 9)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 9)	−1995	−1820	−1695	−1995	−1820	−1695	−1995	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1995		−1625	−1995		−1625	−1995		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. Input and output parameters vary 1:1 with V_{CC}.
9. All loading with 50 Ω to V_{CC} − 2.0 V.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 10. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 11)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 15) CKSEL High CKSEL Low	 3.2 1.6	 3.4 1.7		 3.2 1.6	 3.4 1.7		 3.2 1.6	 3.4 1.7		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CKSEL = 0 CLK TO S_{OUT}, CLK TO PCLK	 650 700	 750 800	 850 900	 700 750	 800 850	 900 950	 725 775	 850 900	 975 1025	ps
	CKSEL = 1 CLK TO S_{OUT}, CLK TO PCLK	775 850	875 950	975 1050	825 900	925 1000	1025 1100	875 950	1000 1075	1125 1200	ps
t_S	Setup Time D to CLK+ (Figure 4) SYNC− to CLK− (Figure 5) CKEN+ to CLK− (Figure 6)	 −375 200 70	 −425 140 40		 −400 200 70	 −450 140 40		 −450 200 70	 −500 140 40		ps
t_h	Hold Time D to CLK+ (Figure 4) SYNC− to CLK− CLK− to CKEN− (Figure 6)	 −525 0 75	 −575 45		 −550 0 75	 −600 45		 −600 0 75	 −650 45		ps
t_{pw}	Minimum Pulse Width (Note 13) Data (D0−D7) SYNC CKEN	 150 200 145			 150 200 145			 150 200 145			ps
t_{JITTER}	Random Clock Jitter (RMS) ≤ f_{max} Typ		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Differential Voltage Swing (Note 12)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times S_{OUT} (20% − 80%)	50	100	150	70	120	170	90	140	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

11. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
12. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.
13. The minimum pulse width is valid only if the setup and hold times are respected.

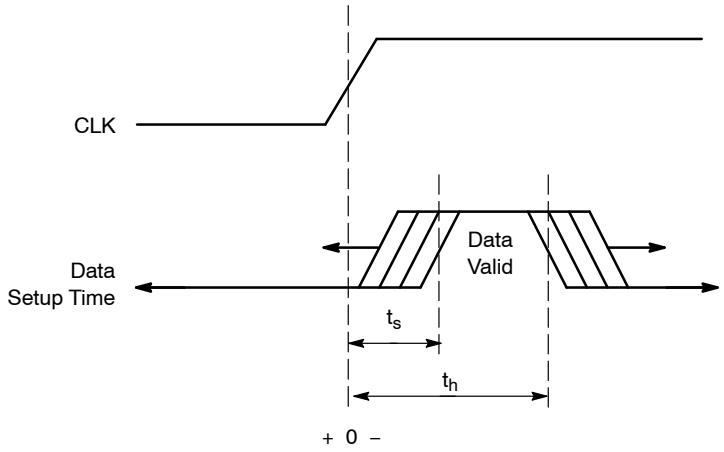


Figure 4. Setup and Hold Time for Data

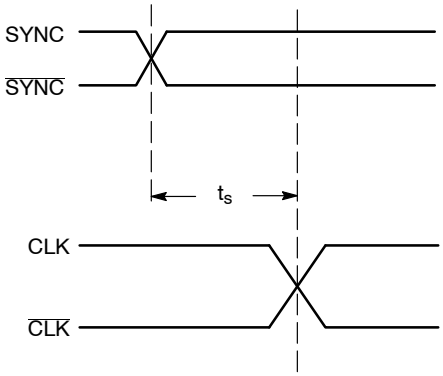


Figure 5. Setup Time for SYNC

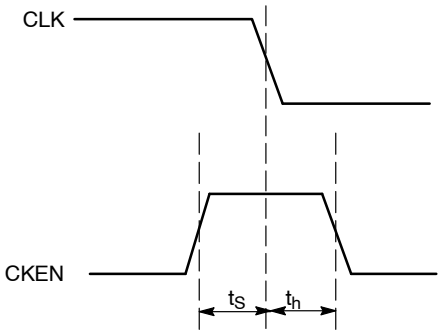


Figure 6. Setup and Hold Time for CKEN

APPLICATION INFORMATION

The MC100EP446 is an integrated 8:1 parallel to serial converter. An attribute for EP446 is that the parallel inputs D0–D7 (Pins 17 – 24) can be configured to accept either CMOS, ECL, or TTL level signals by a combination of interconnects between V_{EF} (Pin 27) and V_{CF} (Pin 26) pins. For CMOS input levels, leave V_{EF} and V_{CF} open. For ECL operation, short V_{CF} and V_{EF} (Pins 26 and 27). For TTL operation, connect a 1.5 V supply reference to V_{CF} and leave the V_{EF} pin open. The 1.5 V reference voltage to V_{CF} pin can be accomplished by placing a 1.5 kΩ or 500 Ω between V_{CF} and V_{EE} for 3.3 V or 5.0 V power supplies, respectively. Note: all pins requiring ECL voltage inputs must have a 50 Ω terminating resistor to V_{TT} ($V_{TT} = V_{CC} – 2.0$ V).

The CKSEL input (Pin 2) is provided to enable the user to select the serial data rate output between internal clock data rate or twice the internal clock data rate. For CKSEL LOW operation, the time from when the parallel data is latched ① to when the data is seen on the S_{OUT} ② is on the falling edge of the 7th clock cycle plus internal propagation delay (Figure 7). Note the PCLK switches on the falling edge of CLK.

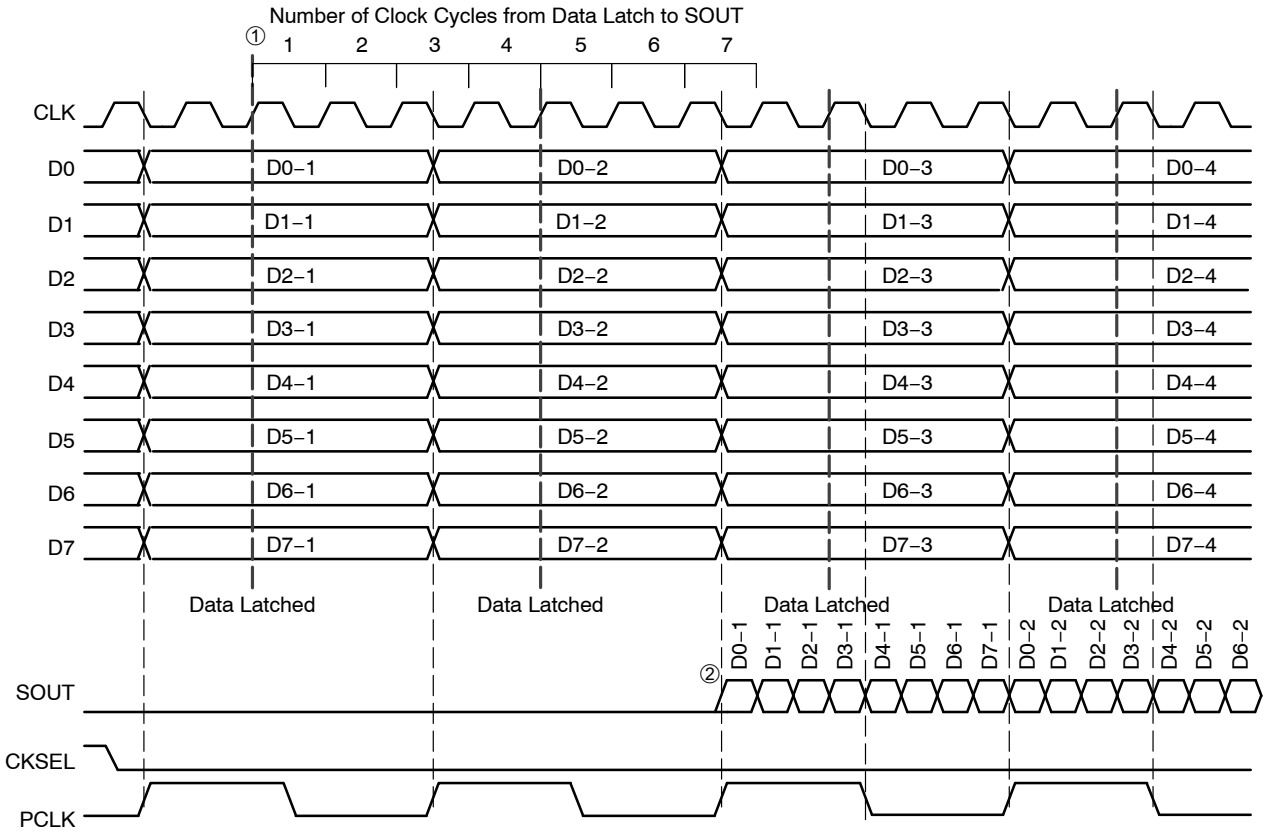


Figure 7. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL LOW

Similarly, for CKSEL HIGH operation, the time from when the parallel data is latched ① to when the data is seen on the S_{OUT} ② is on the rising edge of the 14th clock cycle plus internal propagation delay (Figure 8). Furthermore, the PCLK switches on the rising edge of CLK.

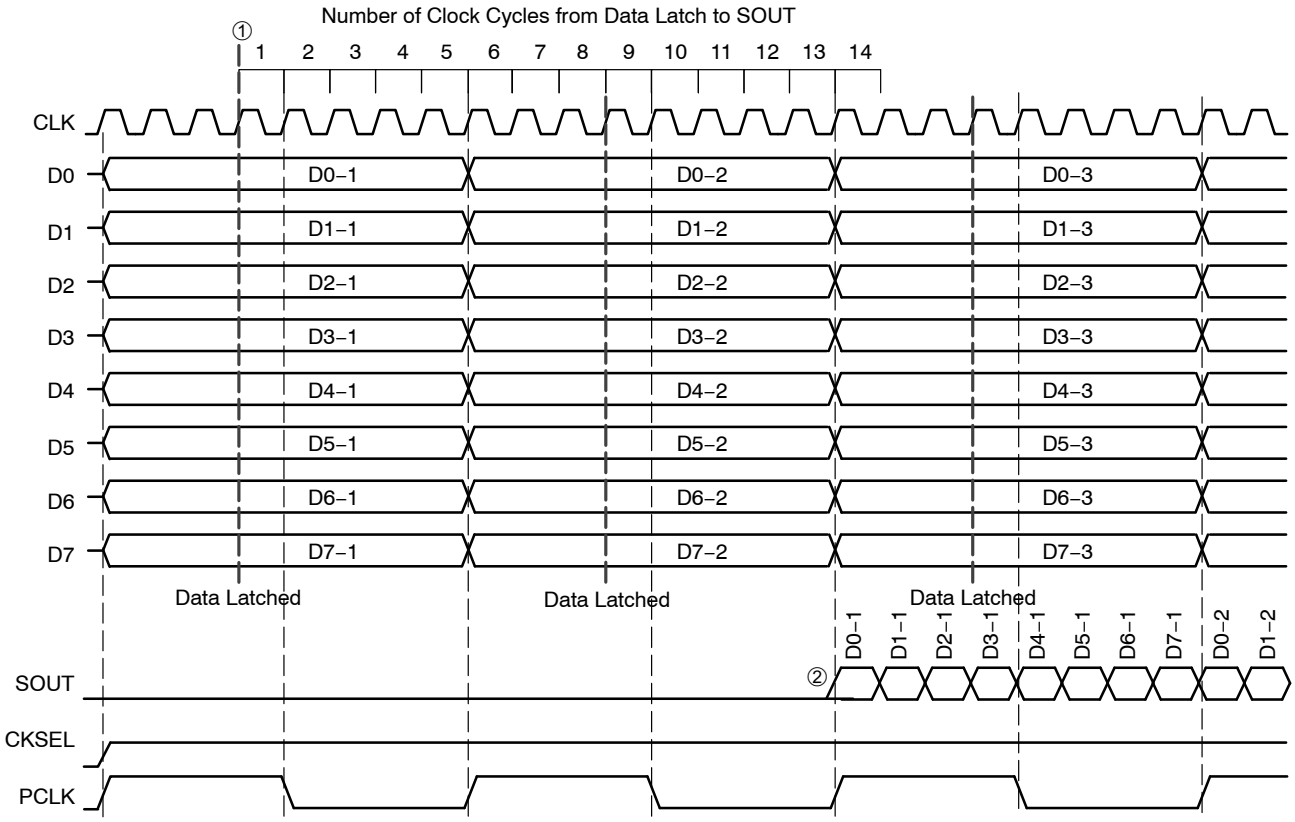


Figure 8. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL HIGH

The device also features a differential SYNC input (Pins 29 and 30), which asynchronously reset all internal flip–flops and clock circuitry on the rising edge of SYNC. The release of SYNC is a synchronous process, which ensures that no runt serial data bits are generated. The falling edge of the SYNC followed by a falling edge of CLK initiates the start of the conversion process on the next rising edge of CLK (Figures 9 and 10). As shown in the figures below, the device will start to latch the parallel input data after the a falling edge of SYNC ①, followed by the falling edge CLK ②, on the next rising of edge of CLK ③ for CKSEL LOW

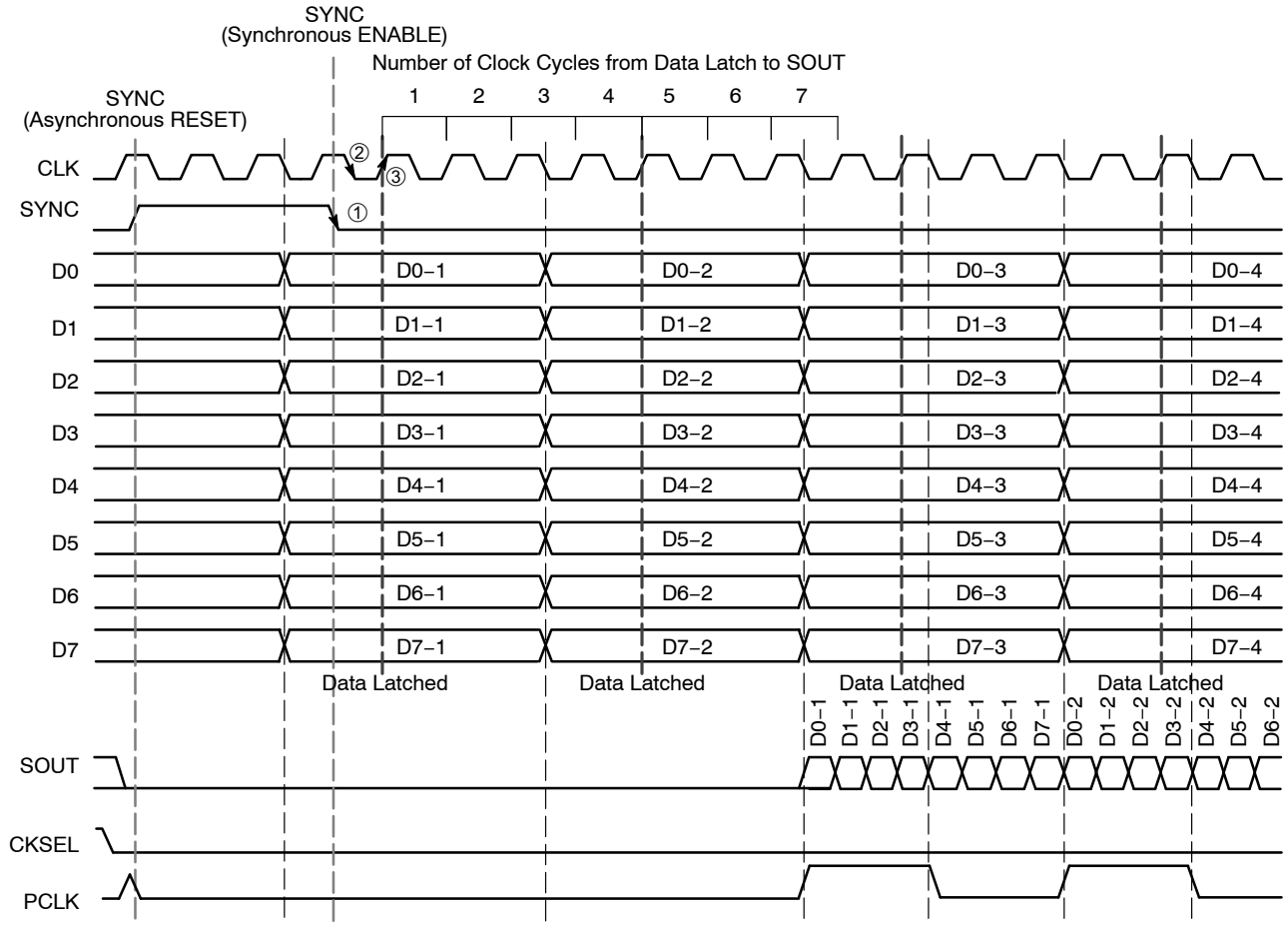


Figure 9. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL LOW and SYNC

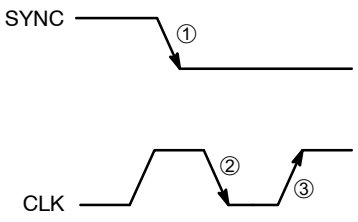


Figure 10. Synchronous Release of SYNC for CKSEL LOW

For CKSEL HIGH, as shown in the timing diagrams below, the device will start to latch the parallel input data after the falling edge of SYNC ①, followed by the falling edge CLK ②, on the second rising edge of CLK ③ (Figures 11 and 12).

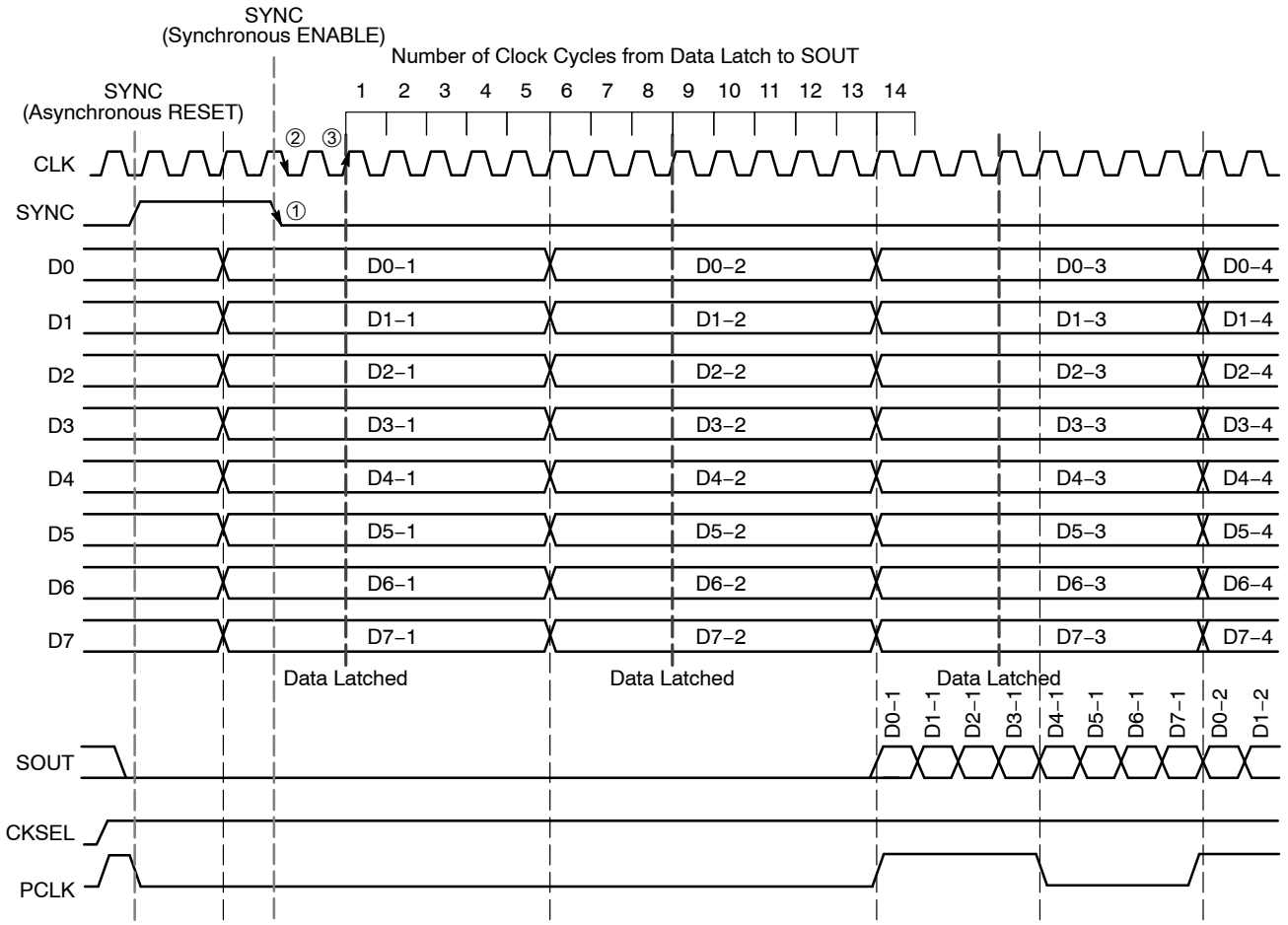


Figure 11. Timing Diagram 1:8 Parallel to Serial Conversion with CKSEL HIGH and SYNC

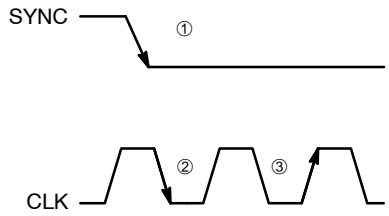


Figure 12. Synchronous Release of SYNC for CKSEL HIGH

The differential synchronous CKEN inputs (Pins 6 and 7), disable the internal clock circuitry. The synchronous CKEN will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of CKEN followed by the falling edge of CLK will suspend all activities. The falling edge of CKEN followed by the falling edge of CLK will resume all activities (Figure 13).

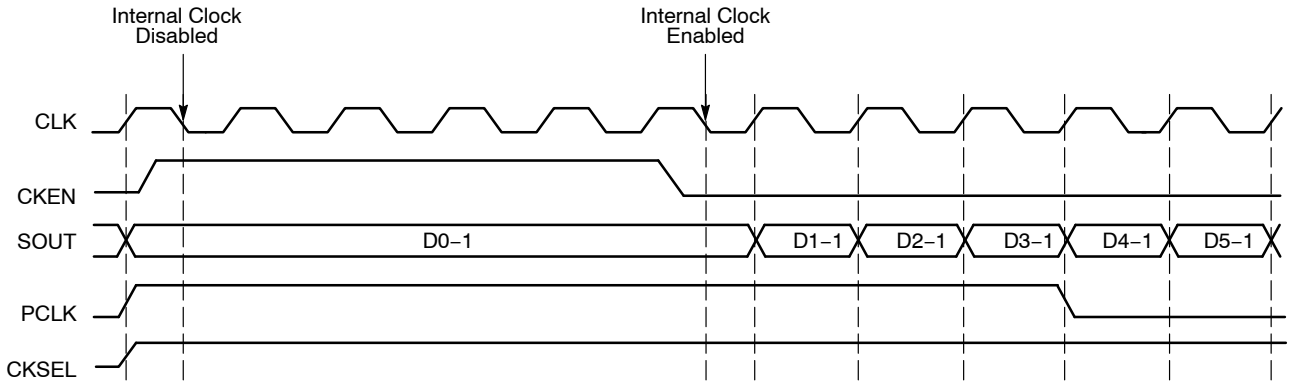


Figure 13. Timing Diagram with CKEN with CKSEL HIGH

The differential PCLK output (Pins 14 and 15) is a word framer and can help the user synchronize the serial data output, S_{OUT} (Pins 11 and 12), in their applications. Furthermore, PCLK can be used as a trigger for input parallel data (Figure 14).

An internally generated voltage supply, the V_{BB} pin, is available to this device only. For single–ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open. Also, both outputs of the differential pair must be terminated (50 Ω to V_{TT}) even if only one output is used.

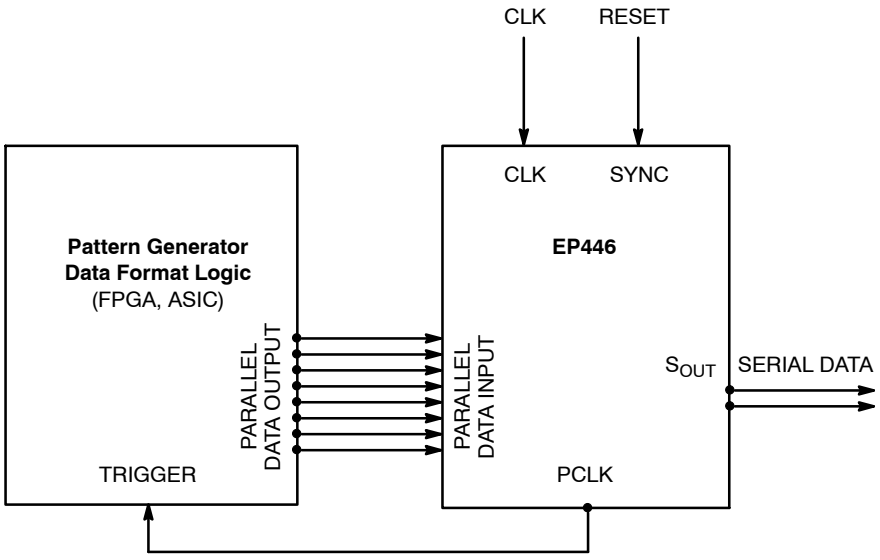


Figure 14. PCLK as Trigger Application

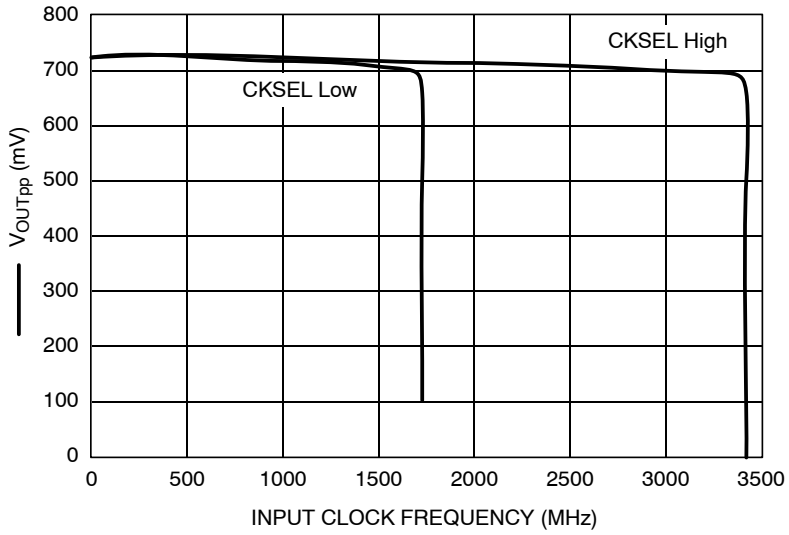


Figure 15. Typical V_{OUTPP} versus Input Clock Frequency, 25°C

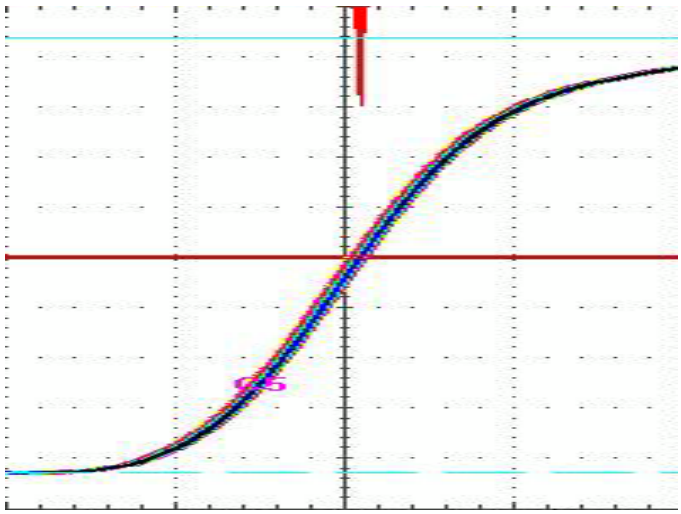


Figure 16. SOUT System Jitter Measurement
(Condition: 3.4 GHz input frequency, CKSEL HIGH, BEOFE32 bit pattern on SOUT

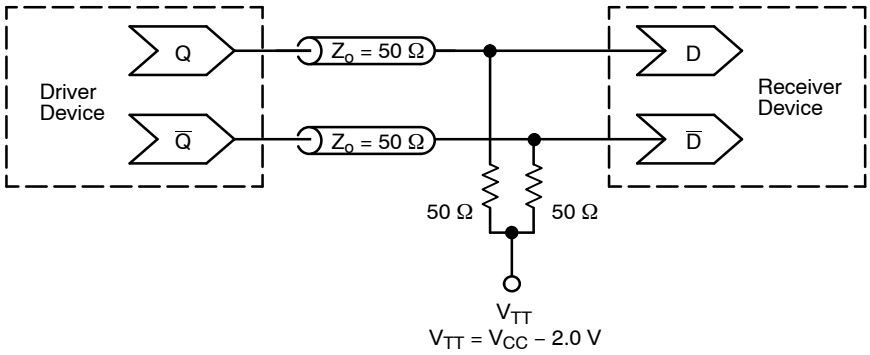


Figure 17. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP446MNG	QFN−32 (Pb−Free)	74 Units / Rail
MC100EP446FAG	LQFP−32 (Pb−Free)	250 Units / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

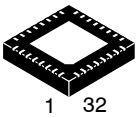
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

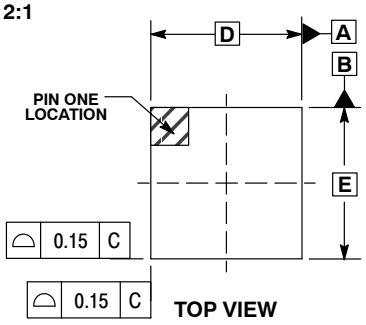
AND8090/D – AC Characteristics of ECL Devices

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

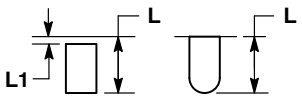
DATE 23 OCT 2013



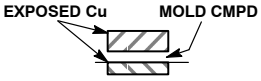
SCALE 2:1



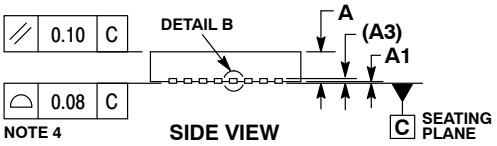
TOP VIEW



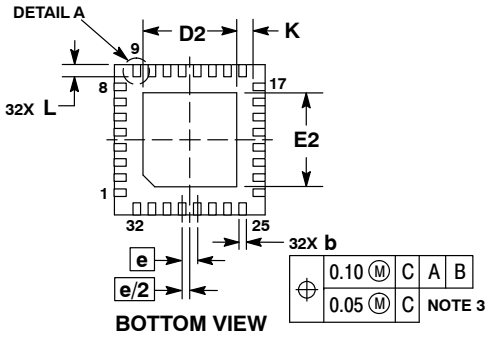
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

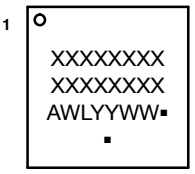


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

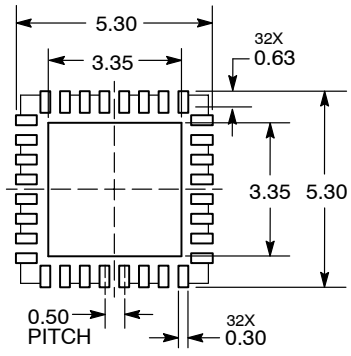


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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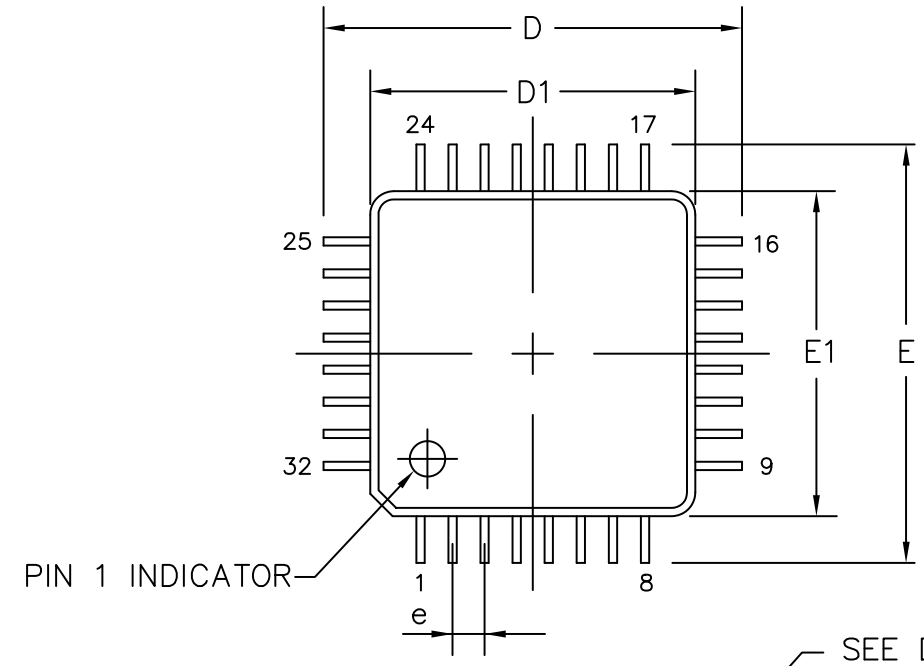
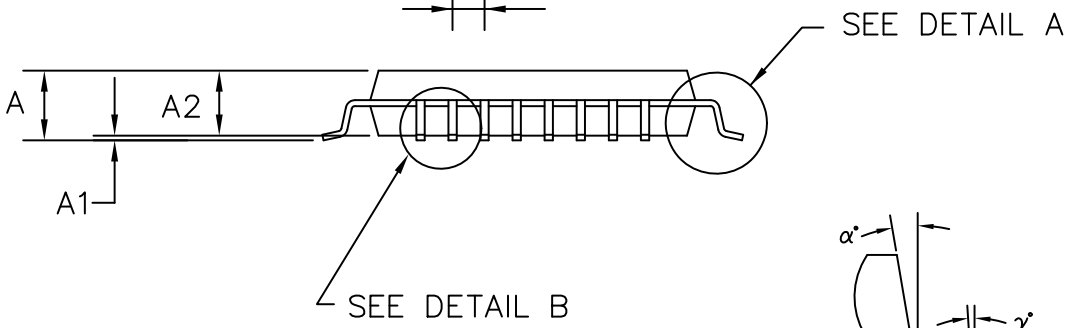
DESCRIPTION:	**QFN32 5x5 0.5P**	**PAGE 1 OF 1**

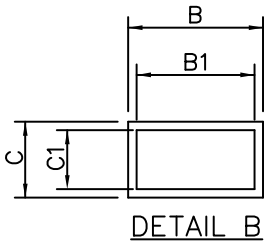
LQFP−32, 7x7
CASE 561AB
ISSUE O

DATE 19 JUN 2008

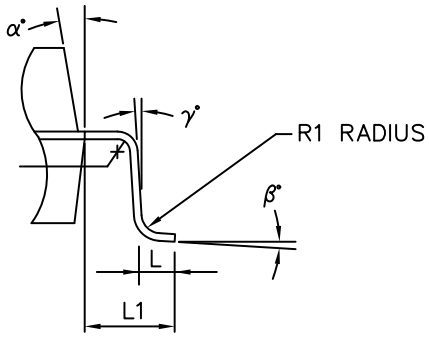


SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
α°	11	–	13
β°	0	–	7
γ°	0	–	–





DETAIL B



DETAIL A

ALL DIMENSIONS IN MM

DOCUMENT NUMBER:	**98AON30893E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**32 LEAD LQFP, 7X7**		**PAGE 1 OF 1**

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