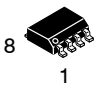
3.3 V ECL Differential Clock D Flip-Flop

MC100LVEL51



SOIC-8 NB
D SUFFIX
CASE 751

TSSOP-8
DT SUFFIX
CASE 948R

Description

The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a 3.3 V supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3 V V_{CC}.

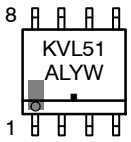
The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the $\overline{CLK}$ input will be biased at $V_{CC}/2$.

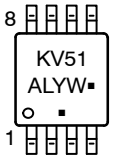
Features

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: > 4 kV Human Body Model, > 200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level
  - Level 1 for SOIC-8 NB
  - Level 3 for TSSOP-8
  - For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 114 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAMS*



SOIC-8



TSSOP-8

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL51DG	SOIC-8 NB (Pb-Free)	98 Units/Tube
MC100LVEL51DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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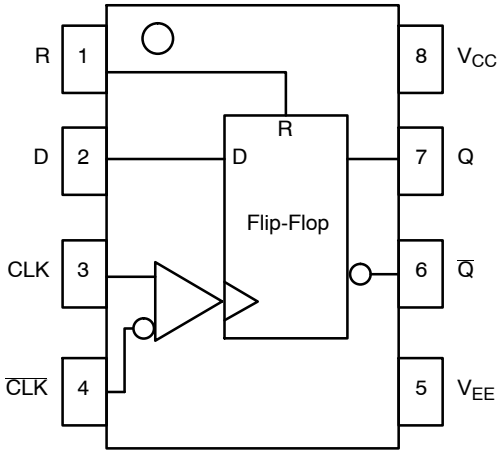

Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Differential Clock Input
Q, $\overline{Q}$	ECL Differential Output
D	ECL D Input
R	ECL Reset Input
V_{CC}	Positive Supp;y
V_{EE}	Negative Supply

Table 2. TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition
X = Don't Care

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 to 0 −6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44 ±5%	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8	185 140	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ±5%	°C/W
T_{sol}	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 4. LVPECL DC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 2))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	37	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7) V_{PP} < 500 mV V_{PP} ≥ 500 mV	 1.2 1.4		 3.0 3.0	 1.1 1.3		 3.0 3.0	 1.1 1.3		 3.0 3.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK}$	 0.5 −600			 0.5 −600			 0.5 −600			μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 5. LVNECL DC CHARACTERISTICS (V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 5))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	37	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 6)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7) V_{PP} < 500 mV V_{PP} ≥ 500 mV	 −2.1 −1.9		 −0.3 −0.3	 −2.2 −2.0		 −0.3 −0.3	 −2.2 −2.0		 −0.3 −0.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK}$	 0.5 −600			 0.5 −600			 0.5 −600			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 6. AC CHARACTERISTICS (V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 8))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	2.7			2.8			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	 330 340	 465 455	 510 540	 340 350	 475 465	 520 550	 370 390	 530 510	 550 590	ps
t_S	Setup Time	150	0		150	0		150	0		ps
t_H	Hold Time	200	100		200	100		200	100		ps
t_{RR}	Reset Recovery	350	200		350	200		350	200		ps
t_{PW}	Minimum Pulse CLK Width Reset	 400 500			 400 500			 400 500			ps
t_{JITTER}	Cycle-to-Cycle Jitter		6.9			7.0			7.1		ps
V_{PP}	Input Swing (Note 9)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% − 80%)	120		320	120		320	120		320	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. V_{EE} can vary ±0.3 V.
9. V_{PP} (min) is minimum input swing for which AC parameters are guaranteed.

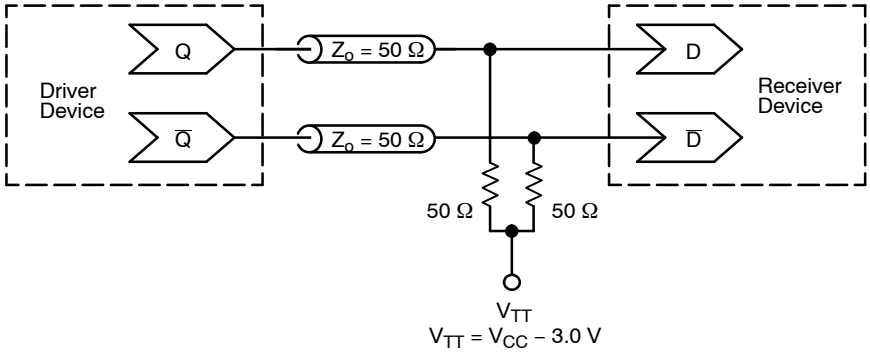

Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D	–	ECL Clock Distribution Techniques
AN1406/D	–	Designing with PECL (ECL at +5.0 V)
AN1503/D	–	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	–	Metastability and the ECLinPS Family
AN1568/D	–	Interfacing Between LVDS and ECL
AN1672/D	–	The ECL Translator Guide
AND8001/D	–	Odd Number Counters Design
AND8002/D	–	Marking and Date Codes
AND8020/D	–	Termination of ECL Logic Devices
AND8066/D	–	Interfacing with ECLinPS
AND8090/D	–	AC Characteristics of ECL Devices

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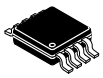
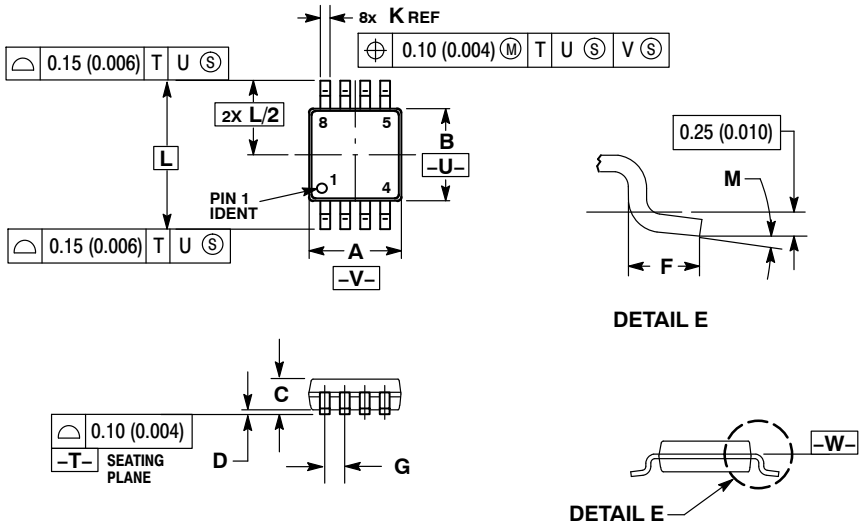


SCALE 2:1

TSSOP–8 3.00x3.00x0.95
CASE 948R–02
ISSUE A

DATE 07 APR 2000



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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