

## 3.3 V/5 V ECL D Flip-Flop with Reset and Differential Clock

### MC10EP51, MC100EP51

#### Description

The MC10/100EP51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 and LVEL51 devices.

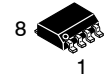
The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to  $V_{EE}$  and the  $\overline{CLK}$  input will be biased at  $V_{CC}/2$ .

The 100 Series contains temperature compensation.

#### Features

- 350 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- These Devices are Pb-Free and are RoHS Compliant



SOIC-8  
D SUFFIX  
CASE 751

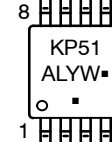
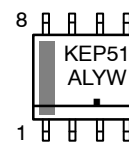
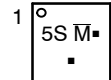
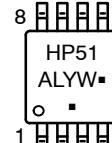
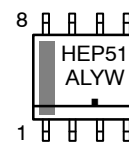


TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA

#### MARKING DIAGRAM



|    |                     |
|----|---------------------|
| H  | = MC10              |
| K  | = MC100             |
| 5S | = MC10              |
| M  | = Date Code         |
| A  | = Assembly Location |
| L  | = Wafer Lot         |
| Y  | = Year              |
| W  | = Work Week         |
| ■  | = Pb-Free Package   |

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

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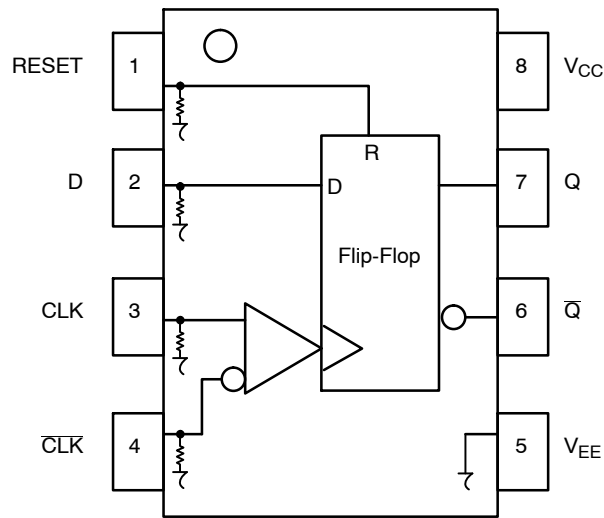


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

| PIN                             | FUNCTION                                                                                                                                                                       |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK*, $\overline{\text{CLK}}$ * | ECL Clock Inputs                                                                                                                                                               |
| Reset*                          | ECL Asynchronous Reset                                                                                                                                                         |
| D*                              | ECL Data Input                                                                                                                                                                 |
| Q, $\overline{\text{Q}}$        | ECL Data Outputs                                                                                                                                                               |
| V <sub>CC</sub>                 | Positive Supply                                                                                                                                                                |
| V <sub>EE</sub>                 | Negative Supply                                                                                                                                                                |
| EP                              | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

\* Pins will default LOW when left open.

Table 2. TRUTH TABLE

| D | R | CLK | Q |
|---|---|-----|---|
| L | L | Z   | L |
| H | L | Z   | H |
| X | H | X   | L |

Z = LOW to HIGH Transition

Table 3. ATTRIBUTES

| Characteristics                                                             | Value                         |
|-----------------------------------------------------------------------------|-------------------------------|
| Internal Input Pulldown Resistor                                            | 75 k $\Omega$                 |
| Internal Input Pullup Resistor                                              | N/A                           |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 200 V<br>> 2 kV   |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               | Pb-Free Pkg                   |
| SOIC-8<br>TSSOP-8<br>DFN8                                                   | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL 94 V-0 @ 0.125 in          |
| Transistor Count                                                            | 165 Devices                   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                               |

1. For additional information, see Application Note [AND8003/D](#).

# MC10EP51, MC100EP51

**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating      | Unit         |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|-------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 6           | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | –6          | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>–6     | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100   | mA<br>mA     |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | –40 to +85  | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | –65 to +150 | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction–to–Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC–8<br>SOIC–8                                                     | 190<br>130  | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction–to–Case)              | Standard Board                                 | SOIC–8                                                               | 41 to 44    | °C/W         |
| θ <sub>JA</sub>  | Thermal Resistance (Junction–to–Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP–8<br>TSSOP–8                                                   | 185<br>140  | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction–to–Case)              | Standard Board                                 | TSSOP–8                                                              | 41 to 44    | °C/W         |
| θ <sub>JA</sub>  | Thermal Resistance (Junction–to–Ambient)           | 0 lfpm<br>500 lfpm                             | DFN8<br>DFN8                                                         | 129<br>84   | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction–to–Case)              | (Note 2)                                       | DFN8                                                                 | 35 to 40    | °C/W         |
| T <sub>sol</sub> | Wave Solder<br>Pb<br>Pb–Free                       |                                                |                                                                      | 265<br>265  | °C           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

**Table 5. 10EP DC CHARACTERISTICS, PECL** V<sub>CC</sub> = 3.3 V, V<sub>EE</sub> = 0 V (Note 3)

| Symbol             | Characteristic                                                             | –40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|--------------------|----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|------|
|                    |                                                                            | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| I <sub>EE</sub>    | Power Supply Current                                                       | 26    | 34   | 44   | 26   | 35   | 45   | 28   | 37   | 47   | mA   |
| V <sub>OH</sub>    | Output HIGH Voltage (Note 4)                                               | 2165  | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV   |
| V <sub>OL</sub>    | Output LOW Voltage (Note 4)                                                | 1365  | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV   |
| V <sub>IH</sub>    | Input HIGH Voltage (Single–Ended)                                          | 2090  |      | 2415 | 2155 |      | 2480 | 2215 |      | 2540 | mV   |
| V <sub>IL</sub>    | Input LOW Voltage (Single–Ended)                                           | 1365  |      | 1690 | 1430 |      | 1755 | 1490 |      | 1815 | mV   |
| V <sub>IHCMR</sub> | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V    |
| I <sub>IH</sub>    | Input HIGH Current                                                         |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| I <sub>IL</sub>    | Input LOW Current                                                          | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.3 V to –2.2 V.

4. All loading with 50 Ω to V<sub>CC</sub> – 2.0 V.

5. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>. V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

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**Table 6. 10EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 6)

| Symbol      | Characteristic                                                             | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                            | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                       | 26    | 34   | 44   | 26   | 35   | 45   | 28   | 37   | 47   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 7)                                               | 3865  | 3990 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 7)                                                | 3065  | 3190 | 3315 | 3130 | 3255 | 3380 | 3190 | 3315 | 3440 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | 3790  |      | 4115 | 3855 |      | 4180 | 3915 |      | 4240 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | 3065  |      | 3390 | 3130 |      | 3455 | 3190 |      | 3515 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

7. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 9)

| Symbol      | Characteristic                                                              | -40°C          |       |       | 25°C           |       |       | 85°C           |       |       | Unit          |
|-------------|-----------------------------------------------------------------------------|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
|             |                                                                             | Min            | Typ   | Max   | Min            | Typ   | Max   | Min            | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                                        | 23             | 30    | 40    | 23             | 30    | 40    | 23             | 30    | 40    | mA            |
| $I_{EE}$    | Power Supply Current                                                        | 26             | 34    | 44    | 26             | 35    | 45    | 28             | 37    | 47    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 10)                                               | -1135          | -1010 | -885  | -1070          | -945  | -820  | -1010          | -885  | -760  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 10)                                                | -1935          | -1810 | -1685 | -1870          | -1745 | -1620 | -1810          | -1685 | -1560 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | -1210          |       | -885  | -1145          |       | -820  | -1085          |       | -760  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | -1935          |       | -1610 | -1870          |       | -1545 | -1810          |       | -1485 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 11) | $V_{EE} + 2.0$ |       | 0.0   | $V_{EE} + 2.0$ |       | 0.0   | $V_{EE} + 2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current                                                          |                |       | 150   |                |       | 150   |                |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                           | 0.5            |       |       | 0.5            |       |       | 0.5            |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .

10. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

11.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 8. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 12)

| Symbol      | Characteristic                                                              | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|-----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                             | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                        | 26    | 34   | 44   | 26   | 35   | 45   | 28   | 37   | 47   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 13)                                               | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 13)                                                | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | 1355  |      | 1675 | 1355 |      | 1675 | 1355 |      | 1675 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 14) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current                                                          |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                           | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

12. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

13. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

14.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 9. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 15)

| Symbol      | Characteristic                                                              | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|-----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                             | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                        | 26    | 34   | 44   | 26   | 35   | 45   | 28   | 37   | 47   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 16)                                               | 3855  | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 16)                                                | 3055  | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | 3775  |      | 4120 | 3775 |      | 4120 | 3775 |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | 3055  |      | 3375 | 3055 |      | 3375 | 3055 |      | 3375 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 17) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current                                                          |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                           | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

15. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

16. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

17.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP51, MC100EP51

**Table 10. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 18)

| Symbol      | Characteristic                                                              | -40°C          |       |       | 25°C           |       |       | 85°C           |       |       | Unit          |
|-------------|-----------------------------------------------------------------------------|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
|             |                                                                             | Min            | Typ   | Max   | Min            | Typ   | Max   | Min            | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                                        | 26             | 34    | 44    | 26             | 35    | 45    | 28             | 37    | 47    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 19)                                               | -1145          | -1020 | -895  | -1145          | -1020 | -895  | -1145          | -1020 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 19)                                                | -1945          | -1820 | -1695 | -1945          | -1820 | -1695 | -1945          | -1820 | -1695 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | -1225          |       | -880  | -1225          |       | -880  | -1225          |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | -1945          |       | -1625 | -1945          |       | -1625 | -1945          |       | -1625 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 20) | $V_{EE} + 2.0$ |       | 0.0   | $V_{EE} + 2.0$ |       | 0.0   | $V_{EE} + 2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current                                                          |                |       | 150   |                |       | 150   |                |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                           | 0.5            |       |       | 0.5            |       |       | 0.5            |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

18. Input and output parameters vary 1:1 with  $V_{CC}$ .

19. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

20.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 11. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 21)

| Symbol                   | Characteristic                                                                                | -40°C      |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|--------------------------|-----------------------------------------------------------------------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                          |                                                                                               | Min        | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| $f_{\max}$               | Maximum Frequency (Figure 2)                                                                  |            | > 3        |            |            | > 3        |            |            | > 3        |            | GHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential<br>CLK, $\overline{\text{CLK}}$ to Q, $\overline{Q}$ | 250<br>275 | 300<br>340 | 350<br>425 | 270<br>300 | 320<br>375 | 370<br>450 | 300<br>350 | 350<br>425 | 420<br>500 | ps   |
|                          | RESET to Q, $\overline{Q}$                                                                    | 300        | 380        | 450        | 325        | 400        | 475        | 350        | 425        | 500        |      |
| $t_{RR}$                 | Reset Recovery                                                                                | 150        |            |            | 150        |            |            | 150        |            |            | ps   |
| $t_S$<br>$t_H$           | Setup Time<br>Hold Time                                                                       | 100<br>100 |            |            | 100<br>100 | 80<br>40   |            | 100<br>100 |            |            | ps   |
| $t_{PW}$                 | Minimum Pulse Width<br>RESET                                                                  | 500        | 440        |            | 500        | 440        |            | 500        | 440        |            | ps   |
| $t_{JITTER}$             | Cycle-to-Cycle Jitter (Figure 2)                                                              |            | 0.2        | < 1        |            | 0.2        | < 1        |            | 0.2        | < 1        | ps   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times<br>(20% – 80%) Q, $\overline{Q}$                                       | 70         | 120        | 170        | 80         | 130        | 180        | 100        | 150        | 200        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

## MC10EP51, MC100EP51

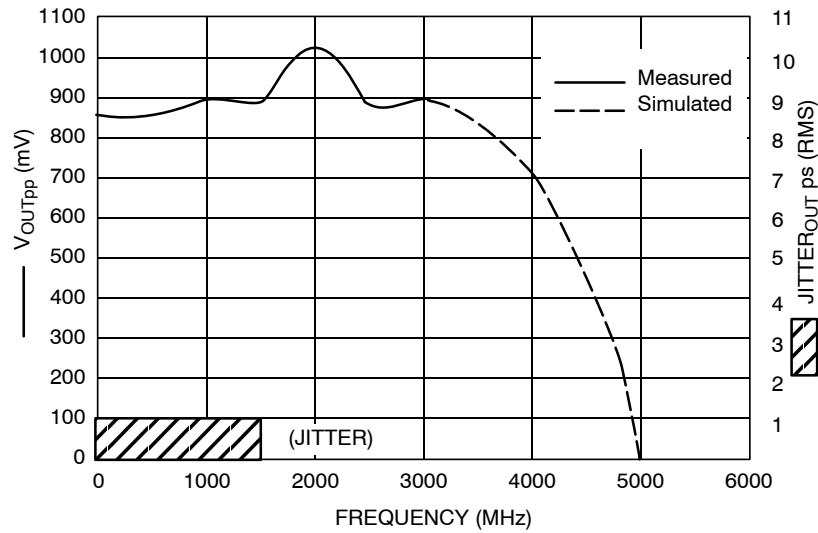


Figure 2.  $F_{max}$ /Jitter

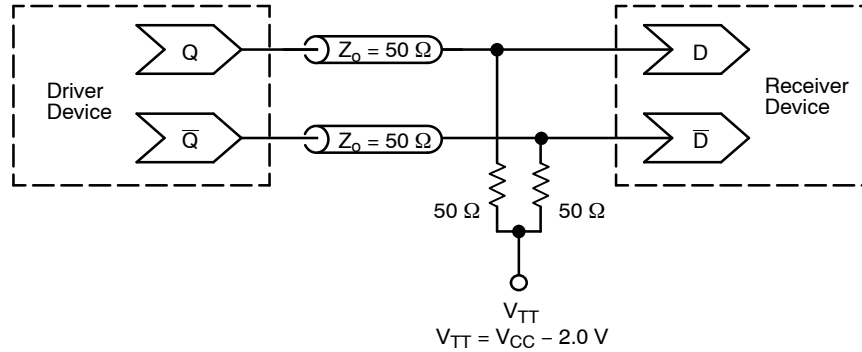


Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

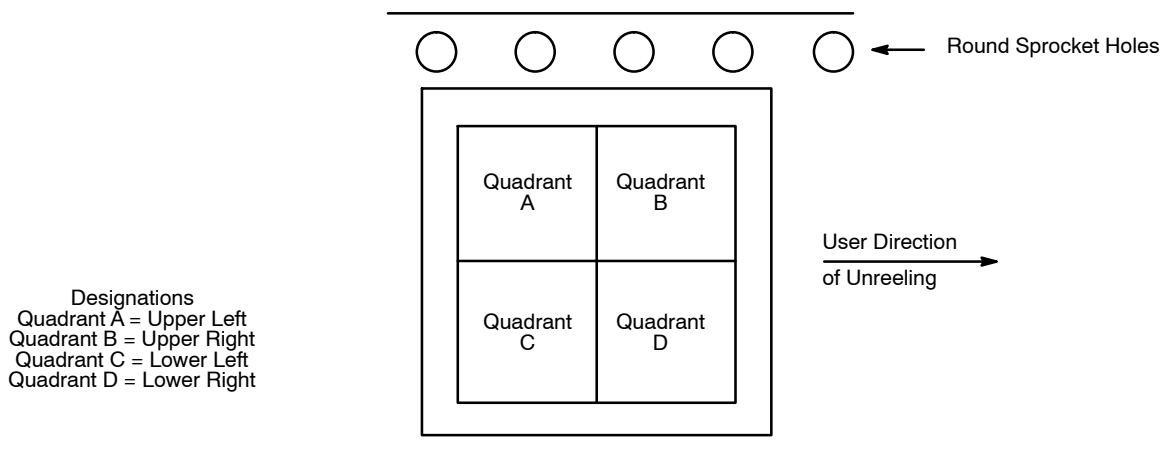


Figure 4. Tape and Reel Pin 1 Quadrant Orientation

# MC10EP51, MC100EP51

## ORDERING INFORMATION

| Device         | Package              | Shipping <sup>†</sup>                                             |
|----------------|----------------------|-------------------------------------------------------------------|
| MC10EP51DR2G   | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel                                                |
| MC10EP51MNTAG  | DFN8<br>(Pb-Free)    | 1000 / Tape & Reel<br>(Pin 1 Orientation in Quadrant A, Figure 4) |
| MC100EP51DG    | SOIC-8<br>(Pb-Free)  | 98 Units / Rail                                                   |
| MC100EP51DR2G  | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel                                                |
| MC100EP51DTG   | TSSOP-8<br>(Pb-Free) | 100 Units / Rail                                                  |
| MC100EP51DTR2G | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel                                                |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

## DISCONTINUED (Note 22)

| Device      | Package              | Shipping <sup>†</sup> |
|-------------|----------------------|-----------------------|
| MC10EP51DG  | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC10EP51DTG | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

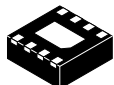
22. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](#).

## Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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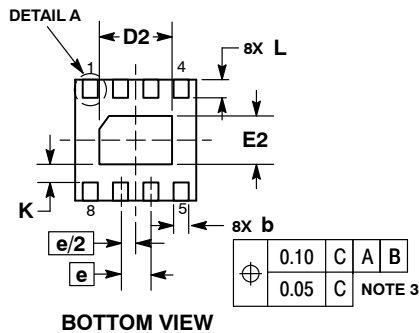
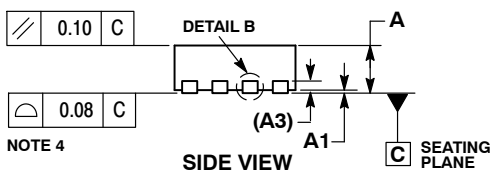
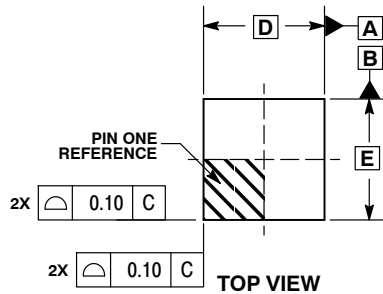




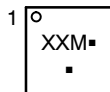
SCALE 4:1

**DFN8 2x2, 0.5P**  
**CASE 506AA**  
**ISSUE F**

DATE 04 MAY 2016

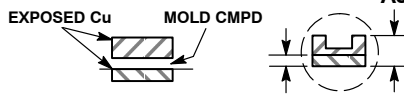
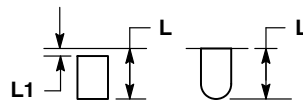


**GENERIC**  
**MARKING DIAGRAM\***



XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Device

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

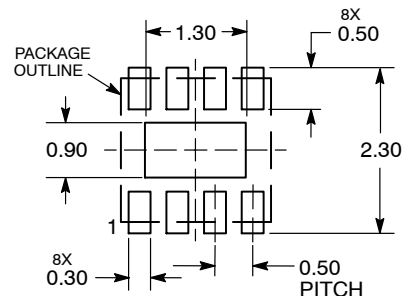


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.20 | 0.30 |
| D           | 2.00 | BSC  |
| D2          | 1.10 | 1.30 |
| E           | 2.00 | BSC  |
| E2          | 0.70 | 0.90 |
| e           | 0.50 | BSC  |
| K           | 0.30 | REF  |
| L           | 0.25 | 0.35 |
| L1          |      | 0.10 |

**RECOMMENDED**  
**SOLDERING FOOTPRINT\***

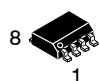


DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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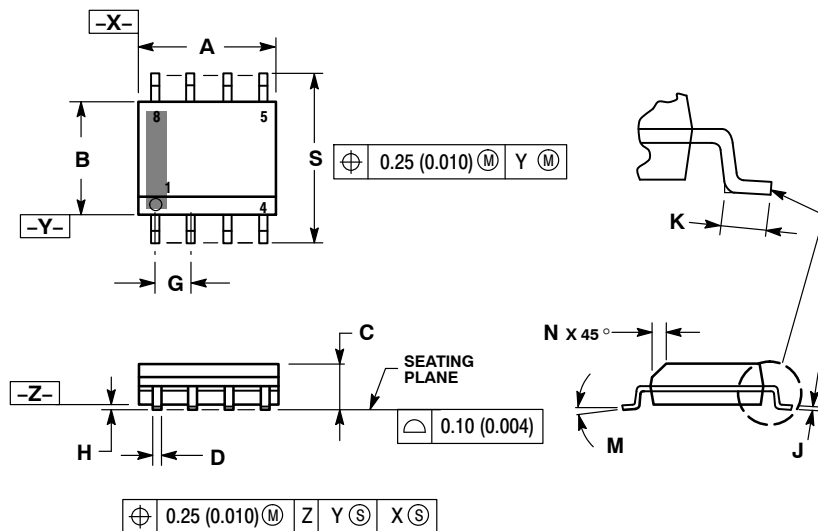
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SCALE 1:1

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

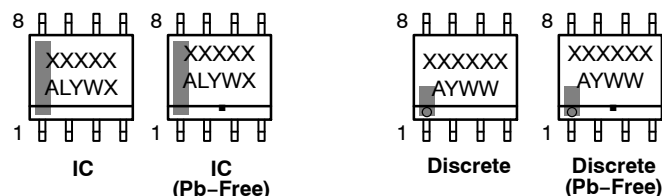
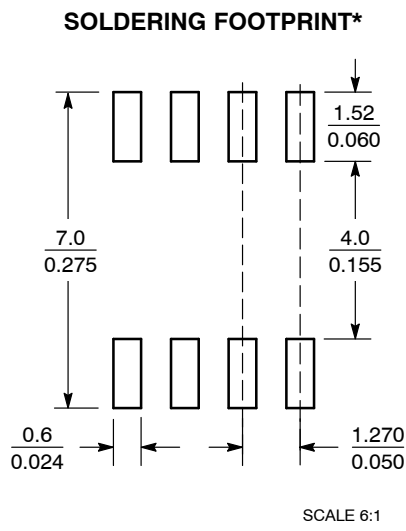
DATE 16 FEB 2011



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

**GENERIC**  
**MARKING DIAGRAM\***


XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

|                         |                    |                                                                                                                                                                                     |
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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

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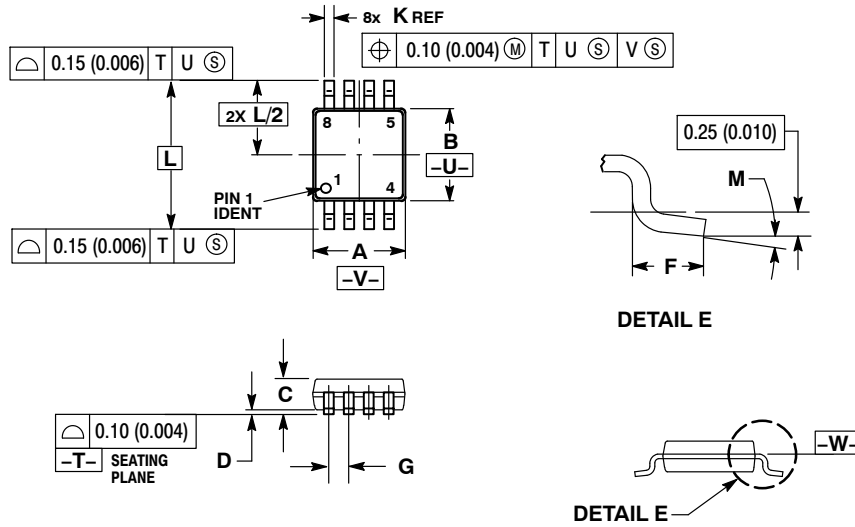
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SCALE 2:1

TSSOP-8 3.00x3.00x0.95  
CASE 948R-02  
ISSUE A

DATE 07 APR 2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

|                  |                        |                                                                                                                                                                                     |
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| DESCRIPTION:     | TSSOP-8 3.00x3.00x0.95 | PAGE 1 OF 1                                                                                                                                                                         |

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