Dual Complementary Pair Plus Inverter

MC14007UB

The MC14007UB multipurpose device consists of three N−Channel and three P−Channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse−shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Antistatic precautions must be taken.
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

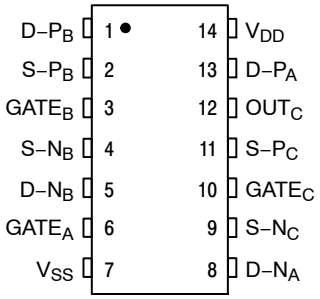
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8 second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: −7.0 mW/°C from 65°C 5o 125°C.

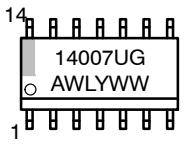
SOIC−14
D SUFFIX
CASE 751A

PIN ASSIGNMENT



D = DRAIN
S = SOURCE

MARKING DIAGRAM



A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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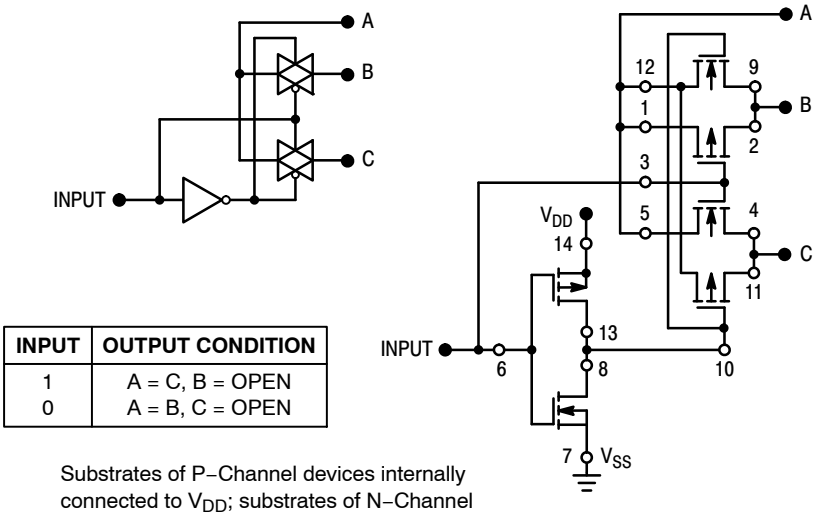
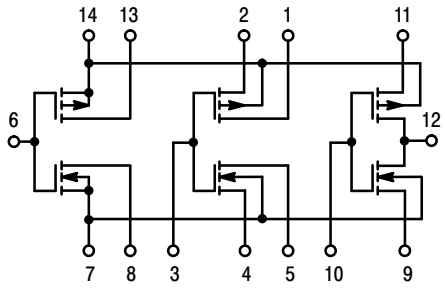


INPUT	OUTPUT CONDITION
1	A = C, B = OPEN
0	A = B, C = OPEN

Substrates of P−Channel devices internally connected to V_{DD}; substrates of N−Channel devices internally connected to V_{SS}.

Figure 1. Typical Application: 2−Input Analog Multiplexer



V_{DD} = PIN 14
V_{SS} = PIN 7

Figure 2. Schematic

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
V_{OL}	Output Voltage “0” Level V_{in} = V_{DD} or 0	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{OH}	V_{in} = 0 or V_{DD} “1” Level	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
V_{IL}	Input Voltage “0” Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)	 5.0 10 15	 – – –	 1.0 2.0 2.5	 – – –	 2.25 4.50 6.75	 1.0 2.0 2.5	 – – –	 1.0 2.0 2.5	Vdc
V_{IH}	(V_O = 0.5 Vdc) “1” Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)	5.0 10 15	4.0 8.0 12.5	– – –	4.0 8.0 12.5	2.75 5.50 8.25	– – –	4.0 8.0 12.5	– – –	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	 5.0 5.0 10 15	 –3.0 –0.64 –1.6 –4.2	 – – – –	 –2.4 –0.51 –1.3 –3.4	 –5.0 –1.0 –2.5 –10	 – – – –	 –1.7 –0.36 –0.9 –2.4	 – – – –	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	1.0 2.5 10	– – –	0.36 0.9 2.4	– – –	mAdc
I_{in}	Input Current	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
C_{in}	Input Capacitance (V_{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I_{DD}	Quiescent Current (Per Package)	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	μAdc
I_T	Total Supply Current (Notes 3 and 4) (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	5.0 10 15	I_T = (0.7 μA/kHz) f + I_{DD}/6 I_T = (1.4 μA/kHz) f + I_{DD}/6 I_T = (2.2 μA/kHz) f + I_{DD}/6							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$
   where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

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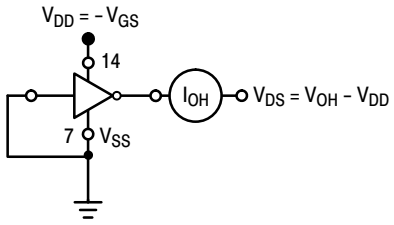
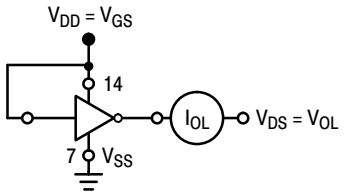
SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
t_{TLH}	Output Rise Time					ns
	t_{TLH} = (1.2 ns/pF) C_L + 30 ns	5.0	–	90	180	
	t_{TLH} = (0.5 ns/pF) C_L + 20 ns	10	–	45	90	
	t_{TLH} = (0.4 ns/pF) C_L + 15 ns	15	–	35	70	
t_{THL}	Output Fall Time					ns
	t_{THL} = (1.2 ns/pF) C_L + 15 ns	5.0	–	75	150	
	t_{THL} = (0.5 ns/pF) C_L + 15 ns	10	–	40	80	
	t_{THL} = (0.4 ns/pF) C_L + 10 ns	15	–	30	60	
t_{PLH}	Turn−Off Delay Time					ns
	t_{PLH} = (1.5 ns/pF) C_L + 35 ns	5.0	–	60	125	
	t_{PLH} = (0.2 ns/pF) C_L + 20 ns	10	–	30	75	
	t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns	15	–	25	55	
t_{PHL}	Turn−On Delay Time					ns
	t_{PHL} = (1.0 ns/pF) C_L + 10 ns	5.0	–	60	125	
	t_{PHL} = (0.3 ns/pF) C_L + 15 ns	10	–	30	75	
	t_{PHL} = (0.2 ns/pF) C_L + 15 ns	15	–	25	55	

5. The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



All unused inputs connected to ground.



All unused inputs connected to ground.

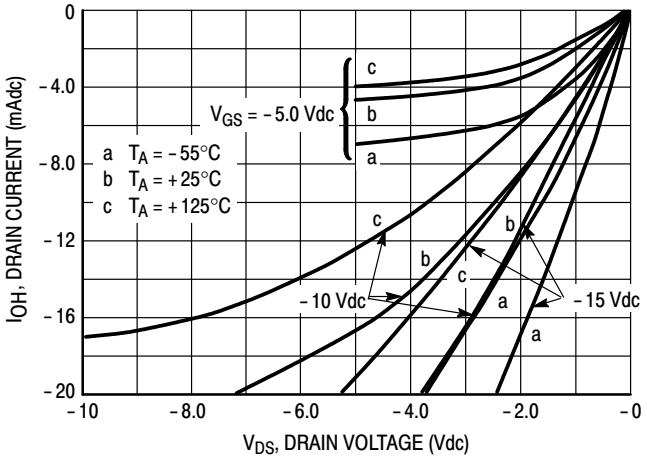


Figure 3. Typical Output Source Characteristics

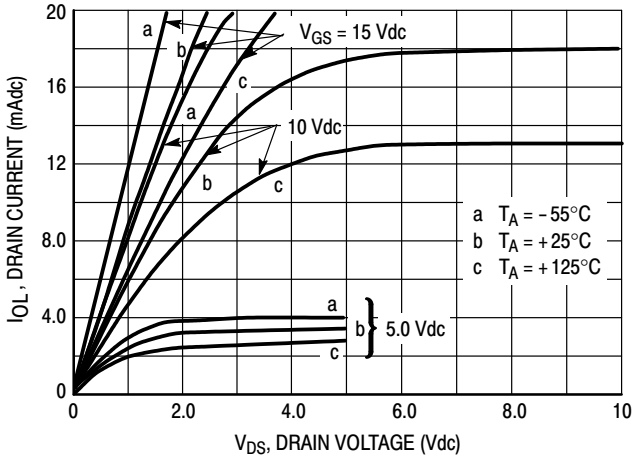


Figure 4. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.
Caution: The maximum current rating is 10 mA per pin.

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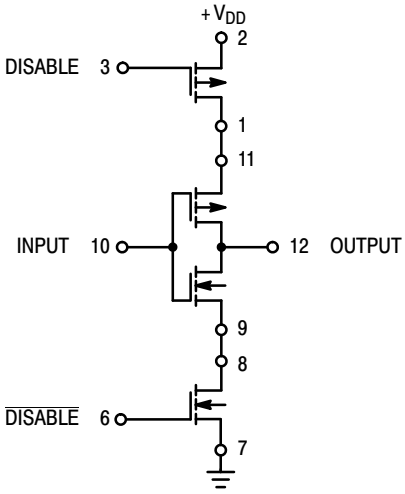
Figure 5. Switching Time and Power Dissipation Test Circuit and Waveforms

APPLICATIONS

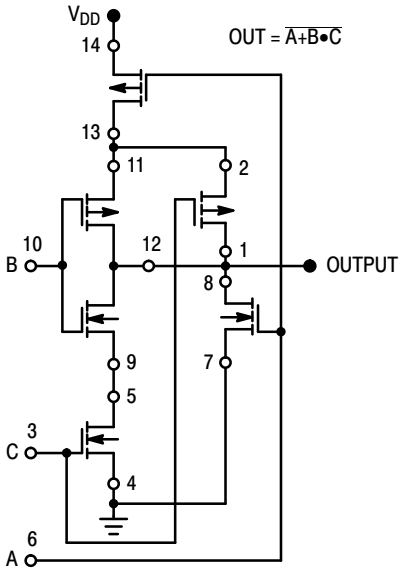
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 6, and 7 are a few examples of the device flexibility.



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don't Care

Figure 6. 3−State Buffer



Substrates of P−Channel devices internally connected to V_{DD};
Substrates of N−Channel devices internally connected to V_{SS}.

Figure 7. AOI Functions Using Tree Logic

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ORDERING INFORMATION

Device	Package	Shipping†
MC14007UBDG	SOIC−14 (Pb−Free)	55 Units / Rail
MC14007UBDR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NLV14007UBDR2G*	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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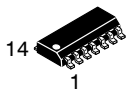

SCALE 1:1

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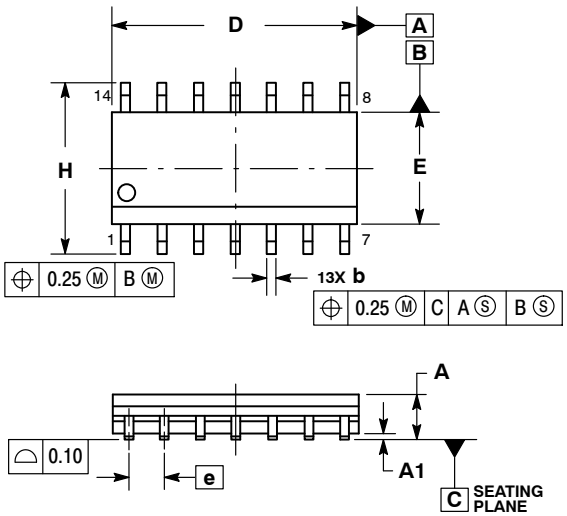
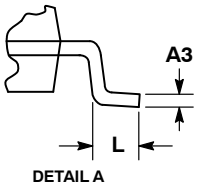
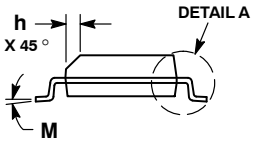
ISSUE L

DATE 03 FEB 2016



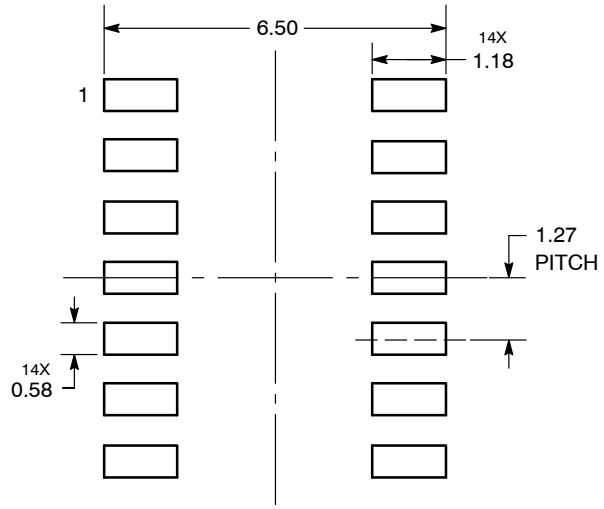




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

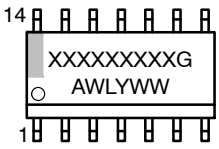
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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