# MC14028B

# **BCD-To-Decimal Decoder Binary-To-Octal Decoder**

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one–of–ten) decoded output, while a 3-bit binary input provides a decoded octal (one–of–eight) code output with D forced to a logic "0". Expanded decoding such as binary–to–hexadecimal (one–of–sixteen), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

#### **Features**

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

# MAXIMUM RATINGS (Voltages Referenced to VSS)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	$V_{DD}$	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V <sub>in</sub> , V <sub>out</sub>	-0.5 to V <sub>DD</sub> + 0.5	V
Input or Output Current (DC or Transient) per Pin	I <sub>in</sub> , I <sub>out</sub>	±10	mA
Power Dissipation per Package (Note 1)	P <sub>D</sub>	500	mW
Ambient Temperature Range	T <sub>A</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Lead Temperature (8–Second Soldering)	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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SOIC-16 D SUFFIX CASE 751B

#### **PIN ASSIGNMENT**

Q4 [	1 ●	16	
Q2 [	2	15	] Q3
Q0 [	3	14	] Q1
Q7 [	4	13	] в
Q9 [	5	12	] C
Q5 [	6	11	D
Q6 [	7	10	] A
v <sub>ss</sub> [	8	9	Q8

#### MARKING DIAGRAM



A = Assembly Location

WL = Wafer Lot
 YY, Y = Year
 WW = Work Week
 G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14028B

#### **BLOCK DIAGRAM** Q0 **o** 3 Q1 **o** 14 3-BIT Q2 **O** 2 **BINARY OCTAL** Q3 13 O-8421 DECODED **INPUTS** DECIMAL Q4 BCD OUTPUTS DECODED Q5 **INPUTS** OUTPUTS Q6 Q7 Q8 **-0** 9 Q9

 $V_{DD} = PIN 16$  $V_{SS} = PIN 8$ 

#### **TRUTH TABLE**

D	С	В	Α	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC14028BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14028BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14028BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

#### MC14028B

#### **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

			-5	5°C		25°C		125	°C	
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage "0" Lev V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
$V_{in}$ = 0 or $V_{DD}$ "1" Lev	V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	1 1 1	4.95 9.95 14.95	- - -	Vdc
Input Voltage "0" Lev (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
"1" Lev $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	1 1 1	3.5 7.0 11	- - -	Vdc
	e I <sub>OH</sub>	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2		-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8	1 1 1	-1.7 -0.36 -0.9 -2.4		mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sir $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	l <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	1 1 1	0.36 0.9 2.4	- - -	mAdc
Input Current	l <sub>in</sub>	15	_	±0.1	_	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	_	-	_	5.0	7.5	_	-	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0 10 15		5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15			$I_T = ($	0.3 μΑ/kHz) 0.6 μΑ/kHz) 0.9 μΑ/kHz)	f + I <sub>DD</sub>			μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

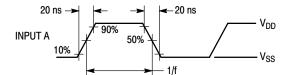
- 2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
- The formulas given are for the typical characteristics only at 25°C.
   To calculate total supply current at loads other than 50 pF: I<sub>T</sub>(C<sub>L</sub>) = I<sub>T</sub>(50 pF) + (C<sub>L</sub> 50) Vfk where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# **SWITCHING CHARACTERISTICS** (Note 5) ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH},t_{THL}=(1.5\;\text{ns/pF})\;C_L+25\;\text{ns}\\t_{TLH},t_{THL}=(0.75\;\text{ns/pF})\;C_L+12.5\;\text{ns}\\t_{TLH},t_{THL}=(0.55\;\text{ns/pF})\;C_L+9.5\;\text{ns}$	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) \text{ C}_{L} + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) \text{ C}_{L} + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) \text{ C}_{L} + 65 \text{ ns}$	t <sub>РLН</sub> , t <sub>РНL</sub>	5.0 10 15	- - -	300 130 90	600 260 180	ns

- 5. The formulas given are for the typical characteristics only at 25°C.
- 6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Inputs B, C, and D switching in respect to a BCD code.



All outputs connected to respective  $C_L$  loads. f in respect to a system clock.

Inputs A, B, and D low.

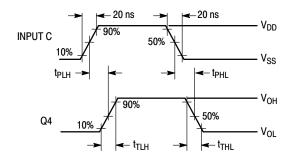
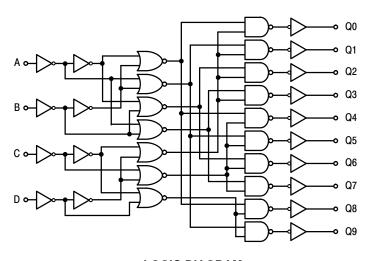


Figure 1. Dynamic Signal Waveforms



# **LOGIC DIAGRAM**

# **APPLICATIONS INFORMATION**

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

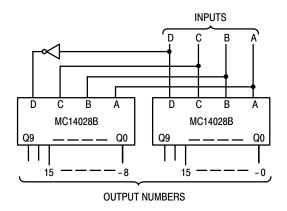


Figure 2. Code Conversion Circuit and Truth Table

																							Rede lumb		
															Hex	adeci	mal	D	ecima	al					
	Inp	uts								Out	put N	lumb	ers							٠ <del>١</del>	t /	5–3	s-3 /	n	
D	С	В	Α	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-	Excess–3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3	_	0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6 7	4	3	1		4
0	1	1	-	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	· ·	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			_
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1 0	0	0	0	0	0	0	0	0	0	0	10 11	12 13	7 8	9	5	6
	Ľ.							'	_		_	_			_	_			_			_	_	_	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	_
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1 1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14 15	11		8 7	8	8
1	T	T	1	1	U	0	0	0	0	U	0	0	0	0	0	0	0	0	0	15	10		/	9	9

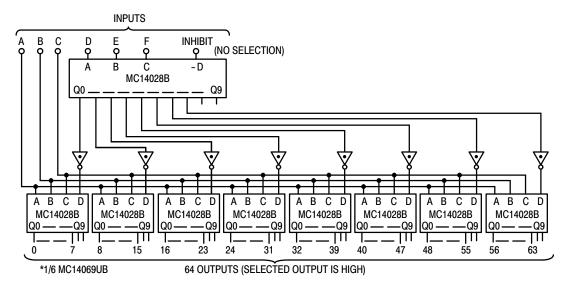


Figure 3. Six-Bit Binary 1-of-64 Decoder

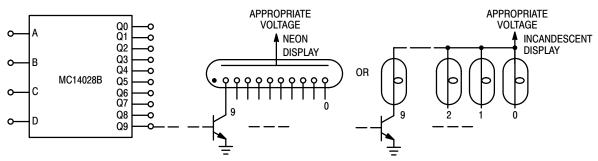


Figure 4. Decimal Digit Display Application



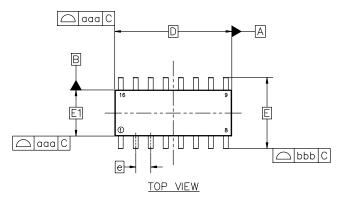


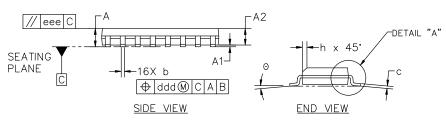
#### SOIC-16 9.90x3.90x1.37 1.27P CASE 751B ISSUE M

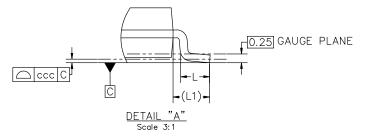
**DATE 18 OCT 2024** 

#### NOTES:

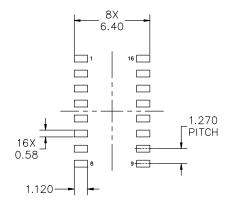
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- 5. DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







	MILLIM	ETERS								
DIM	MIN	NOM	MAX							
А	1.35	1.75								
A1	0.10	0.18	0.25							
A2	1.25	1.37	1.50							
b	0.35	0.42	0.49							
С	0.19	0.22	0.25							
D		9.90 BSC								
E	6.00 BSC									
E1	3.90 BSC									
е	1.27 BSC									
h	0.25		0.50							
L	0.40	0.83	1.25							
L1		1.05 REF								
Θ	0.		7*							
TOLERAN	CE OF FC	RM AND	POSITION							
aaa		0.10								
bbb	0.20									
ccc		0.10								
ddd		0.25								
eee		0.10								



#### RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR
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AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

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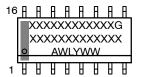
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# **SOIC-16 9.90x3.90x1.37 1.27P** CASE 751B

ISSUE M

**DATE 18 OCT 2024** 

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:		STYLE 2:		STYLE 3:	S	STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE. #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER. #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.		14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1
STYLE 5:		STYLE 6:		STYLE 7:			
PIN 1.							
PIN I.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH		
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)		
	DRAIN, #1 DRAIN, #2		CATHODE CATHODE	2. 3.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
2.	DRAIN, #1 DRAIN, #2 DRAIN, #2	2. 3. 4.	CATHODE CATHODE CATHODE	2. 3. 4.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH		
2. 3.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3	2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE	2. 3.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT)		
2. 3. 4.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3	2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE CATHODE	2. 3. 4.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)	 	
2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4	2. 3. 4. 5. 6. 7.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)	 	
2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4	2. 3. 4. 5. 6. 7.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH	 	
2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4	2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH		
2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT)		
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2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2	2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT)		
2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 SOURCE, #3 SOURCE, #3 SOURCE, #2 GATE, #2 SOURCE, #2 GATE, #1	2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2	2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT)		

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