Hex Contact Bounce Eliminator

MC14490

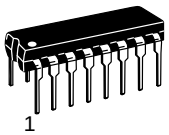
The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the “make” and the “break” of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

NOTE: Immediately after powerup, the outputs of the MC14490 are in indeterminate states.

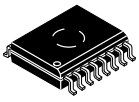
Features

- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both “Make” and “Break” Contacts
- Does Not Require “Form C” (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

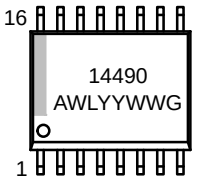
MARKING DIAGRAMS

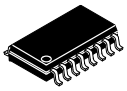


PDIP-16
P SUFFIX
CASE 648

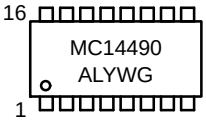


SOIC-16
DW SUFFIX
CASE 751G





SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 9.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8-Second Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65 °C To 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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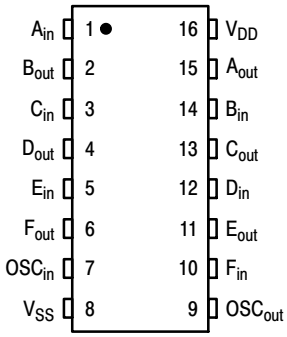
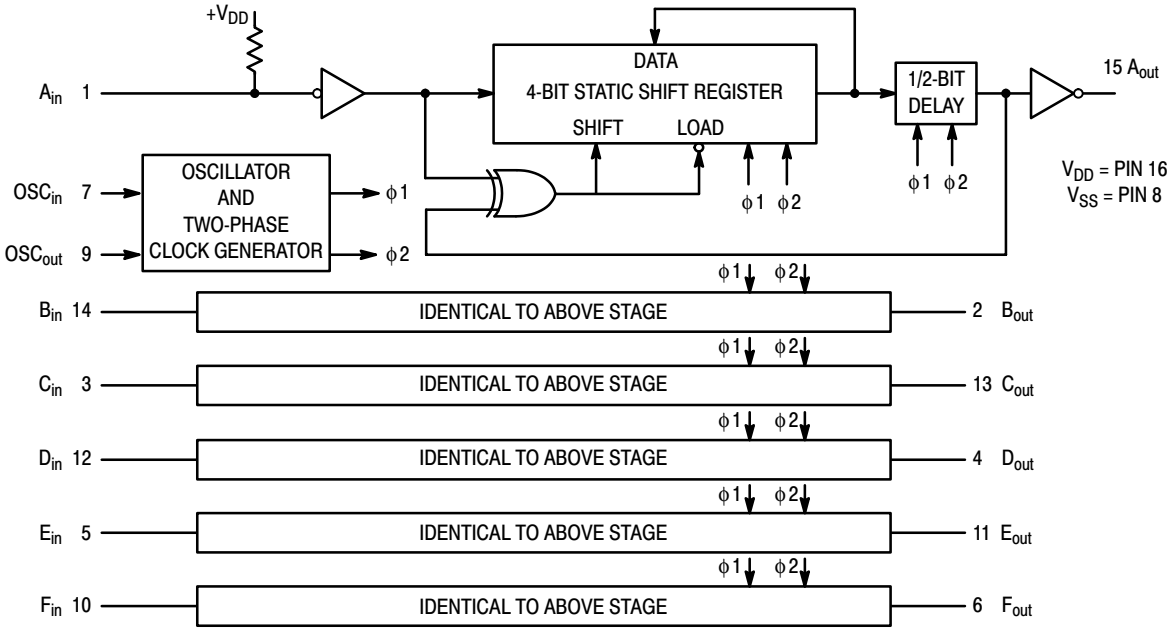
PIN ASSIGNMENT



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55 °C Min	− 55 °C Max	25 °C Min	25 °C Typ (Note 2)	25 °C Max	125 °C Min	125 °C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) “1 Level” (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current Oscillator Output Source Pin 9 (V_{OH} = 2.5 V) (V_{OH} = 4.6 V) (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)	I_{OH}	5.0 5.0 10 15	− 0.6 − 0.12 − 0.23 − 1.4	− − − −	− 0.5 − 0.1 − 0.2 − 1.2	− 1.5 − 0.3 − 0.8 − 3.0	− − − −	− 0.4 − 0.08 − 0.16 − 1.0	− − − −	mAdc
Debounce Outputs (V_{OH} = 2.5 V) Pins 2, 4, 6, (V_{OH} = 4.6 V) 11, 13, 15 (V_{OH} = 9.5 V) (V_{OH} = 13.5 V)		5.0 5.0 10 15	− 0.9 − 0.19 − 0.6 1.8	− − − −	− 0.75 − 0.16 − 0.5 − 1.5	− 2.2 − 0.46 − 1.2 − 4.5	− − − −	− 0.6 − 0.12 − 0.4 − 1.2	− − − −	
Oscillator Output Sink Pin 9 (V_{OL} = 0.4 V) (V_{OL} = 0.5 V) (V_{OL} = 1.5 V)	I_{OL}	5.0 10 15	0.36 0.9 4.2	− − −	0.3 0.75 3.5	0.9 2.3 10	− − −	0.24 0.6 2.8	− − −	mAdc
Debounce Outputs (V_{OL} = 0.4 V) Pins 2, 4, 6, (V_{OL} = 0.5 V) 11, 13, 15 (V_{OL} = 1.5 V)		5.0 10 15	2.6 4.0 12	− − −	2.2 3.3 10	4.0 9.0 35	− − −	1.8 2.7 8.1	− − −	
Input Current Debounce Inputs (V_{in} = V_{DD})	I_{IH}	15	−	2.0	−	0.2	2.0	−	11	μAdc
Input Current Oscillator — Pin 7 (V_{in} = V_{SS} or V_{DD})	I_{in}	15	−	± 620	−	± 255	± 400	−	± 250	μAdc
Pullup Resistor Source Current Debounce Inputs (V_{in} = V_{SS})	I_{IL}	5.0 10 15	210 400 600	425 840 1250	140 280 415	190 380 570	255 500 750	70 145 215	225 440 660	μAdc
Input Capacitance	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (V_{in} = V_{SS} or V_{DD}, I_{out} = 0 μA)	I_{SS}	5.0 10 15	− − −	150 280 840	− − −	40 90 225	100 225 650	− − −	90 180 550	μAdc

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

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SWITCHING CHARACTERISTICS (Note 3) (C_L = 50 pF, T_A = 25 °C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 4)	Max	Unit
Output Rise Time All Outputs	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time Oscillator Output	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Debounce Outputs	t_{THL}	5.0 10 15	– – –	60 30 20	120 60 40	
Propagation Delay Time Oscillator Input to Debounce Outputs	t_{PHL}	5.0 10 15	– – –	285 120 95	570 240 190	ns
	t_{PLH}	5.0 10 15	– – –	370 160 120	740 320 240	
Clock Frequency (50% Duly Cycle) (External Clock)	f_{cl}	5.0 10 15	– – –	2.8 6 9	1.4 3.0 4.5	MHz
Setup Time (See Figure 1)	t_{su}	5.0 10 15	100 80 60	50 40 30	– – –	ns
Maximum External Clock Input Rise and Fall Time Oscillator Input	t_r, t_f	5.0 10 15	No Limit			ns
Oscillator Frequency OSC_{out} $C_{ext} \geq 100$ pF* Note: These equations are intended to be a design guide. Laboratory experimentation may be required. Formulas are typically ± 15% of actual frequencies.	f_{osc}, typ	5.0 10 15	$\frac{1.5}{C_{ext}\ (\text{in } \mu F)}$ $\frac{4.5}{C_{ext}\ (\text{in } \mu F)}$ $\frac{6.5}{C_{ext}\ (\text{in } \mu F)}$			Hz

3. The formulas given are for the typical characteristics only at 25 °C.
4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

***POWER-DOWN CONSIDERATIONS**

Large values of C_{ext} may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA, therefore the turn-off time of the power supply must not be faster than $t = (V_{DD} - V_{SS}) \bullet C_{ext}/(10\ mA)$. For example, If $V_{DD} - V_{SS}$ = 15 V and C_{ext} = 1 μF, the power supply must turn off no faster than t = (15 V) • (1 μF) / 10 mA = 1.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

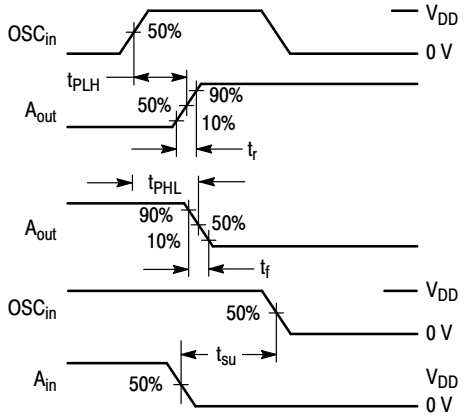

Figure 1. Switching Waveforms

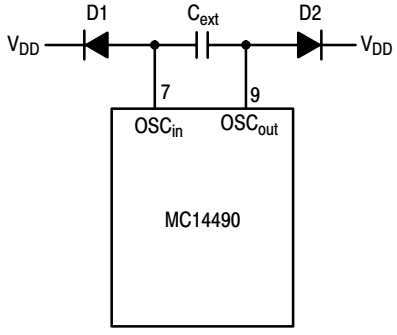

Figure 2. Discharge Protection During Power Down

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THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4-1/2-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is closed, (see Figure 4) the low level is inverted, and the shift register is loaded with a high on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a 3-1/2 to 4-1/2 clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+1 a low is loaded into the first bit. Just after N+1, when the input bounces low, all bits are set to a high. At N+2 nothing happens because the input and output are low and all bits of the shift register are high. At time N+3 and thereafter the input signal is a high, clean signal. At the positive edge of N+6 the output goes high as a result of four lows being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

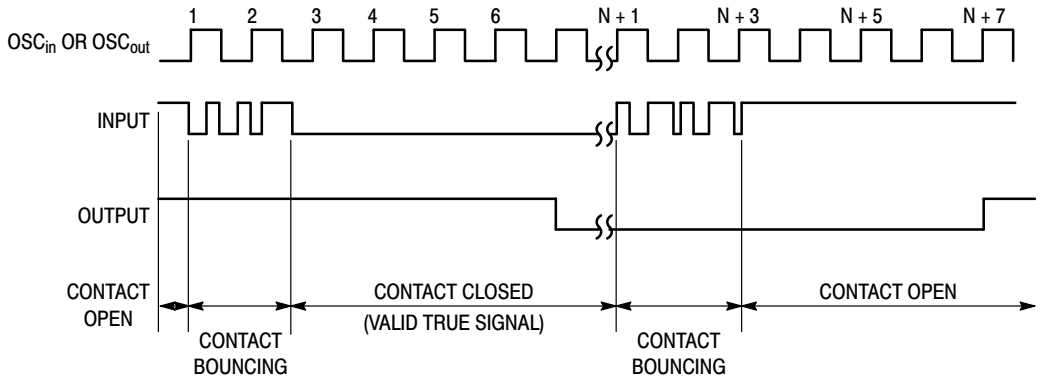

Figure 3. Timing Diagram

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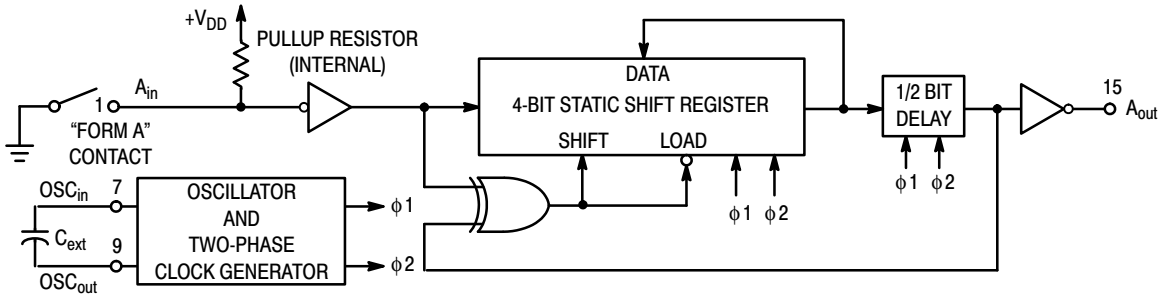

Figure 4. Typical "Form A" Contact Debounce Circuit (Only One Debouncer Shown)

OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

The circuit has a built-in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

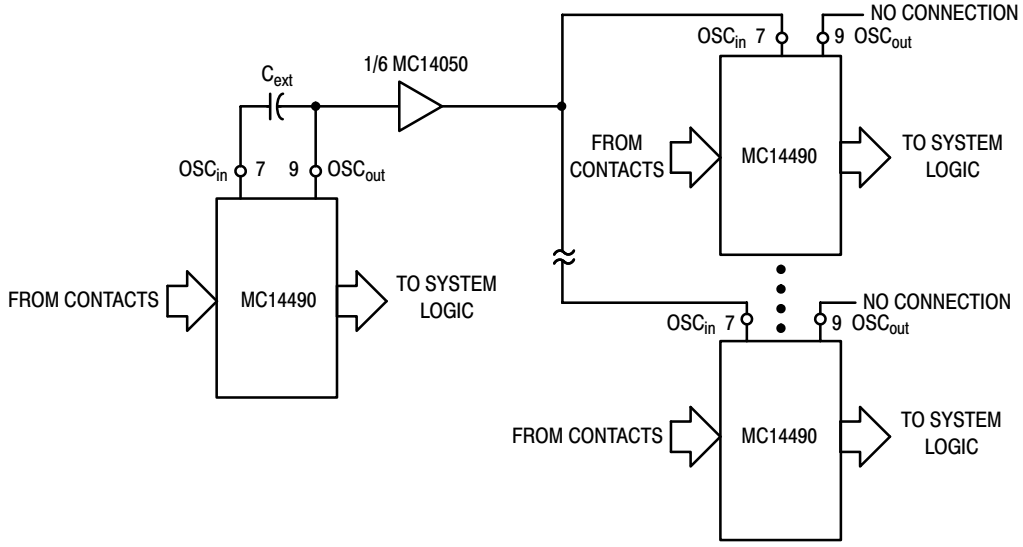

Figure 5. Typical Single Oscillator Debounce System

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TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

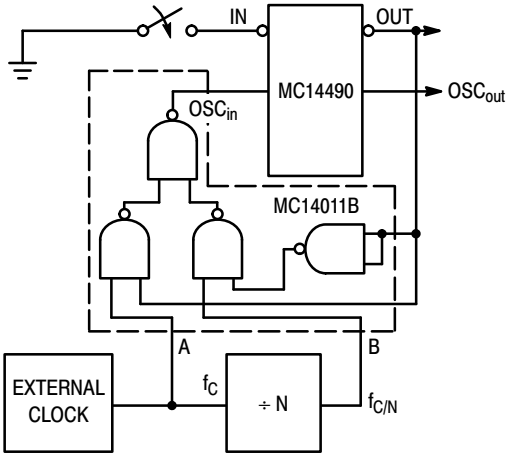

Figure 6. Fast Attack/Slow Release Circuit

LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

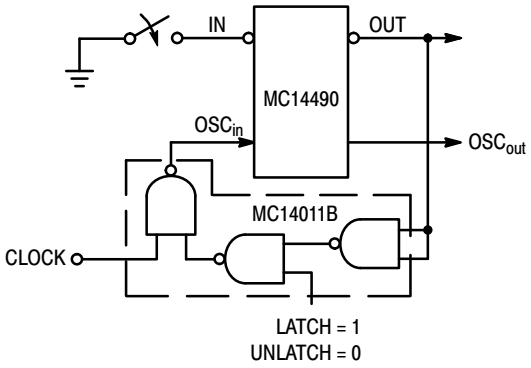

Figure 7. Latched Output Circuit

MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $\overline{A}B$ as shown in Figures 9 and 10. The signal $\overline{A}B$ is four clock periods in length. If the inverter is switched to the A output, the pulse $\overline{A}B$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

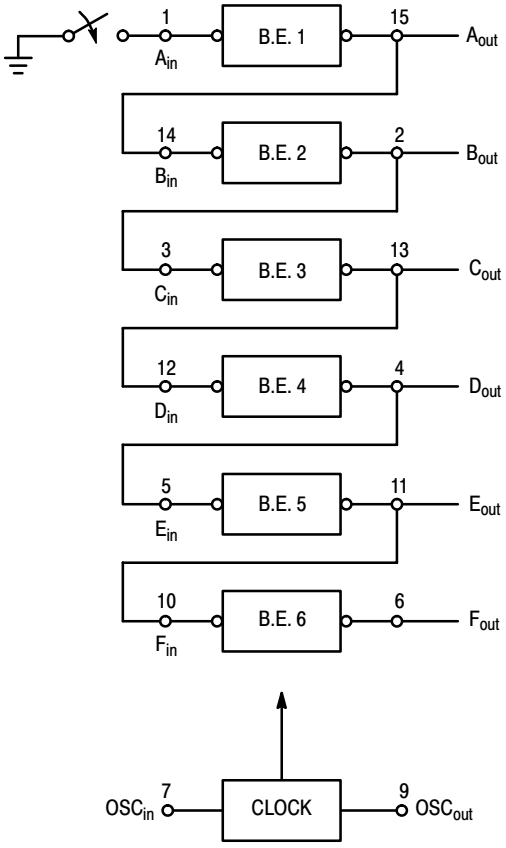

Figure 8. Multiple Timing Circuit Connections

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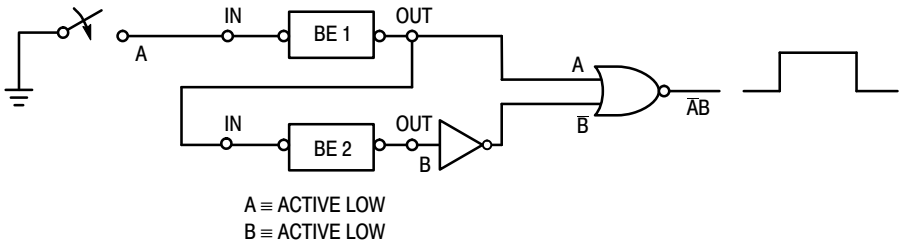

Figure 9. Single Pulse Output Circuit

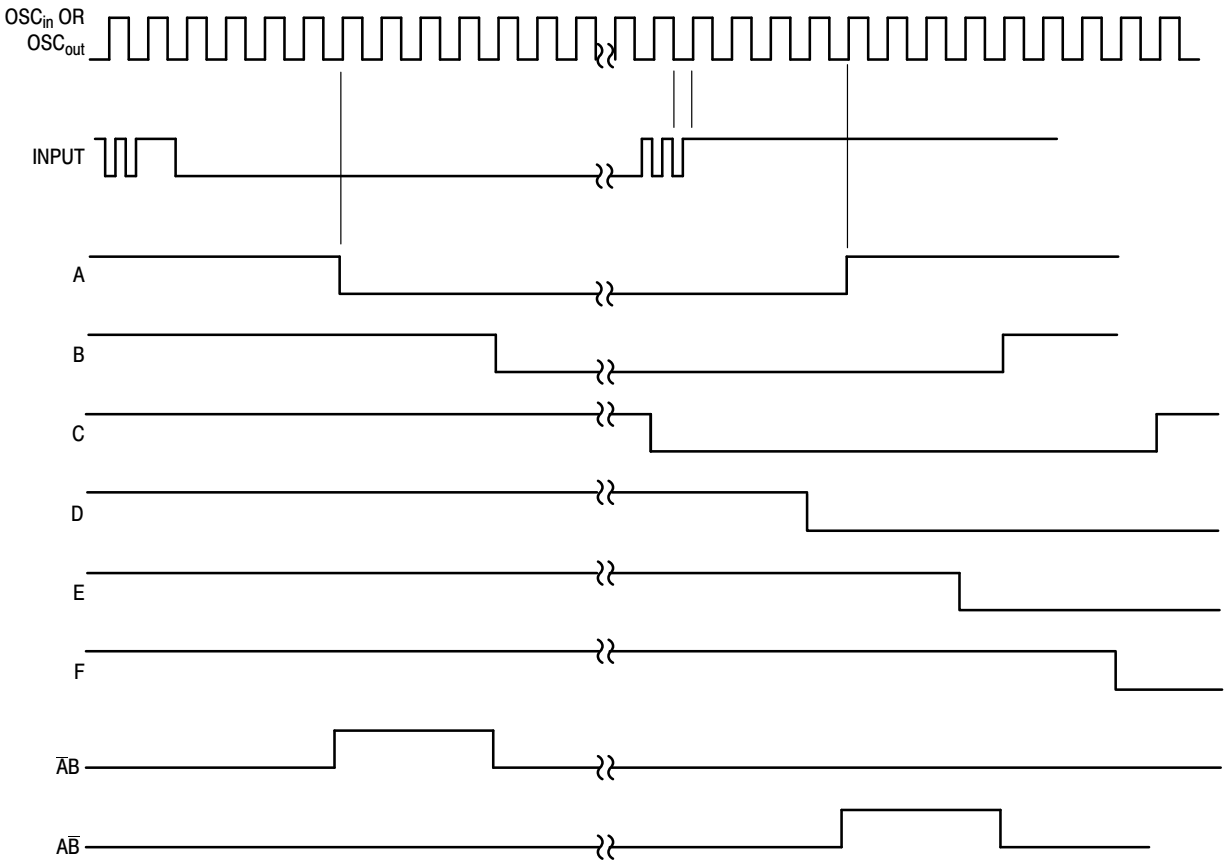

Figure 10. Multiple Output Signal Timing Diagram

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ORDERING INFORMATION

Device	Package	Shipping†
MC14490DWG	SOIC-16 (Pb-Free)	47 Units / Rail
MC14490DWR2G	SOIC-16 (Pb-Free)	1000 / Tape & Reel
NLV14490DWR2G*		

DISCONTINUED (Note 5)

NLV14490DWG*	SOIC-16 (Pb-Free)	47 Units / Rail
MC14490FG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC14490FELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel
MC14490PG	PDIP-16 (Pb-Free)	500 Units / Rail
NLV14490PG*		

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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REVISION HISTORY

Revision	Description of Changes	Date
11	Rebranded the Data Sheet to **onsemi** format. NLV14490DWG, MC14490FG, MC14490FELG, MC14490PG and NLV14490PG OPNs Marked as Discontinued.	8/27/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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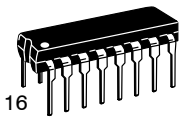

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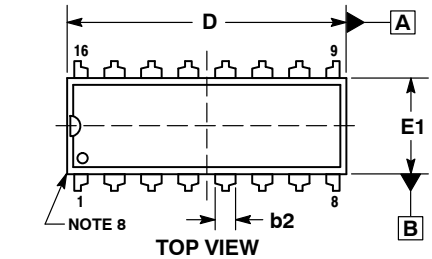
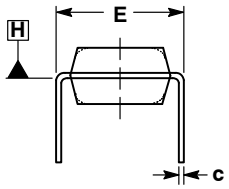
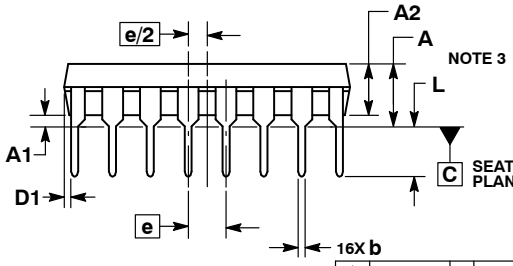


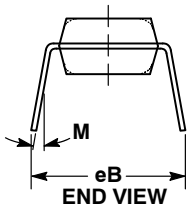
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW
NOTE 6

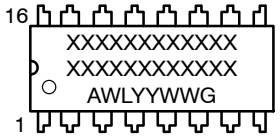
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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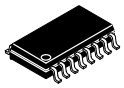
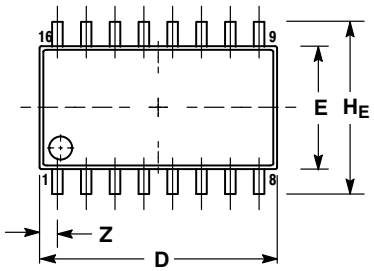
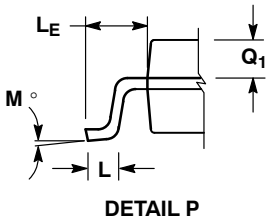
SOEIAJ−16
CASE 966−01
ISSUE A

DATE 27 OCT 2005

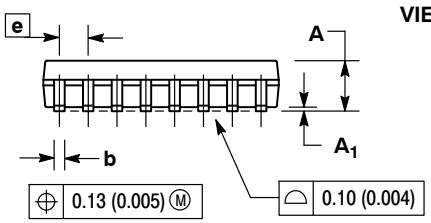


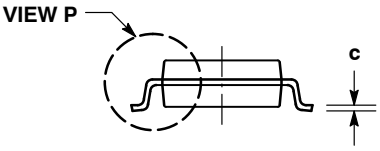
SCALE 1:1





DETAIL P





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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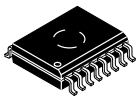

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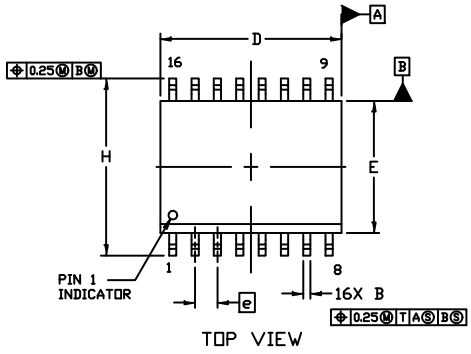
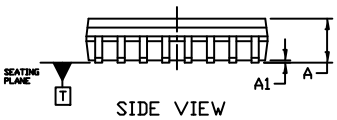
SCALE 1:1

SOIC−16 WB
CASE 751G
ISSUE E

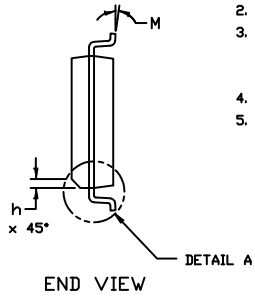
DATE 08 OCT 2021



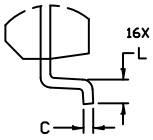
TOP VIEW



SIDE VIEW



END VIEW

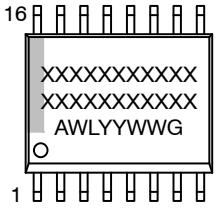


DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

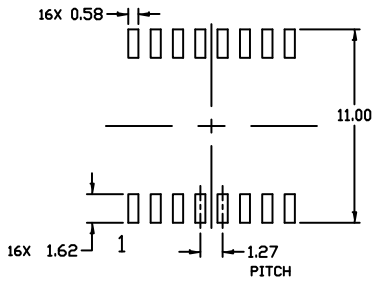
	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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