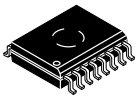
1-to-64 Bit Variable Length Shift Register

MC14557B



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SOIC-16 WB
DW SUFFIX
CASE 751G

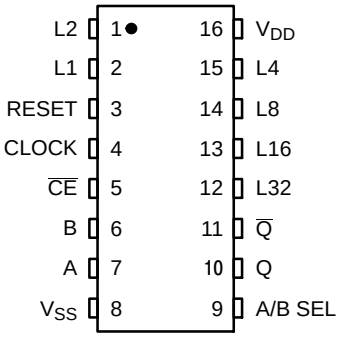
The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

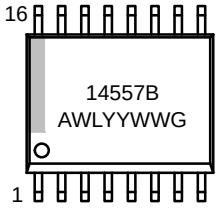
Features

- 1−64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range
- This Device is Pb-Free and is RoHS Compliant

PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
2. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65 °C To 125 °C

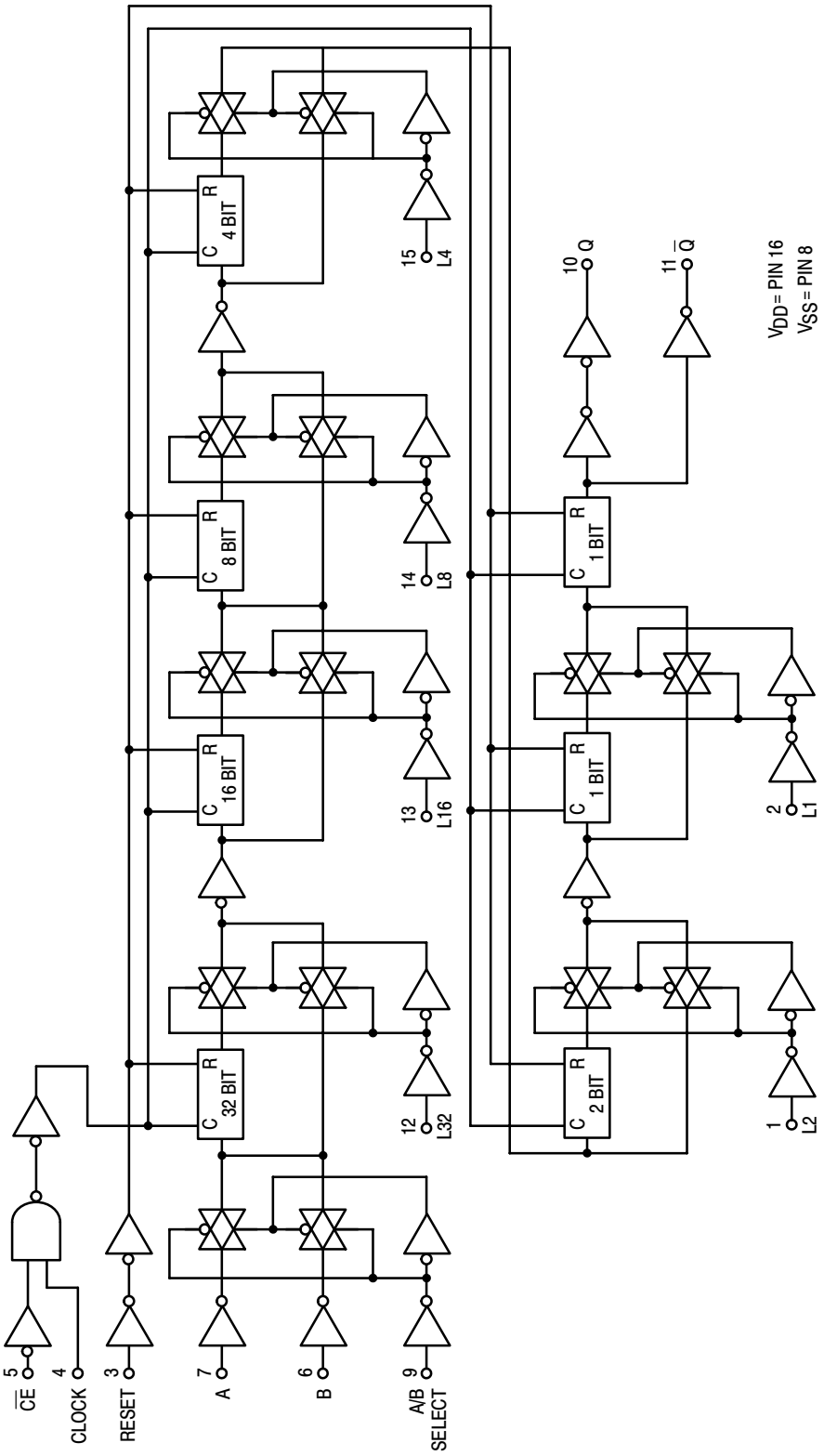


Figure 1. Logic Diagram

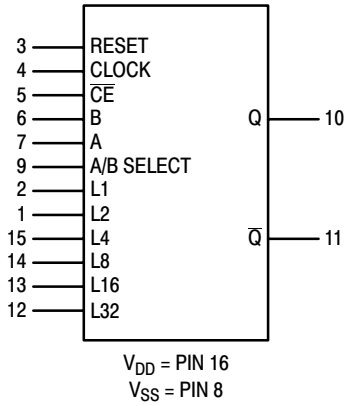


Figure 2. Block Diagram

TRUTH TABLE

Inputs				Output
Rst	**A/B**	**Clock**	**$\overline{CE}$**	**Q**
0	0	⎍	0	B
0	1	⎍	0	A
0	0	1	⎎	B
0	1	1	⎎	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1 Bit
0	0	0	0	0	1	2 Bits
0	0	0	0	1	0	3 Bits
0	0	0	0	1	1	4 Bits
0	0	0	1	0	0	5 Bits
0	0	0	1	0	1	6 Bits
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34 Bits
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	1	1	0	0	61 Bits
1	1	1	1	0	1	62 Bits
1	1	1	1	1	0	63 Bits
1	1	1	1	1	1	64 Bits

NOTE: Length equals the sum of the binary length control subscripts plus one.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic	V_{DD} Vdc	−55 °C Min	−55 °C Max	25 °C Min	25 °C Typ (Note 3)	25 °C Max	125 °C Min	125 °C Max	Unit
V_{OL}	Output Voltage “0” Level V_{in} = V_{DD} or 0	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{OH}	“1” Level V_{in} = 0 or V_{DD}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
V_{IL}	Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	 5.0 10 15	 – – –	 1.5 3.0 4.0	 – – –	 2.25 4.50 6.75	 1.5 3.0 4.0	 – – –	 1.5 3.0 4.0	Vdc
V_{IH}	“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	 5.0 10 15	 3.5 7.0 11	 – – –	 3.5 7.0 11	 2.75 5.50 8.25	 – – –	 3.5 7.0 11	 – – –	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	 5.0 5.0 10 15	 –3.0 –0.64 –1.6 –4.2	 – – – –	 –2.4 –0.51 –1.3 –3.4	 –4.2 –0.88 –2.25 –8.8	 – – – –	 –1.7 –0.36 –0.9 –2.4	 – – – –	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	
I_{in}	Input Current	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
C_{in}	Input Capacitance (V_{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I_{DD}	Quiescent Current (Per Package)	5.0 10 15	– – –	5.0 10 20	– – –	0.010 0.020 0.030	5.0 10 20	– – –	150 300 600	μAdc
I_T	Total Supply Current (Notes 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	5.0 10 15	I_T = (1.75 μA/kHz) f + I_{DD} I_T = (3.50 μA/kHz) f + I_{DD} I_T = (5.25 μA/kHz) f + I_{DD}							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25 °C.
5. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L – 50)$ Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25 °C)

Symbol	Characteristic	V_{DD}	Min	Typ (Note 7)	Max	Unit
t_{TLH}, t_{THL}	Rise and Fall Time, Q or $\overline{Q}$ Output					ns
	t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	5	–	100	200	
	t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns	10	–	50	100	
	t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	15	–	40	80	
t_{PLH}, t_{PHL}	Propagation Delay, Clock or $\overline{CE}$ to Q or $\overline{Q}$					ns
	t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	5	–	300	600	
	t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns	10	–	130	260	
	t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns	15	–	90	180	
t_{PLH}, t_{PHL}	Propagation Delay, Reset to Q or $\overline{Q}$					ns
	t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	5	–	300	600	
	t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns	10	–	130	260	
	t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 70 ns	15	–	95	190	
$t_{WH(cl)}$	Pulse Width, Clock	5	200	95	–	ns
		10	100	45	–	
		15	75	35	–	
$t_{WH(rst)}$	Pulse Width, Reset	5	300	150	–	ns
		10	140	70	–	
		15	100	50	–	
f_{cl}	Clock Frequency (50% Duty Cycle)	5	–	3.0	1.7	MHz
		10	–	7.5	5.0	
		15	–	13.0	6.7	
t_{su}	Setup Time, A or B to Clock or $\overline{CE}$					ns
	Worst case condition: L1 = L2 = L4 = L8 = L16 = L32 = V_{SS} (Register Length = 1)	5	700	350	–	
		10	290	130	–	
		15	145	85	–	
	Best case condition: L32 = V_{DD}, L1 through L16 = Don't Care (Any register length from 33 to 64)	5	400	45	–	
		10	165	5	–	
		15	60	0	–	
t_h	Hold Time, Clock or $\overline{CE}$ to A or B					ns
	Best case condition: L1 = L2 = L4 = L8 = L16 = L32 = V_{SS} (Register Length = 1)	5	200	–150	–	
		10	100	–60	–	
		15	10	–50	–	
	Worst case condition: L32 = V_{DD}, L1 through L16 = Don't Care (Any register length from 33 to 64)	5	400	50	–	
		10	185	25	–	
		15	85	22	–	
t_r, t_f	Rise and Fall Time, Clock	5	No Limit			–
		10				
		15				
t_r, t_f	Rise and Fall Time, Reset or $\overline{CE}$	5	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
t_{rem}	Removal Time, Reset to Clock or $\overline{CE}$	5	160	80	–	ns
		10	80	40	–	
		15	70	35	–	

6. The formulas given are for the typical characteristics only at 25 °C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

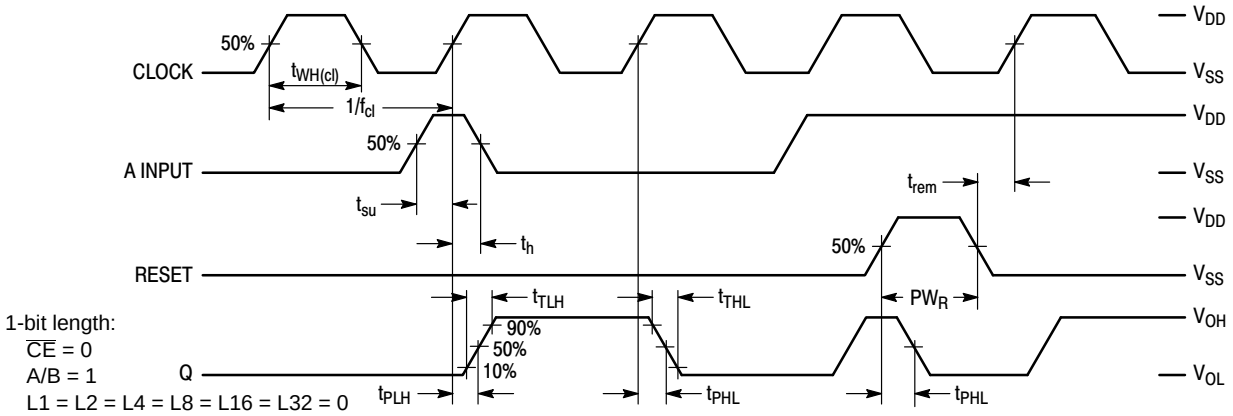


Figure 3. Timing Diagram

ORDERING INFORMATION

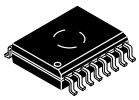
Device	Package	Shipping†
MC14557BDWR2G	SOIC-16 WB (Pb-Free)	1000 / Tape & Reel
MC14557BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

Revision	Description of Changes	Date
9	Rebranded the Data Sheet to **onsemi** format.	10/8/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



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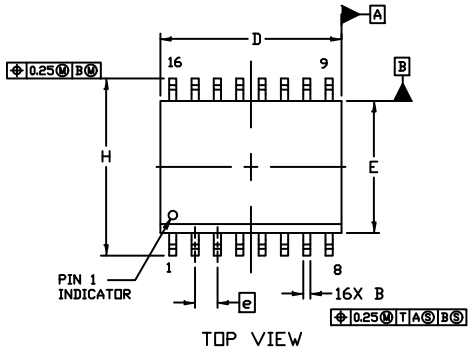
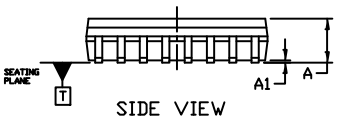
SCALE 1:1

SOIC−16 WB
CASE 751G
ISSUE E

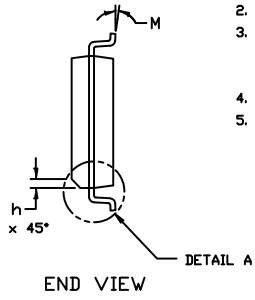
DATE 08 OCT 2021



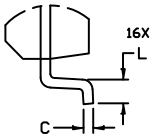
TOP VIEW



SIDE VIEW



END VIEW

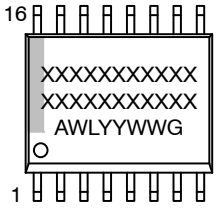


DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

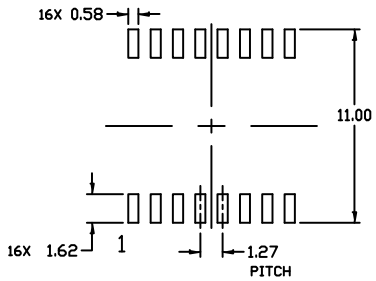
	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

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DESCRIPTION:	**SOIC−16 WB**		**PAGE 1 OF 1**

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