Single Inverter

MC74HC1G04

The MC74HC1G04 is a high speed CMOS inverter fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74HC1G04 output drive current is 1/2 compared to MC74HC series.

Features

- High Speed: t_{PD} = 7 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25 °C
- High Noise Immunity
- Balanced Propagation Delays ($t_{pLH} = t_{pHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL}$ = 2 mA)
- Chip Complexity: < 100 FETs
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

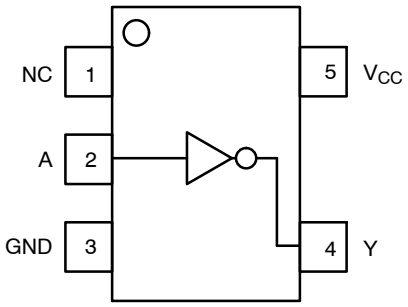


Figure 1. Pinout

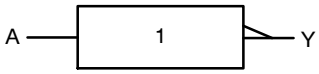
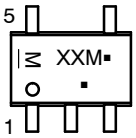


Figure 2. Logic Symbol

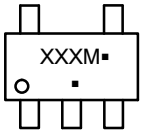
PIN ASSIGNMENT	
1	NC
2	A
3	GND
4	Y
5	V_{CC}

MARKING DIAGRAMS

SC−88A
DF SUFFIX
CASE 419A



SC−74A
DBV SUFFIX
CASE 318BQ



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Input A	Output Y
L	H
H	L

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±20	mA
I_{OUT}	DC Output Source/Sink Current		±12.5	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±25	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SC−88A SC−74A	377 320	°C/W
P_D	Power Dissipation in Still Air at 85 °C	SC−88A SC−74A	332 390	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 20 ounce copper trace with no air flow per JESD51−7.
2. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}	DC Input Voltage		0.0	V_{CC}	V
V_{OUT}	DC Output Voltage		0.0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 2.0 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 6.0 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25 °C Min	T_A = 25 °C Typ	T_A = 25 °C Max	−40 °C ≤ T_A ≤ 85 °C Min	−40 °C ≤ T_A ≤ 85 °C Max	−55 °C ≤ T_A ≤ 125 °C Min	−55 °C ≤ T_A ≤ 125 °C Max	Unit
V_{IH}	High−Level Input Voltage		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.20	– – – –	– – – –	1.5 2.1 3.15 4.20	– – – –	1.5 2.1 3.15 4.20	– – – –	V
V_{IL}	Low−Level Input Voltage		2.0 3.0 4.5 6.0	– – – –	– – – –	0.5 0.9 1.35 1.80	– – – –	0.5 0.9 1.35 1.80	– – – –	0.5 0.9 1.35 1.80	V
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −20 μA	2.0 3.0 4.5 6.0	1.9 2.9 4.4 5.9	2.0 3.0 4.5 6.0	– – – –	1.9 2.9 4.4 5.9	– – – –	1.9 2.9 4.4 5.9	– – – –	V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −2 mA I_{OH} = −2.6 mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	4.08 5.58	– –	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 20 μA	2.0 3.0 4.5 6.0	– – – –	0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1	– – – –	0.1 0.1 0.1 0.1	– – – –	0.1 0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 2 mA I_{OL} = 2.6 mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	– –	0.40 0.40	
I_{IN}	Input Leakage Current	V_{IN} = 6.0 V or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0	–	–	1.0	–	10	–	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	T_A = 25 °C Min	T_A = 25 °C Typ	T_A = 25 °C Max	−40 °C ≤ T_A ≤ 85 °C Min	−40 °C ≤ T_A ≤ 85 °C Max	−55 °C ≤ T_A ≤ 125 °C Min	−55 °C ≤ T_A ≤ 125 °C Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, A to Y	V_{CC} = 5.0 V C_L = 15 pF	–	3.5	15	–	20	–	25	ns
		V_{CC} = 2.0 V C_L = 50 pF V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	– – – –	20 11 8 7	100 27 20 17	– – – –	125 35 25 21	– – – –	155 90 35 26	
t_{TLH}, t_{THL}	Output Transition Time	V_{CC} = 5.0 V C_L = 15 pF	–	3	10	–	15	–	20	ns
		V_{CC} = 2.0 V C_L = 50 pF V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	– – – –	25 16 11 9	125 35 25 21	– – – –	155 45 31 26	– – – –	200 60 38 32	
C_{IN}	Input Capacitance		–	5	10	–	10	–	10	pF

		Typical @ 25 °C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 4)	10	pF

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no−load dynamic power consumption; P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}.

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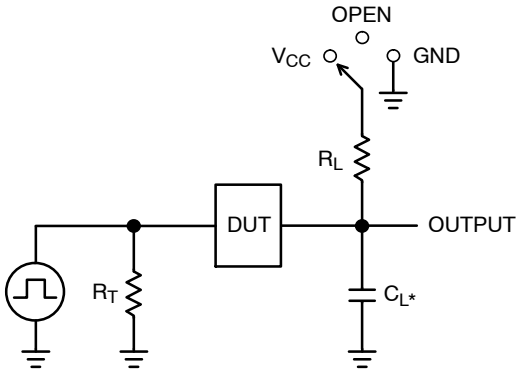

Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{TLH} / t_{THL} (Note 5)	Open		X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X – Don't Care

* C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 W)
f = 1 MHz

Figure 3. Test Circuit

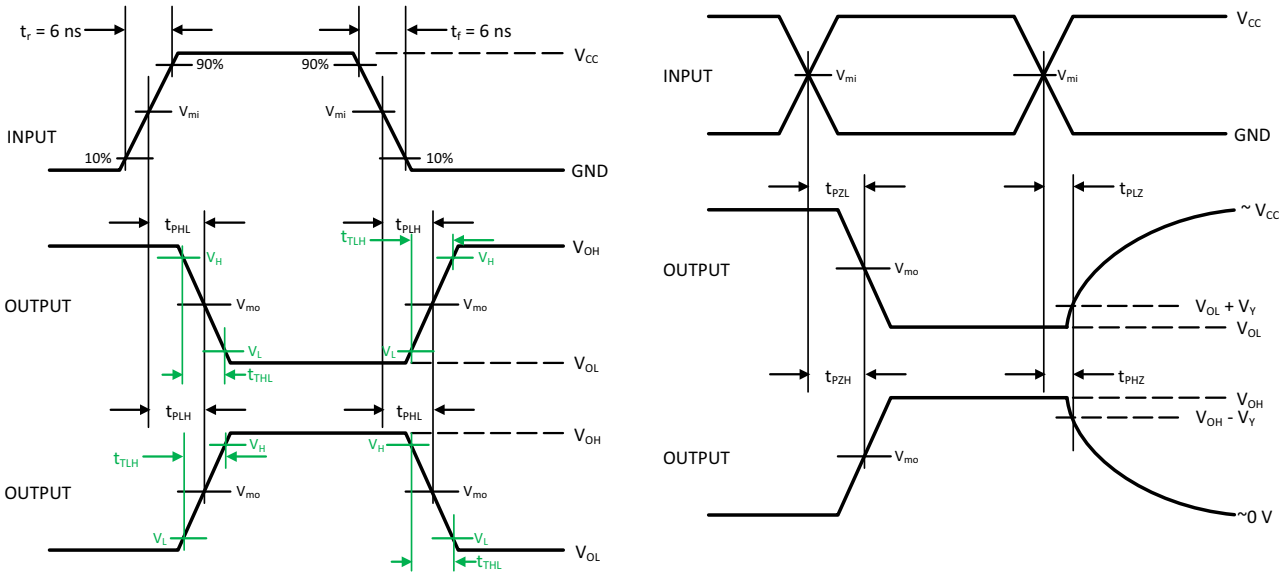

Figure 4. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_L, V	V_H, V	V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}			
3.0 to 3.6	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{OL} + 0.1 (V_{OH} – V_{OL})	V_{OL} + 0.9 (V_{OH} – V_{OL})	0.3
4.5 to 5.5	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{OL} + 0.1 (V_{OH} – V_{OL})	V_{OL} + 0.9 (V_{OH} – V_{OL})	0.3

5. t_{TLH} and t_{THL} are measured from 10% to 90% of (V_{OH} – V_{OL}), and 90% to 10% of (V_{OH} – V_{OL}), respectively.

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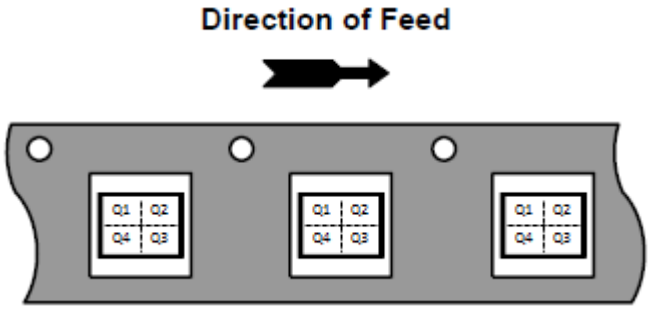
ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
MC74HC1G04DFT1G	SC−88A	H5	Q2	3000 / Tape & Reel
MC74HC1G04DFT1G−Q*	SC−88A	H5	Q2	3000 / Tape & Reel
MC74HC1G04DFT2G	SC−88A	H5	Q4	3000 / Tape & Reel
MC74HC1G04DFT2G−Q*	SC−88A	H5	Q4	3000 / Tape & Reel
MC74HC1G04DBVT1G	SC−74A	H5	Q4	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



REVISION HISTORY

Revision	Description of Changes	Date
16	Revision to remove two ”−Q” OPNs from ordering information table.	1/13/2026
17	Revision to re−enter two ”−Q” OPNs into ordering information table.	4/27/2026

* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

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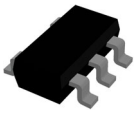
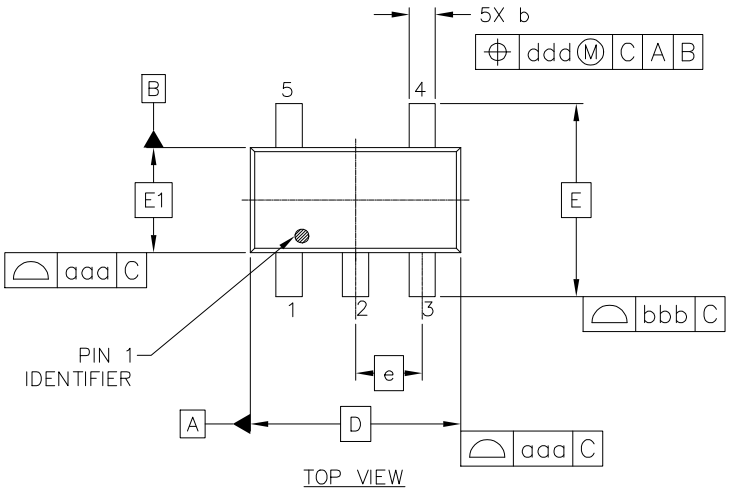
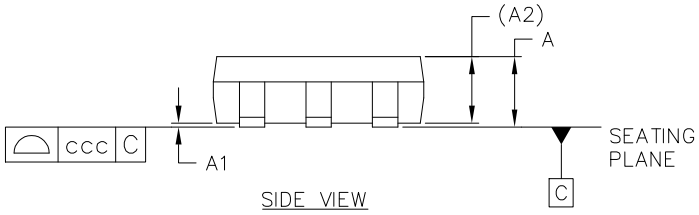


SC−74A−5 3.00x1.50x0.95, 0.95P
CASE 318BQ
ISSUE D

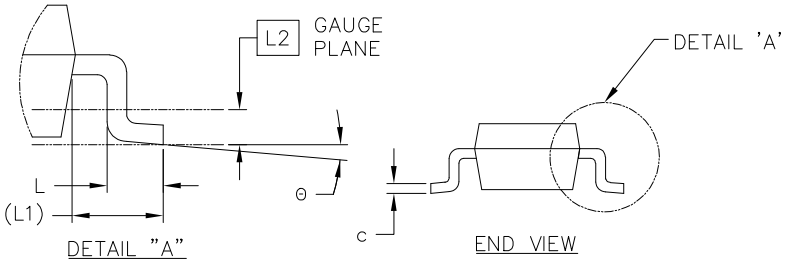
DATE 13 APR 2026



TOP VIEW



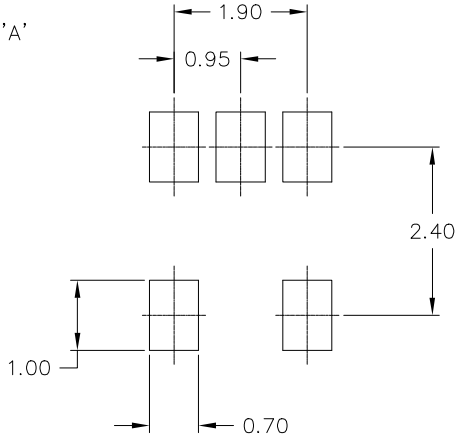
SIDE VIEW



DETAIL "A"
SCALE 2:1

END VIEW

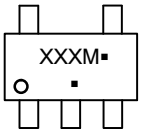
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.05	0.10
A2		0.95 REF	
b	0.25	0.37	0.50
c	0.10	0.18	0.26
D		3.00 BSC	
E		2.75 BSC	
E1		1.50 BSC	
e		0.95 BSC	
L	0.20	0.40	0.60
L1		0.60 REF	
L2		0.25 BSC	
θ	0°	5°	10°
TOLERANCE FORM AND POSITION			
aaa		0.15	
bbb		0.15	
ccc		0.05	
ddd		0.20	



RECOMMENDED MOUNTING FOOTPRINT
*For additional information in our Pb−Free Strategy and Soldering details, Please download the onsemi Soldering and Mounting Techniques Reference manual. SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON66279G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SC−74A−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

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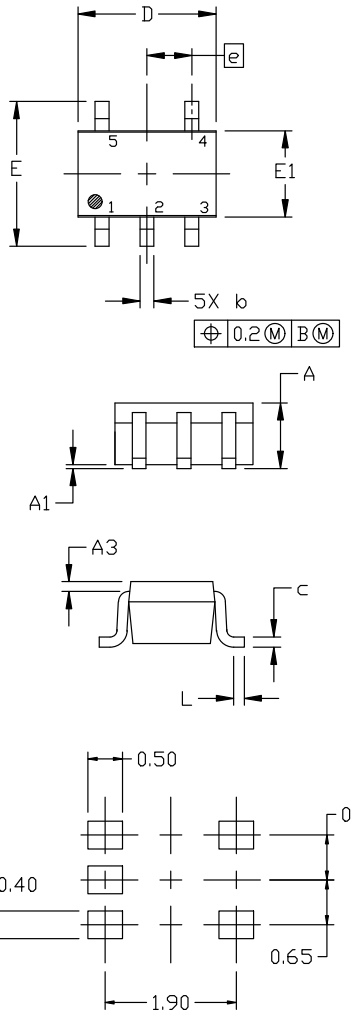
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

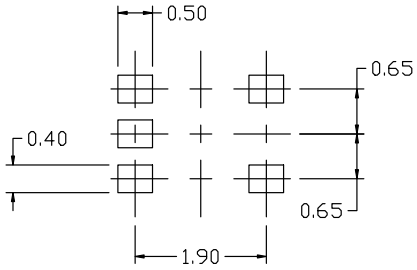
DATE 11 APR 2023

SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

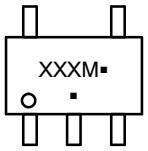
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	**SC−88A (SC−70−5/SOT−353)**	**PAGE 1 OF 1**

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