

# 8-Input NAND Gate

## High-Performance Silicon-Gate CMOS

### MC74HC30A

The MC74HC30 is identical in pinout to the LS30. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

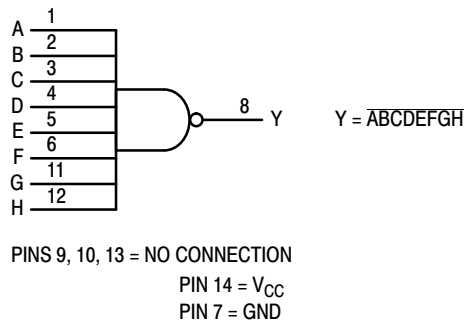


Figure 1. Logic Diagram

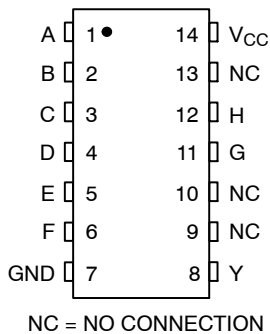
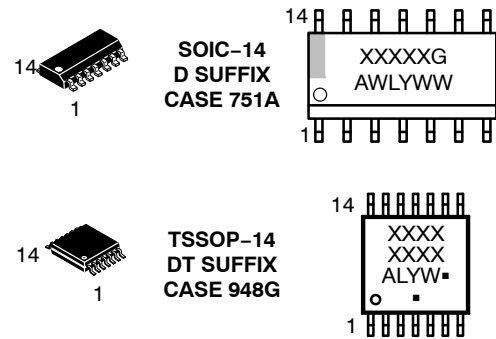


Figure 2. Pinout Diagram (Top View)

#### MARKING DIAGRAMS



XXXX = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

| Inputs A through H   | Output Y |
|----------------------|----------|
| All inputs H         | L        |
| One or more inputs L | H        |

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC74HC30A

## MAXIMUM RATINGS

| Symbol           | Parameter                                                                          | Value                                                    | Unit |
|------------------|------------------------------------------------------------------------------------|----------------------------------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage                                                                  | −0.5 to +6.5                                             | V    |
| V <sub>IN</sub>  | DC Input Voltage                                                                   | −0.5 to V <sub>CC</sub> + 0.5                            | V    |
| V <sub>OUT</sub> | DC Output Voltage                                                                  | −0.5 to V <sub>CC</sub> + 0.5                            | V    |
| I <sub>IN</sub>  | DC Input Current, per Pin                                                          | ±20                                                      | mA   |
| I <sub>OUT</sub> | DC Output Current, per Pin                                                         | ±25                                                      | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                    | ±50                                                      | mA   |
| I <sub>IK</sub>  | Input Clamp Current (V <sub>IN</sub> < 0 or V <sub>IN</sub> > V <sub>CC</sub> )    | ±20                                                      | mA   |
| I <sub>OK</sub>  | Output Clamp Current (V <sub>OUT</sub> < 0 or V <sub>OUT</sub> > V <sub>CC</sub> ) | ±20                                                      | mA   |
| T <sub>STG</sub> | Storage Temperature                                                                | −65 to +150                                              | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds                                    | 260                                                      | °C   |
| T <sub>J</sub>   | Junction Temperature Under Bias                                                    | ±150                                                     | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Note 1)                                                        | SOIC−14<br>TSSOP−14<br>116<br>150                        | °C/W |
| P <sub>D</sub>   | Power Dissipation in Still Air at 25°C                                             | SOIC−14<br>TSSOP−14<br>1077<br>833                       | mW   |
| MSL              | Moisture Sensitivity                                                               | Level 1                                                  | –    |
| F <sub>R</sub>   | Flammability Rating                                                                | Oxygen Index: 28 to 34<br>UL 94 V−0 @<br>0.125 in        | –    |
| V <sub>ESD</sub> | ESD Withstand Voltage (Note 2)                                                     | Human Body Model<br>Charged Device Model<br>>2000<br>N/A | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                                     | Min                                                                                          | Max                | Unit |
|------------------------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------|--------------------|------|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                         | 2.0                                                                                          | 6.0                | V    |
| V <sub>IN</sub> , V <sub>OUT</sub> | DC Input Voltage, Output Voltage (Referenced to GND) (Note 3) | 0                                                                                            | V <sub>CC</sub>    | V    |
| T <sub>A</sub>                     | Operating Free-Air Temperature                                | −55                                                                                          | +125               | °C   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise or Fall Time                                       | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V<br>0<br>0<br>0 | 1000<br>500<br>400 | ns   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

# MC74HC30A

## DC ELECTRICAL CHARACTERISTICS

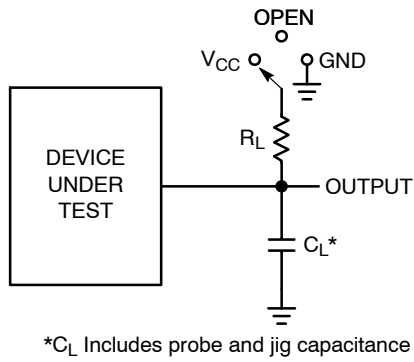
| Symbol          | Parameter                                      | Test Conditions                                                                                                   | V <sub>CC</sub><br>V | Guaranteed Limit   |                    |                    | Unit |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|----------------------|--------------------|--------------------|--------------------|------|
|                 |                                                |                                                                                                                   |                      | - 55 to<br>25°C    | ≤ 85°C             | ≤ 125°C            |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                | 2.0<br>4.5<br>6.0    | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                | 2.0<br>4.5<br>6.0    | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | 0.3<br>0.9<br>1.2  | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                               | 2.0<br>4.5<br>6.0    | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | 1.9<br>4.4<br>5.9  | V    |
|                 |                                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 4.5<br>6.0           | 3.98<br>5.48       | 3.84<br>5.34       | 3.70<br>5.20       |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                               | 2.0<br>4.5<br>6.0    | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | 0.1<br>0.1<br>0.1  | V    |
|                 |                                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 4.5<br>6.0           | 0.26<br>0.26       | 0.33<br>0.33       | 0.40<br>0.40       |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                          | 6.0                  | ± 0.1              | ± 1.0              | ± 1.0              | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                               | 6.0                  | 2                  | 20                 | 40                 | μA   |

## AC ELECTRICAL CHARACTERISTICS

| Symbol                                 | Parameter                                                             | V <sub>CC</sub><br>V | Guaranteed Limit |                 |                 | Unit |
|----------------------------------------|-----------------------------------------------------------------------|----------------------|------------------|-----------------|-----------------|------|
|                                        |                                                                       |                      | - 55 to<br>25°C  | ≤ 85°C          | ≤ 125°C         |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Any Input to Output Y<br>(Figures 3 and 4) | 2.0<br>4.5<br>6.0    | 175<br>35<br>30  | 220<br>44<br>37 | 265<br>53<br>45 | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 3 and 4)       | 2.0<br>4.5<br>6.0    | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                             | –                    | 10               | 10              | 10              | pF   |

|                 |                                          |                                         |    |
|-----------------|------------------------------------------|-----------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Gate) | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|                 |                                          | 27                                      |    |

# MC74HC30A



| Test                                | Switch Position | C <sub>L</sub> | R <sub>L</sub> |
|-------------------------------------|-----------------|----------------|----------------|
| t <sub>PLH</sub> / t <sub>PHL</sub> | Open            | 50 pF          | 1 kΩ           |
| t <sub>PLZ</sub> / t <sub>PZL</sub> | V <sub>CC</sub> |                |                |
| t <sub>PHZ</sub> / t <sub>PZH</sub> | GND             |                |                |

Figure 3. Test Circuit

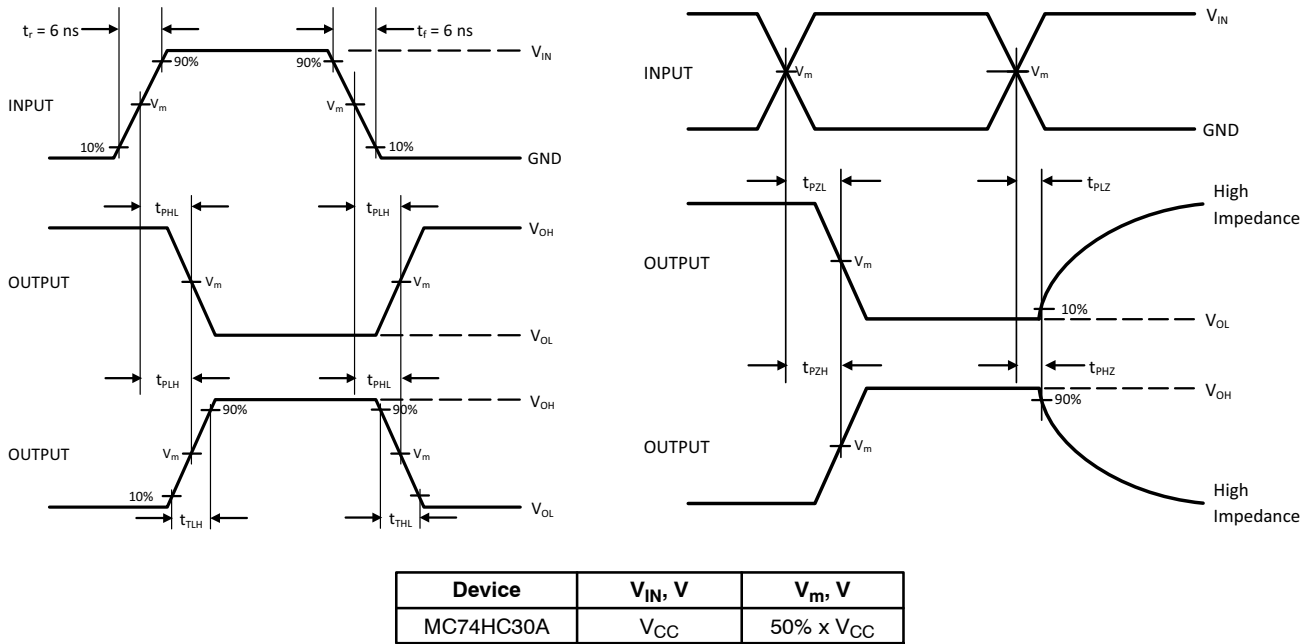


Figure 4. Switching Waveforms

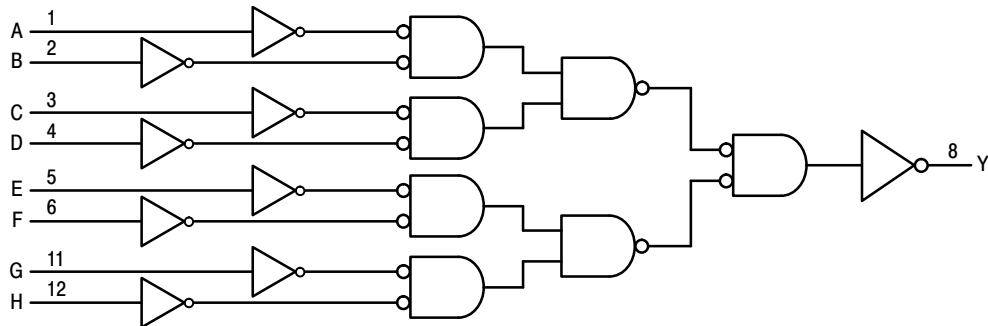


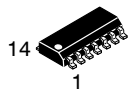
Figure 5. Expanded Logic Diagram

## MC74HC30A

### ORDERING INFORMATION

| Device         | Marking   | Package  | Shipping <sup>†</sup> |
|----------------|-----------|----------|-----------------------|
| MC74HC30ADR2G  | HC30A     | SOIC-14  | 2500 / Tape & Reel    |
| MC74HC30ADTR2G | HC<br>30A | TSSOP-14 | 2500 / Tape & Reel    |

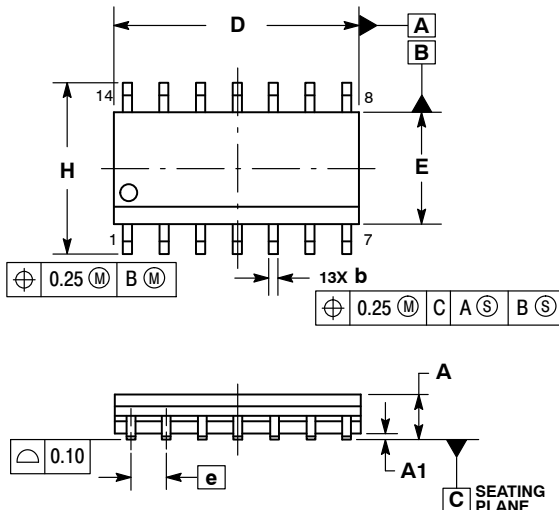
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

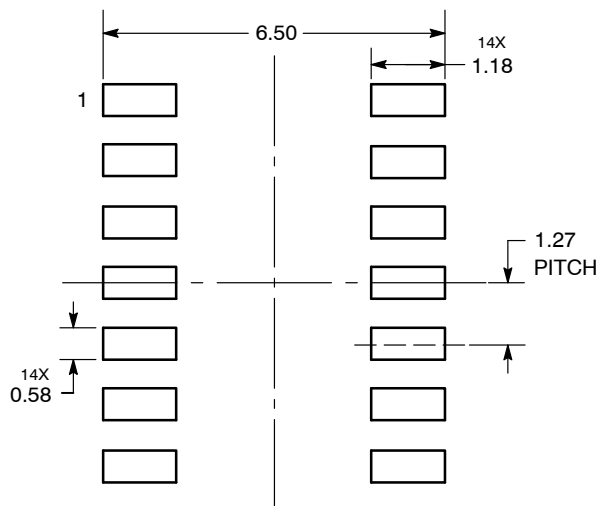


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

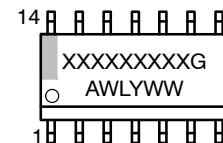
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                     |
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SOIC-14  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

STYLE 1:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 2:  
CANCELLED

STYLE 3:  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

STYLE 4:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 5:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

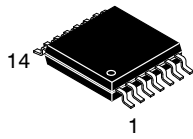
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PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

STYLE 7:  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

STYLE 8:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

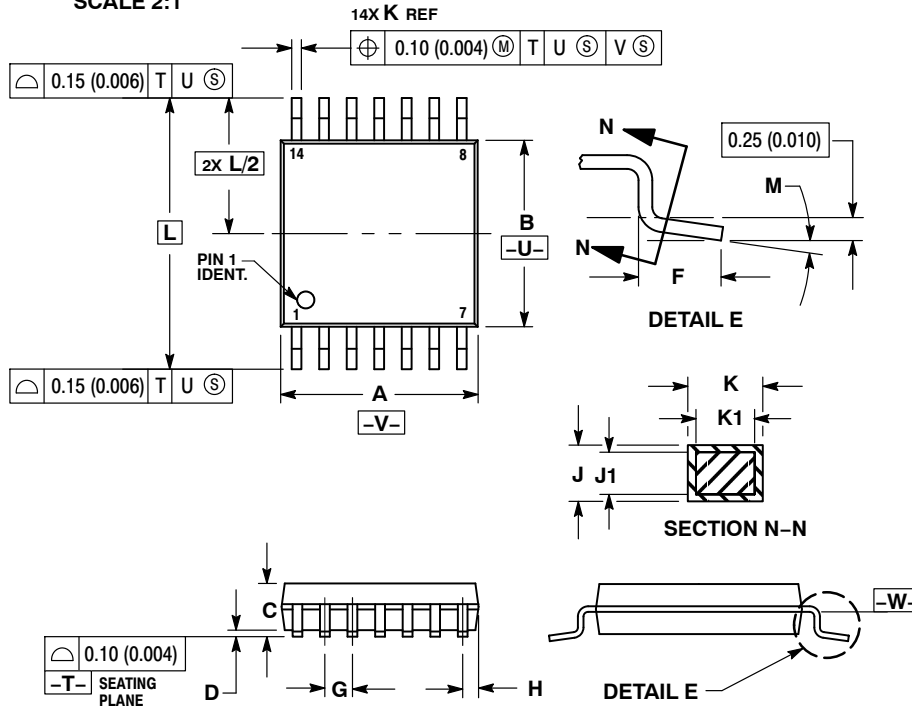
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**TSSOP-14 WB**  
**CASE 948G**  
**ISSUE C**

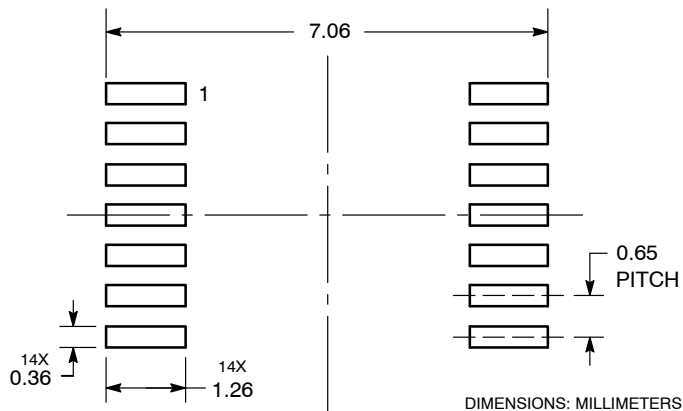
DATE 17 FEB 2016

SCALE 2:1

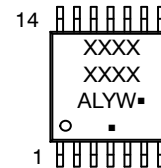

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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