Low-Voltage CMOS 16-Bit Transceiver

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16245

The MC74LCX16245 is a high performance, non-inverting 16-bit transceiver operating from a 1.65 to 5.5 V supply. The device is byte controlled. Each byte has separate Output Enable inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX16245 inputs to be safely driven from 5.0 V devices. The MC74LCX16245 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

The 4.5 ns maximum propagation delays support high performance applications. Current drive capability is 24 mA at V_{CC} = 3.0 V for both A and B ports. The Transmit/Receive (T/$\overline{R}$n) inputs determine the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B to A ports. The Output Enable inputs ($\overline{OEn}$), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

Features

- Designed for 1.65 to 5.5 V V_{CC} Operation
- 4.5 ns Maximum t_{pd}
- 5.0 V Tolerant − Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability at V_{CC} = 3 V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
  - Human Body Model >2000 V
- These Devices are Pb-Free and are RoHS Compliant

**TSSOP-48
DT SUFFIX
CASE 1201**

MARKING DIAGRAM
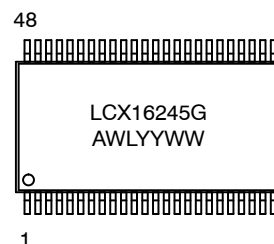
LCX16245G
AWLYYWW

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

MC74LCX16245

T/R̅1	1	48	O̅E̅1
B0	2	47	A0
B1	3	46	A1
GND	4	45	GND
B2	5	44	A2
B3	6	43	A3
V_CC	7	42	V_CC
B4	8	41	A4
B5	9	40	A5
GND	10	39	GND
B6	11	38	A6
B7	12	37	A7
B8	13	36	A8
B9	14	35	A9
GND	15	34	GND
B10	16	33	A10
B11	17	32	A11
V_CC	18	31	V_CC
B12	19	30	A12
B13	20	29	A13
GND	21	28	GND
B14	22	27	A14
B15	23	26	A15
T/R̅2	24	25	O̅E̅2
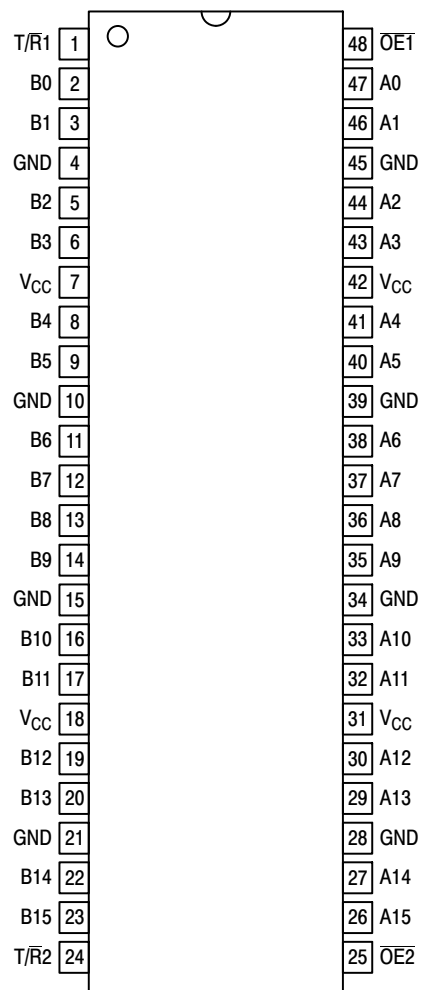
Figure 1. Pinout: 48-Lead (Top View)

Table 1. PIN NAMES

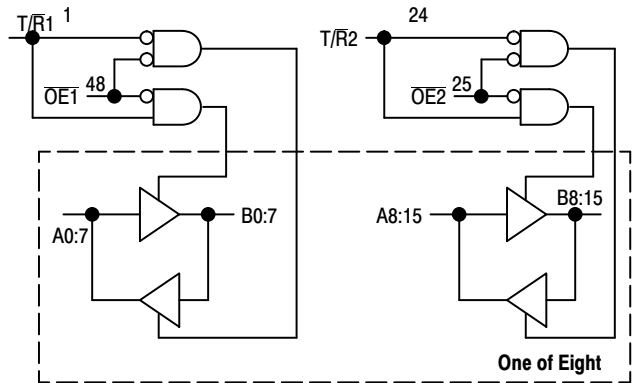| Pins	Function
O̅E̅n	Output Enable Inputs
T/R̅n	Transmit/Receive Inputs
A0 – A15	Side A Inputs or 3-State Outputs
B0 – B15	Side B Inputs or 3-State Outputs

Figure 2. Logic Diagram

TRUTH TABLE

Inputs		Outputs	Inputs		Outputs
O̅E̅1	T/R̅1		O̅E̅2	T/R̅2	
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	H	Bus A0:7 Data to Bus B0:7	L	H	Bus A8:15 Data to Bus B8:15
H	X	High Z State on A0:7, B0:7	H	X	High Z State on A8:15, B8:15

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions Are Acceptable; for I_CC reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V$_{CC}$	DC Supply Voltage		−0.5 to +6.5	V
V$_{IN}$	DC Input Voltage (Note 1)		−0.5 to +6.5	V
V$_{OUT}$	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V$_{CC}$ = 0 V)	−0.5 to V$_{CC}$ + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I$_{IK}$	DC Input Diode Current	V$_{IN}$ < GND	−50	mA
I$_{OK}$	DC Output Diode Current	V$_{OUT}$ < GND	−50	mA
I$_O$	DC Output Source/Sink Current		±50	mA
I$_{CC}$	DC Supply Current per Supply Pin		±100	mA
I$_{GND}$	DC Supply Current per Ground Pin		±100	mA
T$_{STG}$	Storage Temperature Range		−65 to +150	°C
T$_L$	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T$_J$	Junction Temperature Under Bias		+150	°C
θ$_{JA}$	Thermal Resistance (Note 2)		71	°C/W
P$_D$	Power Dissipation in Still Air		1765	mW
MSL	Moisture Sensitivity		Level 1	–
F$_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	–
V$_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	>2000 N/A	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. I$_O$ absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V$_{CC}$	Supply Voltage	Operating Data Retention Only	1.65 1.5	2.5, 3.3 2.5, 3.3	5.5 5.5	V
V$_{IN}$	Digital Input Voltage		0	–	5.5	V
V$_{OUT}$	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode (V$_{CC}$ = 0 V)	0 0 0	– – –	V$_{CC}$ 5.5 5.5	V
T$_A$	Operating Free-Air Temperature		−40	–	+125	°C
t$_r$, t$_f$	Input Rise or Fall Rate	V$_{CC}$ = 1.65 V to 1.95 V V$_{CC}$ = 2.3 V to 2.7 V V$_{IN}$ from 0.8 V to 2.0 V, V$_{CC}$ = 3.0 V V$_{CC}$ = 4.5 V to 5.5 V	0 0 0 0	– – – –	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V$_{CC}$). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40\,°C$ to $+85\,°C$ Min	$T_A = -40\,°C$ to $+85\,°C$ Max	$T_A = -55\,°C$ to $+125\,°C$ Min	$T_A = -55\,°C$ to $+125\,°C$ Max	Unit
V_{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}	–	0.65 x V_{CC}	–	V
			2.3 to 2.7	1.7	–	1.7	–	
			2.7 to 3.6	2.0	–	2.0	–	
			4.5 to 5.5	0.7 x V_{CC}	–	0.7 x V_{CC}	–	
V_{IL}	Low-Level Input Voltage		1.65 to 1.95	–	0.35 x V_{CC}	–	0.35 x V_{CC}	V
			2.3 to 2.7	–	0.7	–	0.7	
			2.7 to 3.6	–	0.8	–	0.8	
			4.5 to 5.5	–	0.3 x V_{CC}	–	0.3 x V_{CC}	
V_{OH}	High-Level Output Voltage	$V_I = V_{IH}$ or V_{IL} $I_{OH} = -100\ \mu A$ $I_{OH} = -4$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA $I_{OH} = -16$ mA $I_{OH} = -24$ mA $I_{OH} = -32$ mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	$V_{CC} - 0.1$ 1.2 1.8 2.2 2.4 2.2 3.8	– – – – – – –	$V_{CC} - 0.1$ 1.2 1.8 2.2 2.4 2.2 3.8	– – – – – – –	V
V_{OL}	Low-Level Output Voltage	$V_I = V_{IH}$ or V_{IL} $I_{OH} = -100\ \mu A$ $I_{OH} = -4$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA $I_{OH} = -16$ mA $I_{OH} = -24$ mA $I_{OH} = -32$ mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	– – – – – – –	0.1 0.45 0.6 0.4 0.4 0.55 0.6	– – – – – – –	0.1 0.45 0.6 0.4 0.4 0.55 0.6	V
I_I	Input Leakage Current	$V_I = 0$ to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I_{OZ}	3-State Output Leakage Current	$V_I = V_{IH}$ or V_{IL}, $V_O = 0$ V to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I_{OFF}	Power Off Leakage Current	$V_I = 5.5$ V or $V_O = 5.5$ V	0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	$V_I = 5.5$ V or GND	3.6	–	10	–	10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6$ V	2.3 to 3.6	–	500	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	$T_A = -40\,°C$ to $+85\,°C$ Min	Max	$T_A = -55\,°C$ to $+125\,°C$ Min	Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay, D to O	See Figures 3 and 4	1.65 to 1.95	–	8.5	–	8.5	ns
			2.3 to 2.7	–	5.4	–	5.4	
			2.7	–	5.2	–	5.2	
			3.0 to 3.6	–	4.5	–	4.5	
			4.5 to 5.5	–	4.0	–	4.0	
t_{PZH}, t_{PZL}	Output Enable Time, $\overline{OE}$ to O	See Figures 3 and 4	1.65 to 1.95	–	10.5	–	10.5	ns
			2.3 to 2.7	–	8.5	–	8.5	
			2.7	–	7.2	–	7.2	
			3.0 to 3.6	–	6.5	–	6.5	
			4.5 to 5.5	–	5.5	–	5.5	
t_{PHZ}, t_{PLZ}	Output Disable Time, $\overline{OE}$ to O	See Figures 3 and 4	1.65 to 1.95	–	9.7	–	9.7	ns
			2.3 to 2.7	–	7.7	–	7.7	
			2.7	–	6.9	–	6.9	
			3.0 to 3.6	–	6.4	–	6.4	
			4.5 to 5.5	–	5.4	–	5.4	
t_{OSHL}, t_{OSLH}	Output to Output Skew, (Note 5)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25\,°C$ Min	Typ	Max	Units
V_{OLP}	Dynamic LOW Peak Voltage (Note 6)	$V_{CC} = 3.3$ V, $C_L = 50$ pF, $V_{IH} = 3.3$ V, $V_{IL} = 0$ V $V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = 2.5$ V, $V_{IL} = 0$ V		0.8 0.6		V V
V_{OLV}	Dynamic LOW Valley Voltage (Note 6)	$V_{CC} = 3.3$ V, $C_L = 50$ pF, $V_{IH} = 3.3$ V, $V_{IL} = 0$ V $V_{CC} = 2.5$ V, $C_L = 30$ pF, $V_{IH} = 2.5$ V, $V_{IL} = 0$ V		−0.8 −0.6		V V

6. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3$ V, $V_I = 0$ V or V_{CC}	20	pF

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Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND
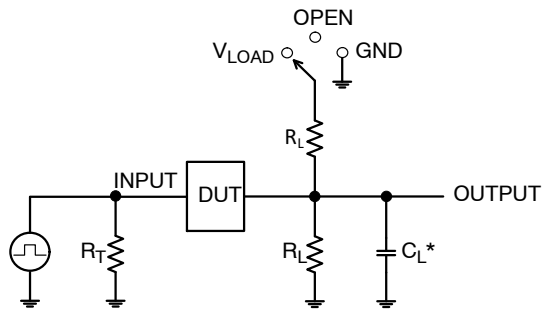
C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit
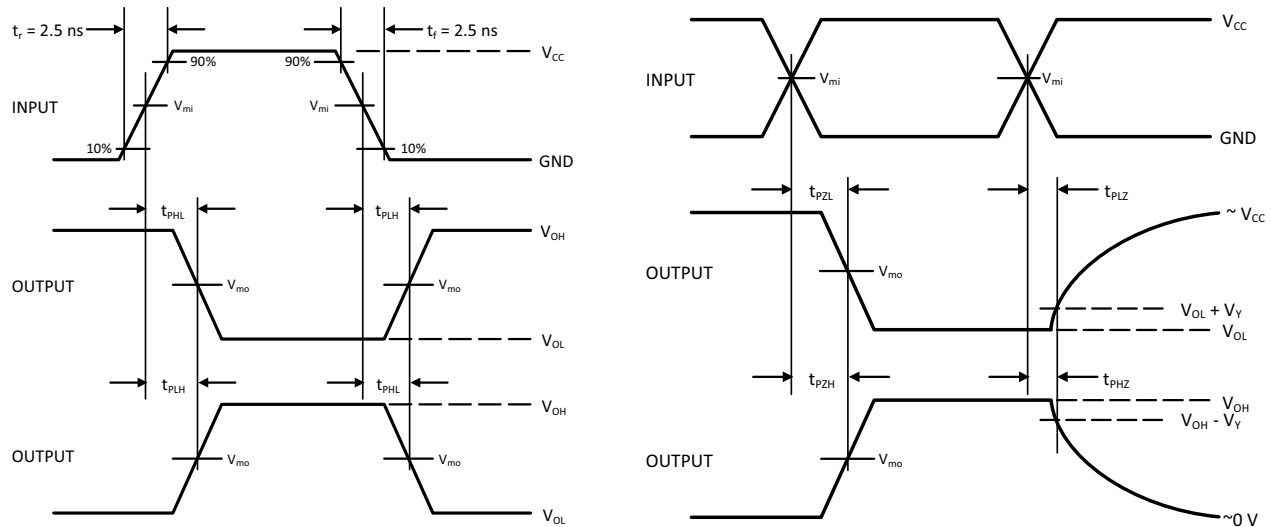
V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_{mi}, V	V_{mo}, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	2 x V_{CC}	$V_{CC}/2$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	$V_{CC}/2$	0.3
3.0 to 3.6	500	50	6 V	1.5	$V_{CC}/2$	0.3
4.5 to 4.5	500	50	2 x V_{CC}	$V_{CC}/2$	$V_{CC}/2$	0.3

Figure 4. Switching Waveforms

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74LCX16245DTR2G	TSSOP-48*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb-Free.

MC74LCX16245

Revision	Description of Changes	Date
11	Update formatting, revive from obsolete, replace five page 1 values, delete one bullet and edit another, replace all tables on pages 3 and 4, edit AC table values, replace figures 3 and 4	7/8/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.
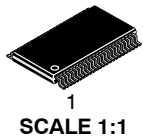
TSSOP−48
CASE 1201
ISSUE B

DATE 06 JUL 2010

SCALE 1:1

1

48X K REF

⊕ 0.12 (0.005) Ⓜ T U Ⓢ V Ⓢ

Ⓣ U Ⓢ
0.254 (0.010) Ⓜ T
L

48   25

B
−U−

24

PIN 1
IDENT.

A
−V−

K
K1

J J1

SECTION N−N

N

N

F M

DETAIL E 0.25 (0.010)

D
C

0.076 (0.003)
−T− **SEATING
PLANE**

G H

−W−

DETAIL E
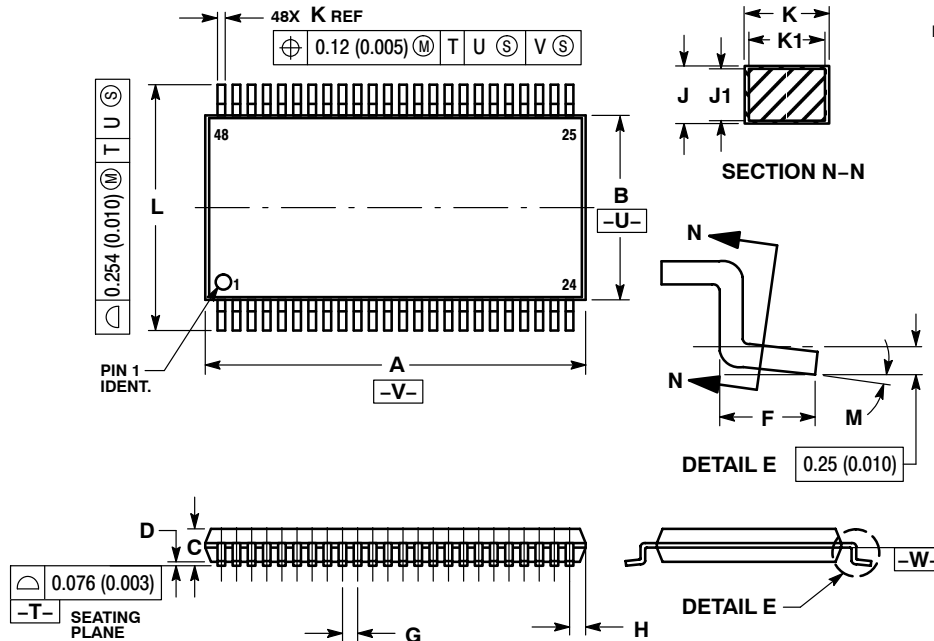
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	–––	1.10	–––	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	–––	0.015	–––
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

**RECOMMENDED
SOLDERING FOOTPRINT***

48X
0.32

48X
1.00

8.45

1

0.50
PITCH
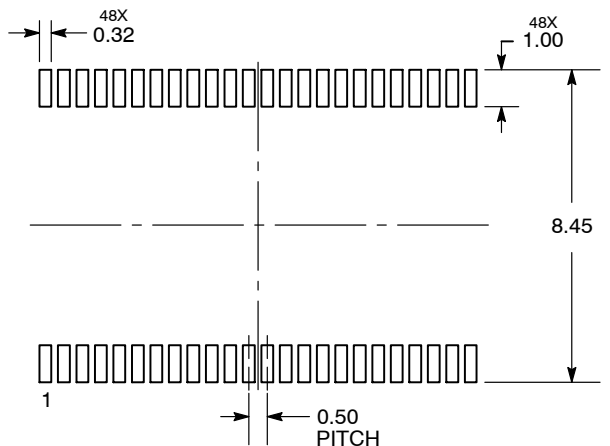
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***

XXXXXXXXXXXXG
AWLYYWW

1

XXXXX = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
G   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSSOP−48		PAGE 1 OF 1

ADDITIONAL INFORMATION

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