

# Octal D-Type Latch with 3-State Outputs

With 5 V-Tolerant Inputs

## MC74LVX573

The MC74LVX573 is an advanced high speed CMOS octal latch with 3-state outputs. The inputs tolerate voltages up to 5.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

### Features

- High Speed:  $t_{PD} = 6.4$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25$  °C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- These Devices are Pb-Free and are RoHS Compliant

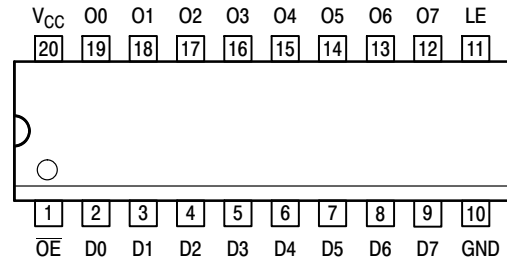


SOIC-20  
DW SUFFIX  
CASE 751D



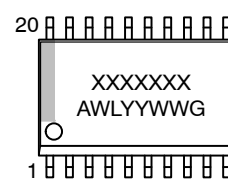
TSSOP-20  
DT SUFFIX  
CASE 948E

### PIN ASSIGNMENT

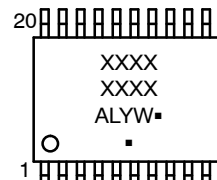


20-Lead (Top View)

### MARKING DIAGRAMS



SOIC-20



TSSOP-20

XXXXXXX = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or  $\blacksquare$  = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74LVX573

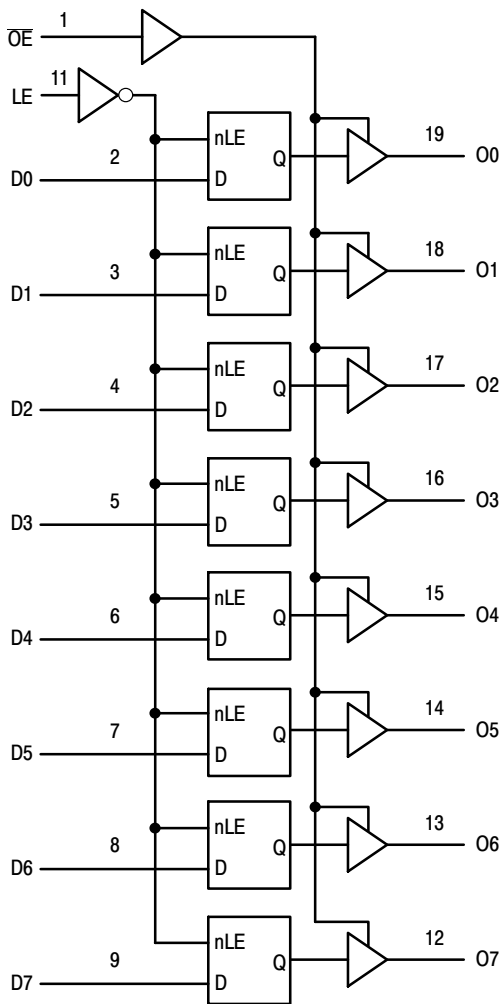


Figure 1. Logic Diagram

PIN NAMES

Pins	Function
OE	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3-State Latch Outputs

TRUTH TABLE

INPUTS			OUTPUTS	OPERATING MODE
OE	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; NC = No Change, State Prior to the Latch Enable High-to-Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs.

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## MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V <sub>CC</sub>	DC Supply Voltage		−0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage		−0.5 to +6.5	V
V <sub>OUT</sub>	DC Output Voltage		−0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin		±20	mA
I <sub>OUT</sub>	DC Output Current, Per Pin		±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins		±75	mA
I <sub>IK</sub>	Input Clamp Current		−20	mA
I <sub>OK</sub>	Output Clamp Current		±20	mA
T <sub>STG</sub>	Storage Temperature Range		−65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 s		260	°C
T <sub>J</sub>	Junction Temperature Under Bias		+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2)	SOIC-20W	96	°C/W
		TSSOP-20	150	
P <sub>D</sub>	Power Dissipation in Still Air at 25 °C	SOIC-20W	1302	mW
		TSSOP-20	833	
MSL	Moisture Sensitivity	SOIC-20W	Level 3	–
		All Other Packages	Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.573 in	–
V <sub>ESD</sub>	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	
I <sub>LATCHUP</sub>	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>IN</sub>	DC Input Voltage (Note 5)	0	5.5	V
V <sub>OUT</sub>	DC Output Voltage (Note 5)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	−40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -40 to 85 °C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4	– – –	– – –	1.5 2.0 2.4	– – –	V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6	– – –	– – –	0.5 0.8 0.8	– – –	0.5 0.8 0.8	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = -50 µA I <sub>OH</sub> = -50 µA I <sub>OH</sub> = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 –	– – –	1.9 2.9 2.48	– – –	V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50 µA I <sub>OL</sub> = 50 µA I <sub>OL</sub> = 4 mA	2.0 3.0 3.0	– – –	0.0 0.0 –	0.1 0.1 0.36	– – –	0.1 0.1 0.44	V
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	3.6	–	–	±0.1	–	±1.0	µA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	3.6 –	– –	– –	±0.2 5	– –	±2.5 –	µA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6	–	–	4.0	–	40.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -40 to 85 °C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay LE to O	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF	– –	8.2 10.7	15.6 19.1	1.0 1.0	18.5 22.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3 V    C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF	– –	6.4 8.9	10.1 13.6	1.0 1.0	12.0 15.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay D to O	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF	– –	7.6 10.1	14.5 18.0	1.0 1.0	17.5 21.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3 V    C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF	– –	5.9 8.4	9.3 12.8	1.0 1.0	11.0 14.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time OE to O	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 kΩ        C <sub>L</sub> = 50 pF	– –	7.8 10.3	15.0 18.5	1.0 1.0	18.5 22.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3 V    C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 kΩ        C <sub>L</sub> = 50 pF	– –	6.1 8.6	9.7 13.2	1.0 1.0	12.0 15.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time OE to O	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ	–	12.1	19.1	1.0	22.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3 V    C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ	–	10.1	13.6	1.0	15.5	
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output-to-Output Skew (Note 6)	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 50 pF V <sub>CC</sub> = 3.3 ± 0.3 V    C <sub>L</sub> = 50 pF	– –	– –	1.5 1.5	– –	1.5 1.5	ns

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

# MC74LVX573

## TIMING REQUIREMENTS

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25 °C		T <sub>A</sub> = -40 to 85 °C	Unit
			Typ	Limit	Limit	
t <sub>w(h)</sub>	Minimum Pulse Width, LE	V <sub>CC</sub> = 2.7 V V <sub>CC</sub> = 3.3 ± 0.3 V		6.5 5.0	7.5 5.0	ns
t <sub>su</sub>	Minimum Setup Time, D to LE	V <sub>CC</sub> = 2.7 V V <sub>CC</sub> = 3.3 ± 0.3 V		5.0 3.5	5.0 3.5	ns
t <sub>h</sub>	Minimum Hold Time, D to LE	V <sub>CC</sub> = 2.7 V V <sub>CC</sub> = 3.3 ± 0.3 V		1.5 1.5	1.5 1.5	ns

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -40 to 85 °C		Unit
		Min	Typ	Max	Min	Max	
C <sub>in</sub>	Input Capacitance	–	4	10	–	10	pF
C <sub>out</sub>	Maximum 3-State Output Capacitance	–	6	–	–	–	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 7)	–	29	–	–	–	pF

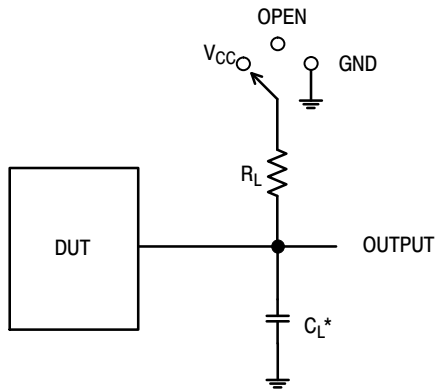
7. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per latch). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns, C<sub>L</sub> = 50 pF, V<sub>CC</sub> = 3.3 V)

Symbol	Characteristic	T <sub>A</sub> = 25 °C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.5	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	–0.5	–0.8	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	–	2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	–	0.8	V

# MC74LVX573

## TEST CIRCUITS



\*CL includes probe and jig capacitance  
Input  $t_R = t_F = 3 \text{ ns}$

Test	Switch Position	$C_L$	$R_L$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table	1 k $\Omega$
$t_{PLZ} / t_{PZL}$	$V_{CC}$		
$t_{PHZ} / t_{PZH}$	GND		

Figure 2. AC Test Circuit

## SWITCHING WAVEFORMS

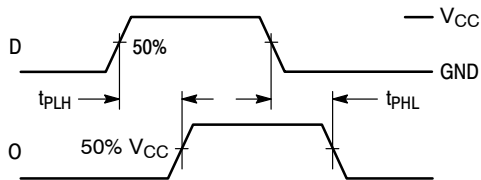


Figure 3.

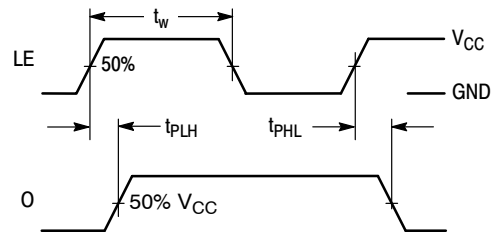


Figure 4.

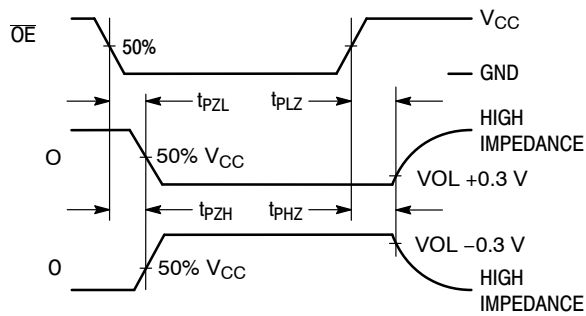


Figure 5.

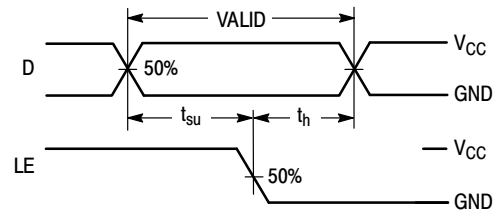


Figure 6.

## ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74LVX573DWR2G	LVX573G	SOIC-20 WB	1000 / Tape & Reel
MC74LVX573DTG	LVX 573	TSSOP-20	75 Units / Rail
MC74LVX573DTR2G	LVX 573	TSSOP-20	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*

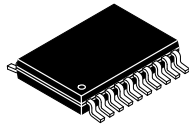


XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

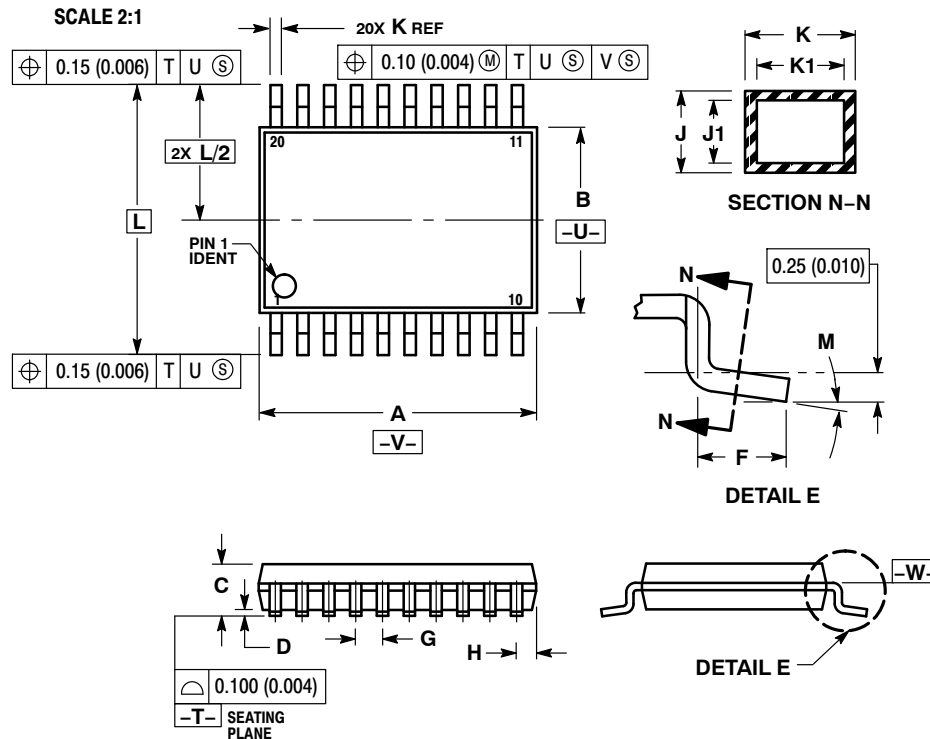
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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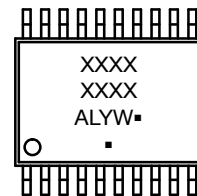

**TSSOP-20 WB**  
**CASE 948E**  
**ISSUE D**

DATE 17 FEB 2016


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***


- A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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