Quad Bus Buffer with 3-State Control Inputs

MC74VHC125, MC74VHCT125A

The MC74VHC125 and MC74VHCT125A are high speed CMOS bus buffers fabricated with silicon gate CMOS technology. These achieve high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

These devices require the 3−state control input ($\overline{OE}$) to be set High to place the output into the high impedance state.

The MC74VHC125 inputs are compatible with standard CMOS levels while the MC74VHCT125A inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

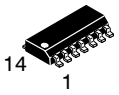
The MC74VHC125 and MC74VHCT125A internal circuits are composed of three stages, including a buffer output which provides high noise immunity and stable output. The input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT125A output structures provide protection when V_{CC} = 0 V. These output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

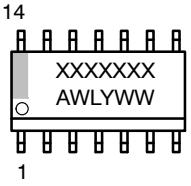
Features

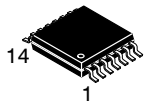
- High Speed: t_{PD} = 3.8 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAMS

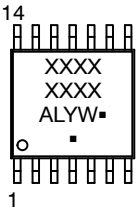


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



XXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Output
A	$\overline{OE}$	Y
H	L	H
L	L	L
X	H	Z

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

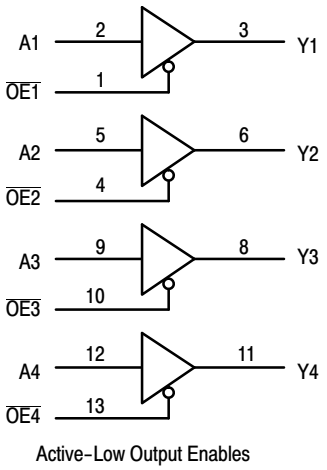


Figure 1. Logic Diagram

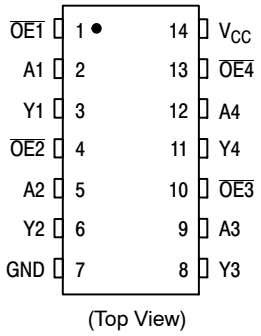


Figure 2. Pinout: 14−Lead Packages

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
Vin	DC Input Voltage		−0.5 to +6.5	V
Vout	DC Output Voltage (**MC74VHC**)		−0.5 to V_{CC}+0.5	V
	DC Output Voltage (**MC74VHCT**)	Active Mode (High or Low State) Tristate Mode (Note 1) Power−Off Mode (V_{CC} = 0 V)	−0.5 to V_{CC}+0.5 −0.5 to +6.5 −0.5 to +6.5	
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current	MC74VHC MC74VHCT	±20 −20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC−14 QFN14 TSSOP−14	116 130 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−14 QFN14 TSSOP−14	1077 962 833	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	> 2000 N/A	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74VHC					
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 5)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)		0	V_{CC}	V
T_A	Operating Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V
MC74VHCT					
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 5)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State) Tristate Mode Power−Off Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	V
T_A	Operating Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74VHC125)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	High−Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{OZ}	3−State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I_{IN}	Input Leakage Current	V_{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			4.0		40		40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHC125)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A ≤ 85°C		T_A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3V C_L = 15 pF		5.6	8.0	1.0	9.5	1.0	12.0	ns
		C_L = 50 pF		8.1	11.5	1.0	13.0	1.0	16.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15 pF		3.8	5.5	1.0	6.5	1.0	8.5	
		C_L = 50 pF		5.3	7.5	1.0	8.5	1.0	10.5	
t_{PZL}, t_{PZH}	Output Enable TIme, $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3V C_L = 15 pF, R_L = 1 kΩ		5.4	8.0	1.0	9.5	1.0	11.5	ns
		C_L = 50 pF		7.9	11.5	1.0	13.0	1.0	15.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15 pF, R_L = 1 kΩ		3.6	5.1	1.0	6.0	1.0	7.5	
		C_L = 50 pF		5.1	7.1	1.0	8.0	1.0	9.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3V C_L = 50 pF, R_L = 1 kΩ		9.5	13.2	1.0	15.0	1.0	18.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50 pF, R_L = 1 kΩ		6.1	8.8	1.0	10.0	1.0	12.0	
t_{OSLH}, t_{OSHL}	Output−to−Output Skew	V_{CC} = 3.3 ± 0.3V C_L = 50 pF (Note 6)			1.5		1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50 pF (Note 6)			1.0		1.0		1.0	
C_{in}	Input Capacitance			4.0	10		10		10	pF
C_{out}	Three−State Output Capacitance (Output in High Impedance State)			6.0						pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 7)	14	pF

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per gate). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (MC74VHC125) (C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

DC ELECTRICAL CHARACTERISTICS (MC74VHCT125A)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le 85°C$		$T_A \le 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	High−Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Low−Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4.0 mA I_{OH} = −8.0 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	3.0 4.5		0 0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4.0 mA I_{OL} = 8.0 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±0.1		±0.1	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I_{OZ}	Three−State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (MC74VHCT125A)

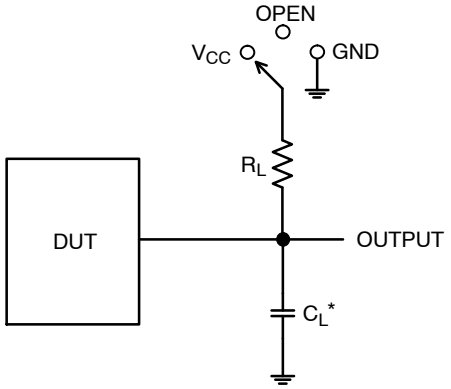
Symbol	Parameter	Test Conditions	T_A = 25°C			T_A ≤ 85°C		T_A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		5.6	8.0	1.0	9.5		12.0	ns
		C_L = 50 pF		8.1	11.5	1.0	13.0		16.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		3.8	5.5	1.0	6.5		8.5	
		C_L = 50 pF		5.3	7.5	1.0	8.5		10.5	
t_{PZL}, t_{PZH}	Output Enable TIme, $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		5.4	8.0	1.0	9.5		11.5	ns
		R_L = 1.0 kΩ C_L = 50 pF		7.9	11.5	1.0	13.0		15.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		3.6	5.1	1.0	6.0		7.5	
		R_L = 1.0 kΩ C_L = 50 pF		5.1	7.1	1.0	8.0		9.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Y	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF R_L = 1.0 kΩ		9.5	13.2	1.0	15.0		18.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF R_L = 1.0 kΩ		6.1	8.8	1.0	10.0		12.0	
t_{OSLH}, t_{OSHL}	Output−to−Output Skew	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF (Note 6)			1.5		1.5		2.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF (Note 6)			1.0		1.0		1.5	
C_{in}	Input Capacitance			4	10		10		10	pF
C_{out}	Three−State Output Capacitance (Output in High Impedance State)			6						pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 2)	14	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (MC74VHCT125A)

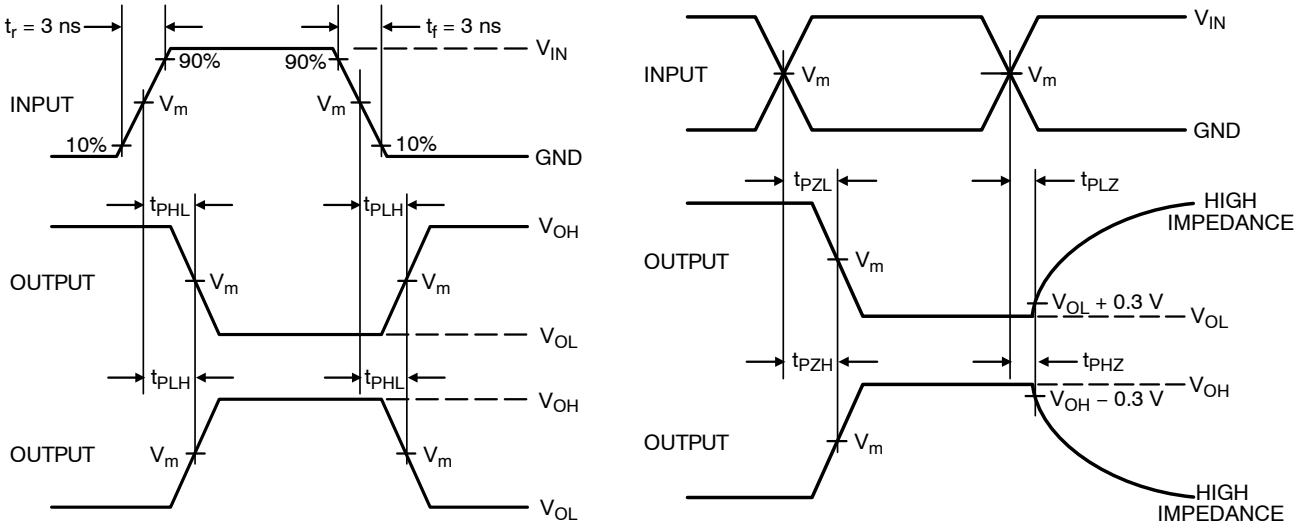
Symbol	Characteristic	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V



Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

C_L includes probe and jig capacitance

Figure 3. AC Test Circuit



Device	V_{IN}, V	V_m, V
MC74VHC125	V_{CC}	50% x V_{CC}
MC74VHCT125A	3 V	1.5 V

Figure 4. Switching Waveforms

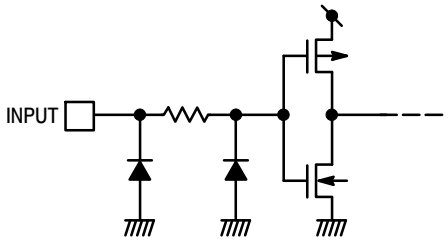


Figure 5. Input Equivalent Circuit

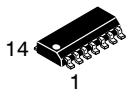
ORDERING INFORMATION

Device	Package	Marking	Shipping†
MC74VHC125DG	SOIC−14	VHC125G	55 Units / Tube
MC74VHC125DR2G	SOIC−14	VHC125G	2500 Units / Tape & Reel
MC74VHC125DTR2G	TSSOP−14	VHC 125	2500 Units / Tape & Reel
MC74VHC125DTR2G−Q*	TSSOP−14	VHC 125	2500 Units / Tape & Reel
MC74VHCT125ADR2G	SOIC−14	VHCT125AG	2500 Units / Tape & Reel
MC74VHCT125ADTR2G	TSSOP−14	VHCT 125A	2500 Units / Tape & Reel
MC74VHCT125ADTR2G−Q*	TSSOP−14	VHCT 125A	2500 Units / Tape & Reel

†For complete information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

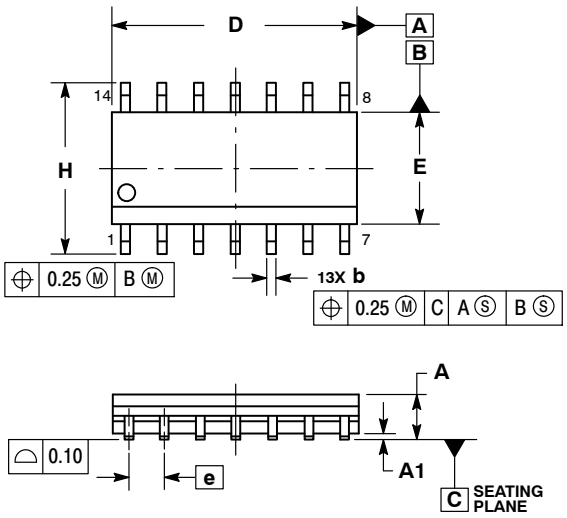
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

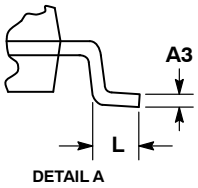


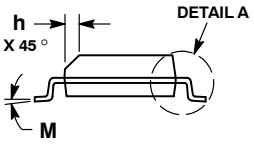
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



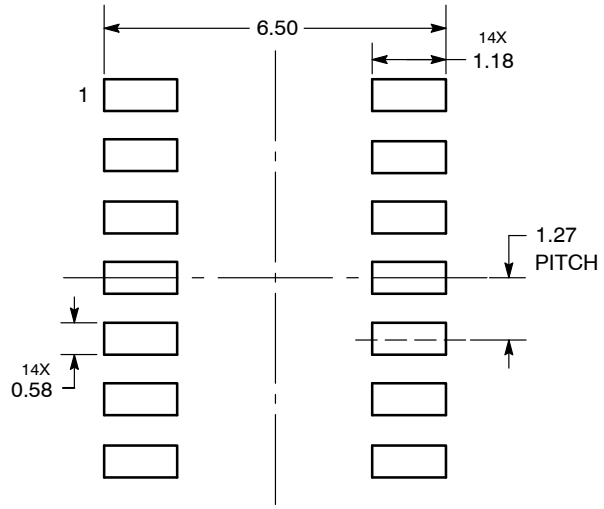




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

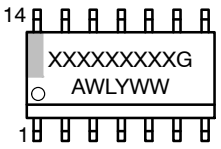
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

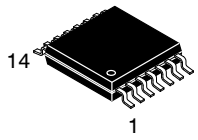
STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

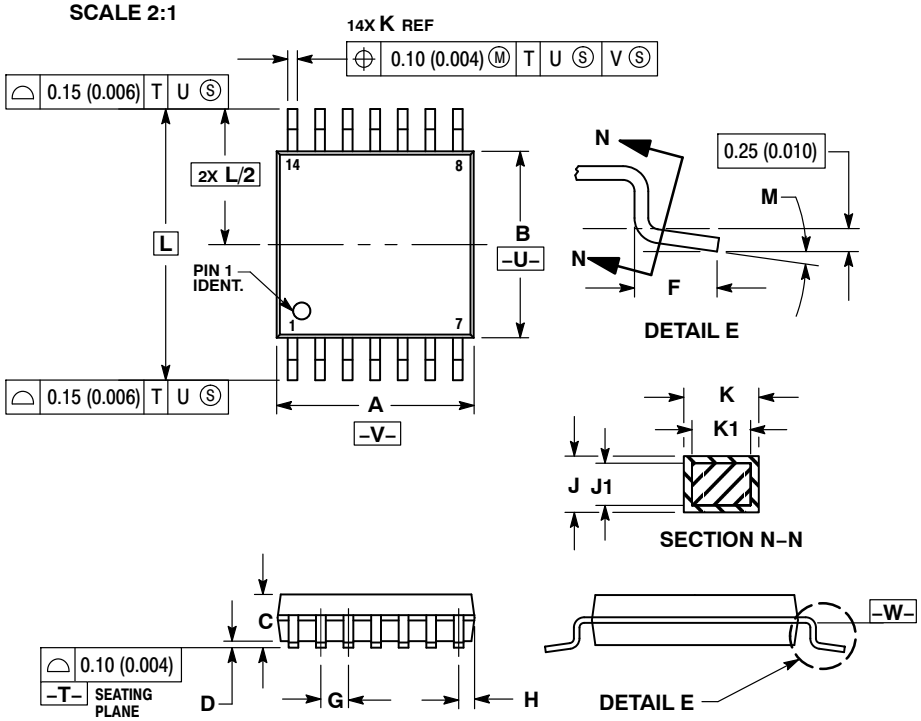
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



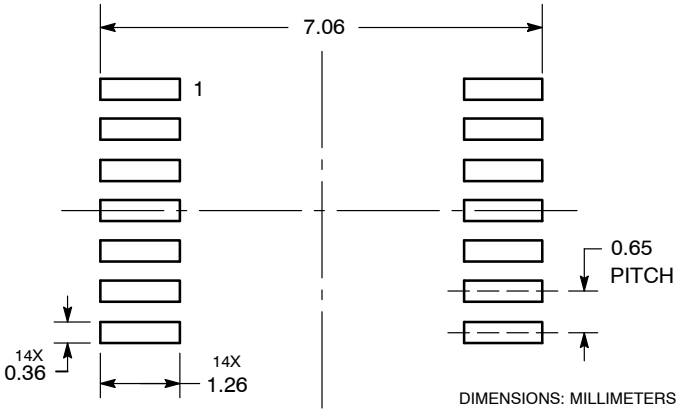
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

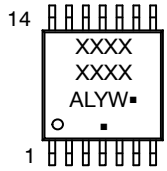
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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