# Analog Multiplexers / Demultiplexers

## High−Performance Silicon−Gate CMOS

# MC74VHC4051, MC74VHC4052, MC74VHC4053

The MC74VHC4051, MC74VHC4052 and MC74VHC4053 utilize silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from $V_{CC}$ to $V_{EE}$).

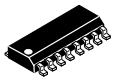
The VHC4051, VHC4052 and VHC4053 are identical in pinout to the high−speed HC4051A, HC4052A and HC4053A, and the metal−gate MC14051B, MC14052B and MC14053B. The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel−Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance ($R_{on}$) is more linear over input voltage than $R_{on}$ of metal−gate CMOS analog switches.

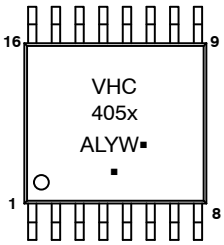
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC}$ − GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal−Gate Counterparts
- Low Noise
- Chip Complexity: VHC4051 — 184 FETs or 46 Equivalent Gates
  VHC4052 — 168 FETs or 42 Equivalent Gates
  VHC4053 — 156 FETs or 39 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MARKING DIAGRAMS**



**SOIC−16**
**D SUFFIX**
**CASE 751B**

**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




| | |
|---|---|
| VHC405x | = Specific Device Code (x = 1, 2 or 3) |
| A | = Assembly Location |
| L, WL | = Wafer Lot |
| Y, YY | = Year |
| W, WW | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 16.

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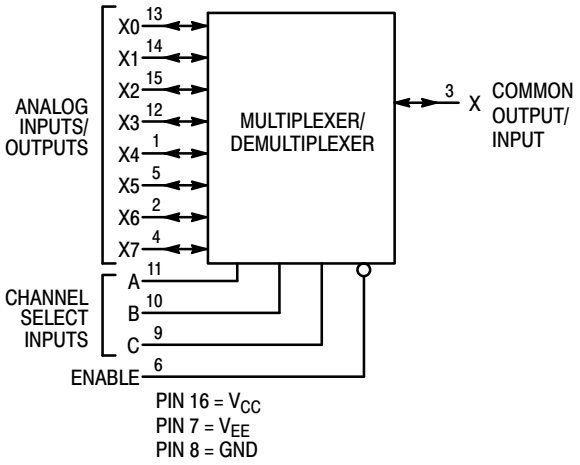
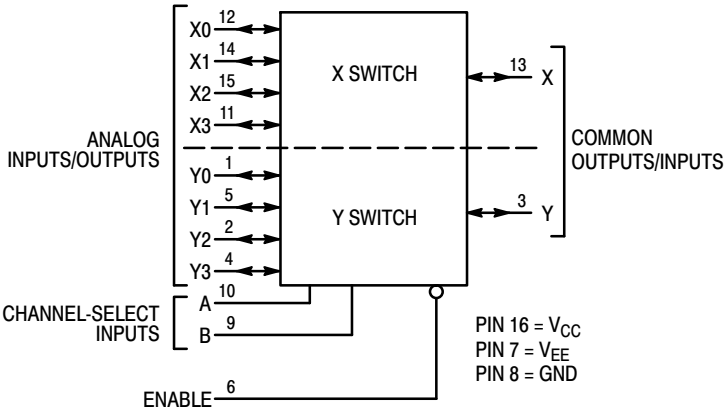
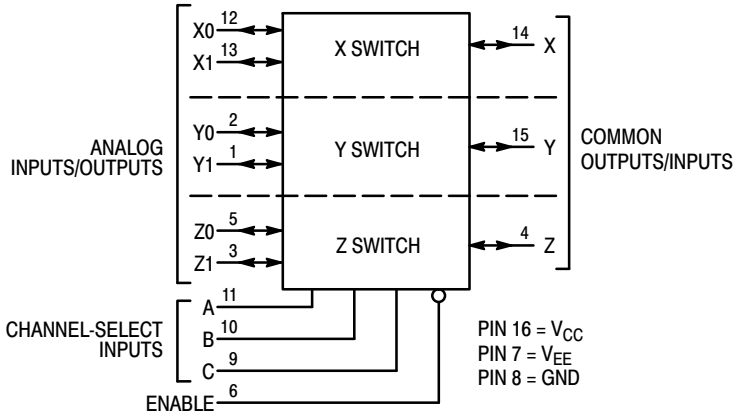



**MC74VHC4051**
**Single−Pole, 8−Position Plus Common Off**




**MC74VHC4052**
**Double−Pole, 4−Position Plus Common Off**




NOTE: This device allows independent control of each switch. Channel−Select Input A controls the X−Switch, Input B controls the Y−Switch and Input C controls the Z−Switch

**MC74VHC4053**
**Triple Single−Pole, Double−Position Plus Common Off**

**Figure 1. Logic Diagrams**



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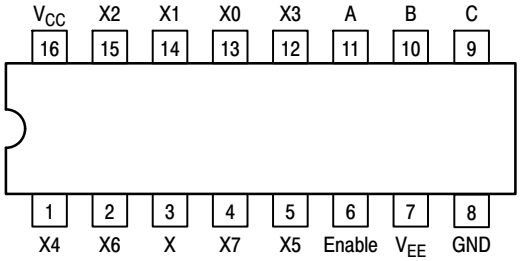


**Figure 2. Pinout: MC74VHC4051** (Top View)

**FUNCTION TABLE – MC74VHC4051**

| Control Inputs | | | | |
|---|---|---|---|---|
| | Select | | | |
| Enable | C | B | A | ON Channels |
| L | L | L | L | X0 |
| L | L | L | H | X1 |
| L | L | H | L | X2 |
| L | L | H | H | X3 |
| L | H | L | L | X4 |
| L | H | L | H | X5 |
| L | H | H | L | X6 |
| L | H | H | H | X7 |
| H | X | X | X | NONE |

X = Don't Care

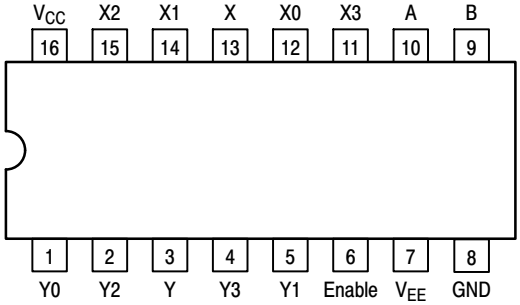


**Figure 3. Pinout: MC74VHC4052** (Top View)

**FUNCTION TABLE – MC74VHC4052**

| Control Inputs | | | |
|---|---|---|---|
| | Select | | |
| Enable | B | A | ON Channels |
| L | L | L | Y0 X0 |
| L | L | H | Y1 X1 |
| L | H | L | Y2 X2 |
| L | H | H | Y3 X3 |
| H | X | X | NONE |

X = Don't Care

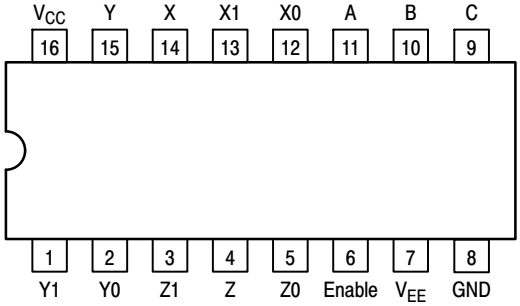


**Figure 4. Pinout: MC74VHC4053** (Top View)

**FUNCTION TABLE – MC74VHC4053**

| Control Inputs | | | | |
|---|---|---|---|---|
| | Select | | | |
| Enable | C | B | A | ON Channels |
| L | L | L | L | Z0 Y0 X0 |
| L | L | L | H | Z0 Y0 X1 |
| L | L | H | L | Z0 Y1 X0 |
| L | L | H | H | Z0 Y1 X1 |
| L | H | L | L | Z1 Y0 X0 |
| L | H | L | H | Z1 Y0 X1 |
| L | H | H | L | Z1 Y1 X0 |
| L | H | H | H | Z1 Y1 X1 |
| H | X | X | X | NONE |

X = Don't Care



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## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage (Referenced to GND)<br>(Referenced to $V_{EE}$) | – 0.5 to + 7.0<br>– 0.5 to + 14.0 | V |
| $V_{EE}$ | Negative DC Supply Voltage (Referenced to GND) | – 7.0 to + 5.0 | V |
| $V_{IS}$ | Analog Input Voltage | $V_{EE}$ – 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{in}$ | Digital Input Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| I | DC Current, Into or Out of Any Pin | ± 25 | mA |
| $P_D$ | Power Dissipation in Still Air SOIC Package†<br>TSSOP Package† | 500<br>450 | mW |
| $T_{stg}$ | Storage Temperature Range | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage (Referenced to GND)<br>(Referenced to $V_{EE}$) | 2.0<br>2.0 | 6.0<br>12.0 | V |
| $V_{EE}$ | Negative DC Supply Voltage, Output (Referenced to GND) | – 6.0 | GND | V |
| $V_{IS}$ | Analog Input Voltage | $V_{EE}$ | $V_{CC}$ | V |
| $V_{in}$ | Digital Input Voltage (Referenced to GND) | GND | $V_{CC}$ | V |
| $V_{IO}$* | Static or Dynamic Voltage Across Switch | | 1.2 | V |
| $T_A$ | Operating Temperature Range, All Package Types | – 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise/Fall Time (Channel Select or Enable Inputs) $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 3.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0<br>0 | 1000<br>800<br>500<br>400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*For voltage drops across switch greater than 1.2V (switch on), excessive $V_{CC}$ current may be drawn; i.e., the current out of the switch may contain both $V_{CC}$ and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.



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**DC CHARACTERISTICS — Digital Section** (Voltages Referenced to GND) $V_{EE}$ = GND, Except Where Noted

| Symbol | Parameter | Condition | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | –55 to 25°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage, Channel–Select or Enable Inputs | $R_{on}$ = Per Spec | 2.0<br>3.0<br>4.5<br>6.0 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs | $R_{on}$ = Per Spec | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V |
| $I_{in}$ | Maximum Input Leakage Current, Channel–Select or Enable Inputs | $V_{in}$ = $V_{CC}$ or GND,<br>$V_{EE}$ = – 6.0 V | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | Channel Select, Enable and<br>$V_{IS}$ = $V_{CC}$ or GND; $V_{EE}$ = GND<br>$V_{IO}$ = 0 V $V_{EE}$ = – 6.0 | <br>6.0<br>6.0 | <br>1<br>4 | <br>10<br>40 | <br>40<br>80 | μA |

**DC ELECTRICAL CHARACTERISTICS** Analog Section

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $V_{EE}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $R_{on}$ | Maximum “ON” Resistance | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{IS}$ = $V_{CC}$ to $V_{EE}$<br>$I_S$ ≤ 2.0 mA<br>(Figures 5 through 11) | 3.0<br>4.5<br>4.5<br>6.0 | 0.0<br>0.0<br>– 4.5<br>– 6.0 | 200<br>160<br>120<br>100 | 240<br>200<br>150<br>125 | 320<br>280<br>170<br>140 | Ω |
| | | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{IS}$ = $V_{CC}$ or $V_{EE}$ (Endpoints)<br>$I_S$ ≤ 2.0 mA<br>(Figures 5 through11) | 3.0<br>4.5<br>4.5<br>6.0 | 0.0<br>0.0<br>– 4.5<br>– 6.0 | 150<br>110<br>90<br>80 | 180<br>140<br>120<br>100 | 230<br>190<br>140<br>115 | |
| $\Delta R_{on}$ | Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package | $V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{IS}$ = 1/2 ($V_{CC}$ – $V_{EE}$)<br>$I_S$ ≤ 2.0 mA | 3.0<br>4.5<br>4.5<br>6.0 | 0.0<br>0.0<br>– 4.5<br>– 6.0 | 40<br>20<br>10<br>10 | 50<br>25<br>15<br>12 | 80<br>40<br>18<br>14 | Ω |
| $I_{off}$ | Maximum Off–Channel Leakage Current, Any One Channel | $V_{in}$ = $V_{IL}$ or $V_{IH}$;<br>$V_{IO}$ = $V_{CC}$ – $V_{EE}$;<br>Switch Off (Figure 12) | 6.0 | – 6.0 | 0.1 | 0.5 | 1.0 | μA |
| | Maximum Off–Channel Leakage Current, Common Channel VHC4051<br>VHC4052<br>VHC4053 | $V_{in}$ = $V_{IL}$ or $V_{IH}$;<br>$V_{IO}$ = $V_{CC}$ – $V_{EE}$;<br>Switch Off (Figure 13) | 6.0<br>6.0<br>6.0 | – 6.0<br>– 6.0<br>– 6.0 | 0.2<br>0.1<br>0.1 | 2.0<br>1.0<br>1.0 | 4.0<br>2.0<br>2.0 | |
| $I_{on}$ | Maximum On–Channel Leakage Current, Channel–to–Channel VHC4051<br>VHC4052<br>VHC4053 | $V_{in}$ = $V_{IL}$ or $V_{IH}$;<br>Switch–to–Switch =<br>$V_{CC}$ – $V_{EE}$; (Figure 14) | 6.0<br>6.0<br>6.0 | – 6.0<br>– 6.0<br>– 6.0 | 0.2<br>0.1<br>0.1 | 2.0<br>1.0<br>1.0 | 4.0<br>2.0<br>2.0 | μA |



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**AC CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | –55 to 25°C | ≤85°C | ≤125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Channel–Select to Analog Output (Figures 18, 19) | 2.0<br>3.0<br>4.5<br>6.0 | 270<br>90<br>59<br>45 | 320<br>110<br>79<br>65 | 350<br>125<br>85<br>75 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Analog Input to Analog Output (Figures 20, 21) | 2.0<br>3.0<br>4.5<br>6.0 | 40<br>25<br>12<br>10 | 60<br>30<br>15<br>13 | 70<br>32<br>18<br>15 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Enable to Analog Output (Figures 22, 23) | 2.0<br>3.0<br>4.5<br>6.0 | 160<br>70<br>48<br>39 | 200<br>95<br>63<br>55 | 220<br>110<br>76<br>63 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Enable to Analog Output (Figures 22, 23) | 2.0<br>3.0<br>4.5<br>6.0 | 245<br>115<br>49<br>39 | 315<br>145<br>69<br>58 | 345<br>155<br>83<br>67 | ns |
| $C_{in}$ | Maximum Input Capacitance, Channel–Select or Enable Inputs | | 10 | 10 | 10 | pF |
| $C_{I/O}$ | Maximum Capacitance — Analog I/O | | 35 | 35 | 35 | pF |
| | (All Switches Off) — Common O/I: VHC4051<br>VHC4052<br>VHC4053 | | 130<br>80<br>50 | 130<br>80<br>50 | 130<br>80<br>50 | |
| | Feedthrough | | 1.0 | 1.0 | 1.0 | |

| | | | Typical @ 25°C, $V_{CC}$ = 5.0 V, $V_{EE}$ = 0 V | |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Figure 25)* | VHC4051<br>VHC4052<br>VHC4053 | 45<br>80<br>45 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.



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**ADDITIONAL APPLICATION CHARACTERISTICS** (GND = 0 V)

| Symbol | Parameter | Condition | $V_{CC}$ V | $V_{EE}$ V | Limit* 25°C '51 | Limit* 25°C '52 | Limit* 25°C '53 | Unit |
|---|---|---|---|---|---|---|---|---|
| BW | Maximum On−Channel Bandwidth or Minimum Frequency Response (Figure 15) | $f_{in}$ = 1MHz Sine Wave; Adjust $f_{in}$ Voltage to Obtain 0dBm at $V_{OS}$; Increase $f_{in}$ Frequency Until dB Meter Reads −3dB; $R_L$ = 50Ω, $C_L$ = 10pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | 80<br>80<br>80 | 95<br>95<br>95 | 120<br>120<br>120 | MHz |
| — | Off−Channel Feedthrough Isolation (Figure 16) | $f_{in}$ = Sine Wave; Adjust $f_{in}$ Voltage to Obtain 0dBm at $V_{IS}$<br>$f_{in}$ = 10kHz, $R_L$ = 600Ω, $C_L$ = 50pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | −50<br>−50<br>−50 | | | dB |
| | | $f_{in}$ = 1.0MHz, $R_L$ = 50Ω, $C_L$ = 10pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | −40<br>−40<br>−40 | | | |
| — | Feedthrough Noise. Channel−Select Input to Common I/O (Figure 17) | $V_{in}$ ≤ 1MHz Square Wave ($t_r$ = $t_f$ = 6ns); Adjust $R_L$ at Setup so that $I_S$ = 0A; Enable = GND $R_L$ = 600Ω, $C_L$ = 50pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | 25<br>105<br>135 | | | $mV_{PP}$ |
| | | $R_L$ = 10kΩ, $C_L$ = 10pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | 35<br>145<br>190 | | | |
| — | Crosstalk Between Any Two Switches (Figure 24) (Test does not apply to VHC4051) | $f_{in}$ = Sine Wave; Adjust $f_{in}$ Voltage to Obtain 0dBm at $V_{IS}$<br>$f_{in}$ = 10kHz, $R_L$ = 600Ω, $C_L$ = 50pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | −50<br>−50<br>−50 | | | dB |
| | | $f_{in}$ = 1.0MHz, $R_L$ = 50Ω, $C_L$ = 10pF | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | −60<br>−60<br>−60 | | | |
| THD | Total Harmonic Distortion (Figure 26) | $f_{in}$ = 1kHz, $R_L$ = 10kΩ, $C_L$ = 50pF<br>THD = $THD_{measured}$ − $THD_{source}$<br>$V_{IS}$ = 4.0$V_{PP}$ sine wave<br>$V_{IS}$ = 8.0$V_{PP}$ sine wave<br>$V_{IS}$ = 11.0$V_{PP}$ sine wave | 2.25<br>4.50<br>6.00 | −2.25<br>−4.50<br>−6.00 | 0.10<br>0.08<br>0.05 | | | % |

*Limits not tested. Determined by design and verified by qualification.

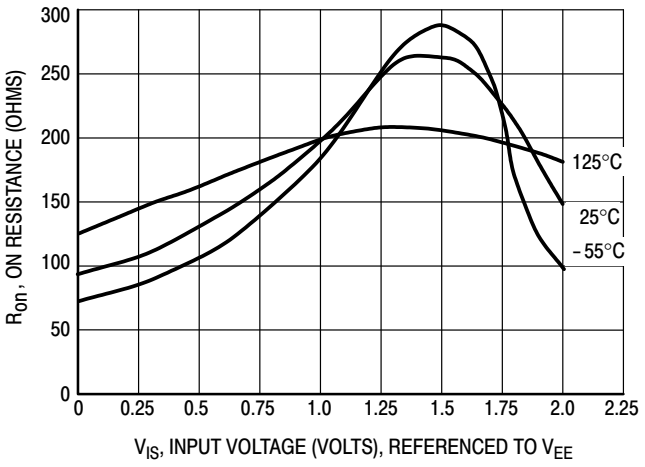


**Figure 5. Typical On Resistance, $V_{CC}$ − $V_{EE}$ = 2.0 V**

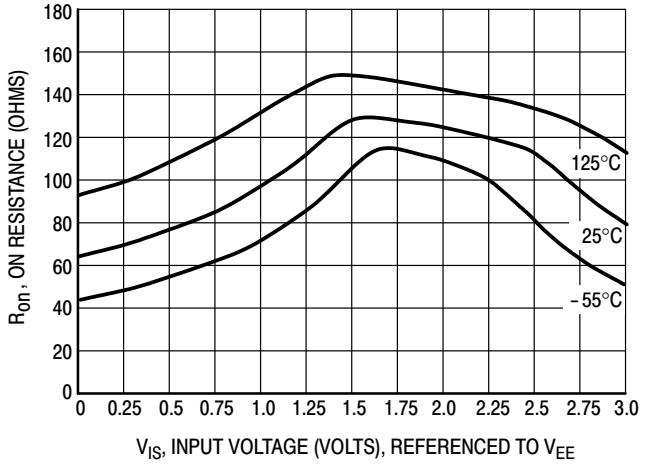


**Figure 6. Typical On Resistance, $V_{CC}$ − $V_{EE}$ = 3.0 V**



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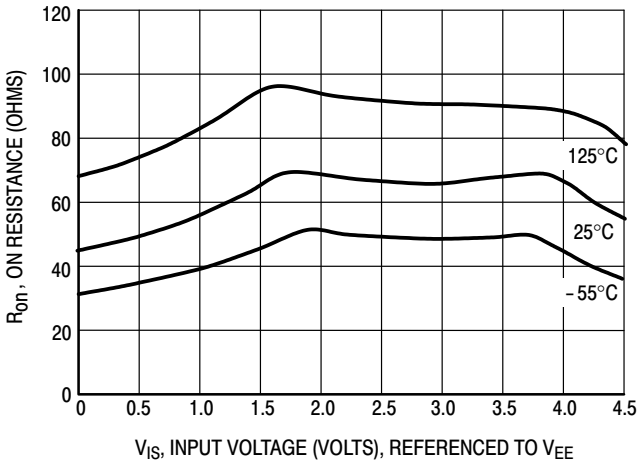


**Figure 7. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V**

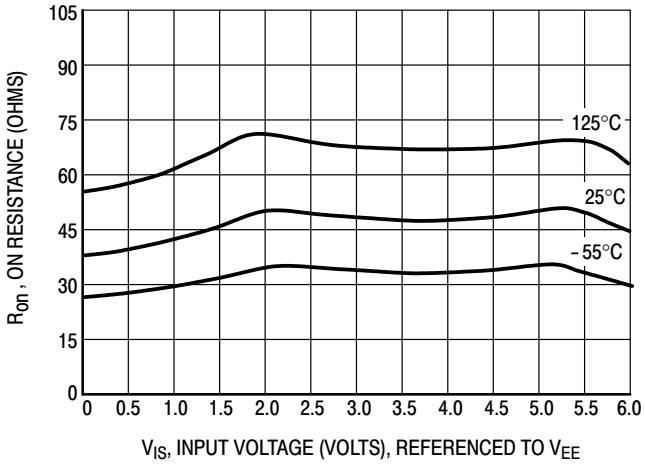


**Figure 8. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V**

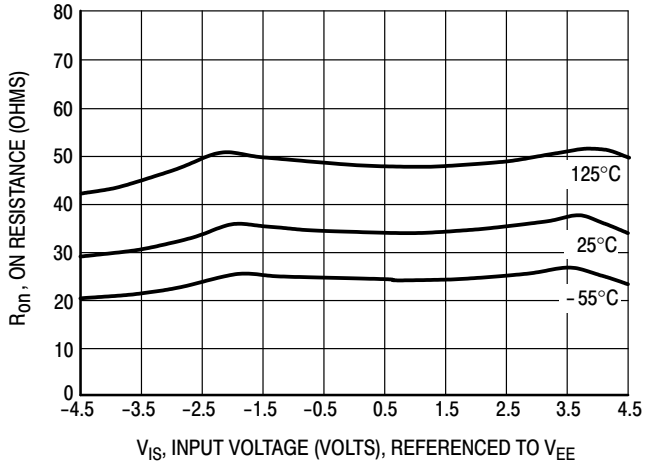


**Figure 9. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V**

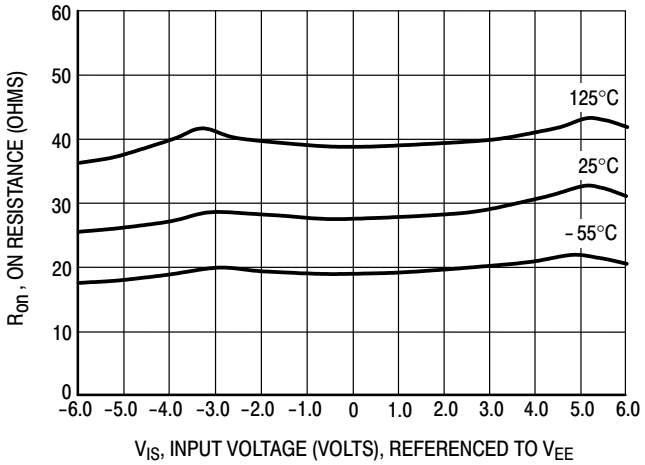


**Figure 10. Typical On Resistance, $V_{CC} - V_{EE} = 12.0$ V**

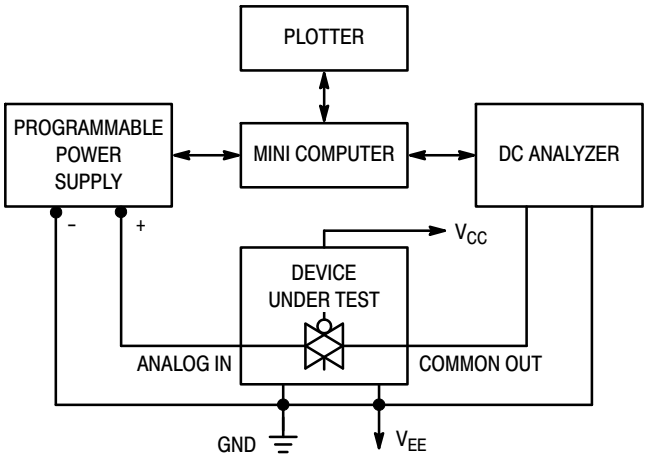


**Figure 11. On Resistance Test Set−Up**



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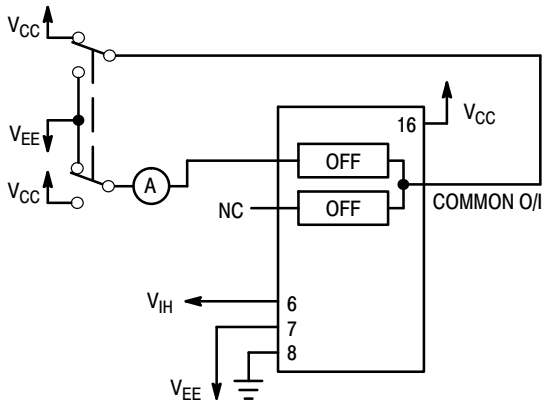


**Figure 12. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up**

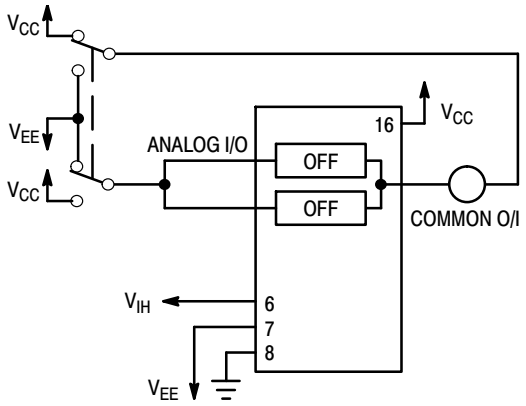


**Figure 13. Maximum Off Channel Leakage Current, Common Channel, Test Set−Up**

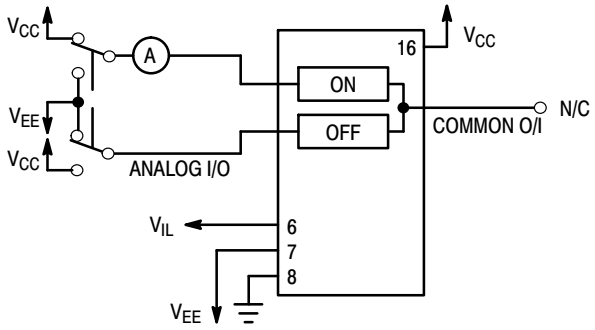


**Figure 14. Maximum On Channel Leakage Current, Channel to Channel, Test Set−Up**

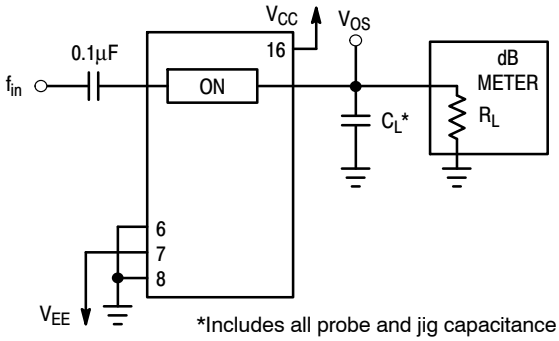


**Figure 15. Maximum On Channel Bandwidth, Test Set−Up**

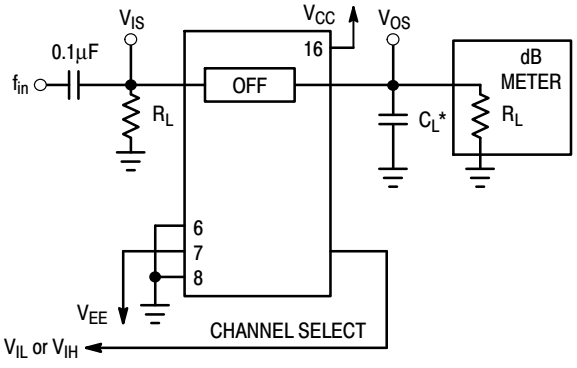


**Figure 16. Off Channel Feedthrough Isolation, Test Set−Up**

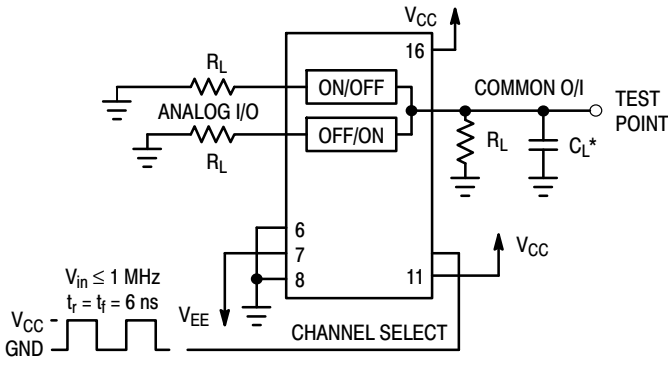


**Figure 17. Feedthrough Noise, Channel Select to Common Out, Test Set−Up**



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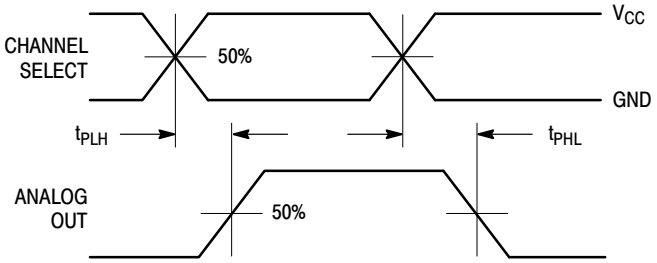
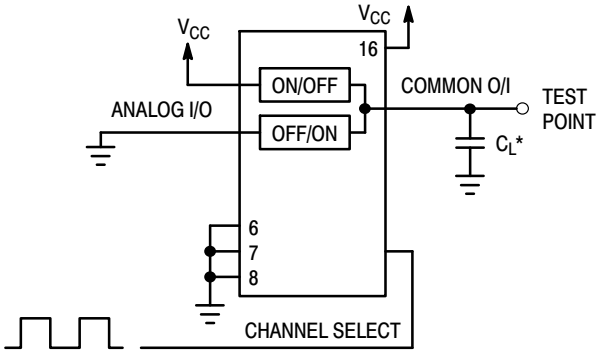



**Figure 18. Propagation Delays, Channel Select to Analog Out**




*Includes all probe and jig capacitance

**Figure 19. Propagation Delay, Test Set−Up Channel Select to Analog Out**

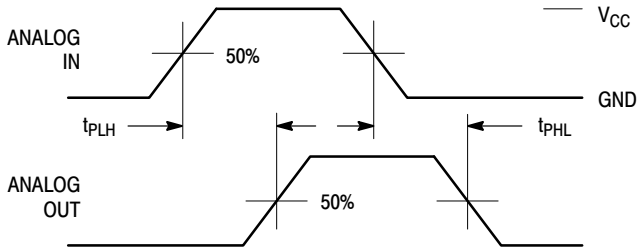
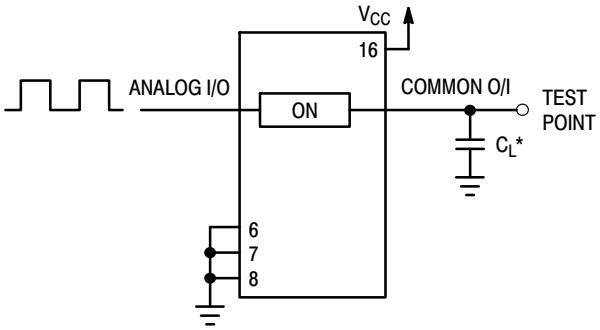



**Figure 20. Propagation Delays, Analog In to Analog Out**




*Includes all probe and jig capacitance

**Figure 21. Propagation Delay, Test Set−Up Analog In to Analog Out**

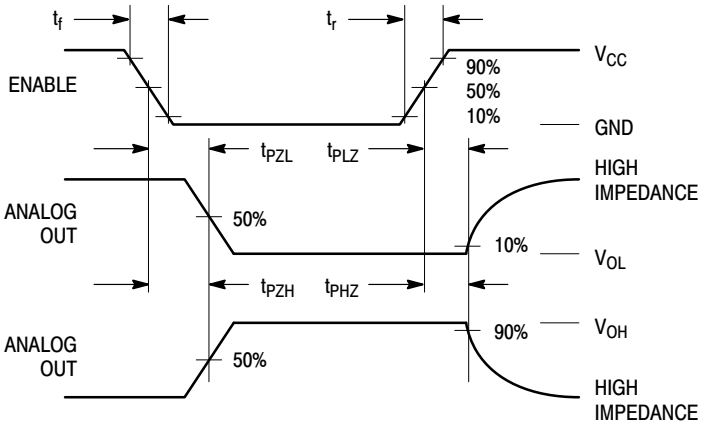



**Figure 22. Propagation Delays, Enable to Analog Out**

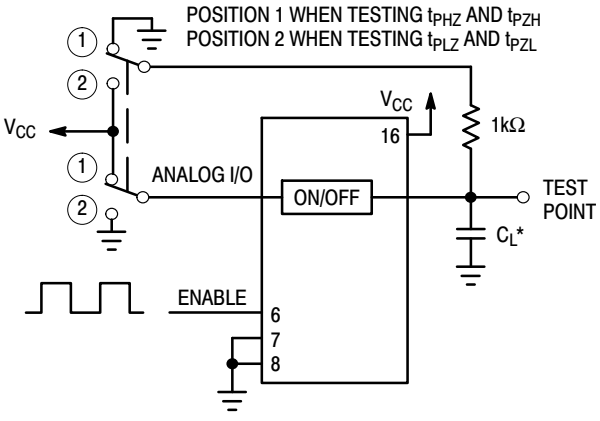



**Figure 23. Propagation Delay, Test Set−Up Enable to Analog Out**



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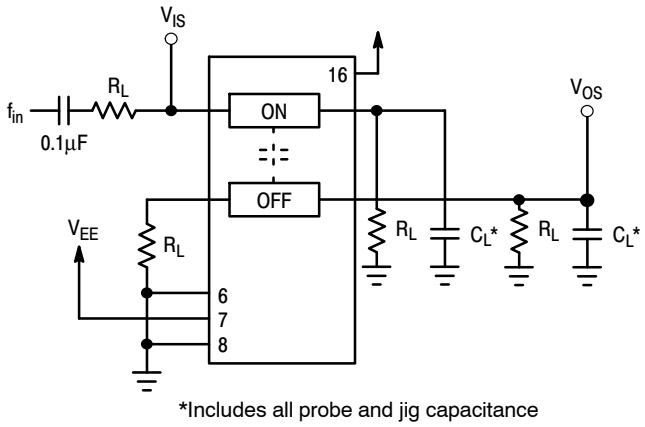


**Figure 24. Crosstalk Between Any Two Switches, Test Set−Up**

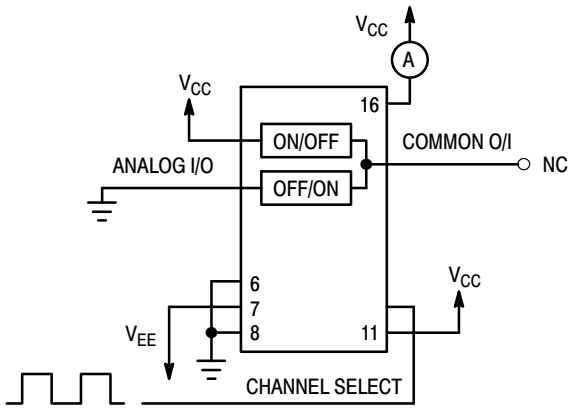


**Figure 25. Power Dissipation Capacitance, Test Set−Up**

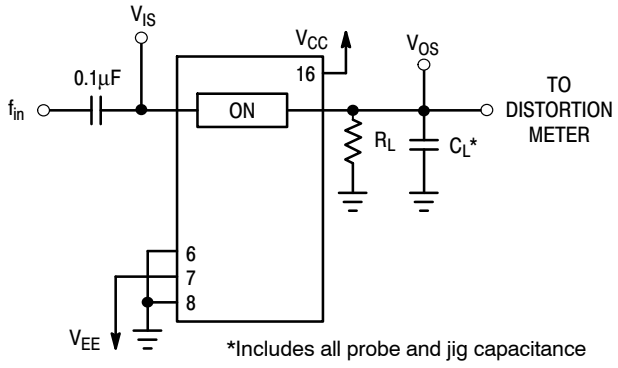


**Figure 26. Total Harmonic Distortion, Test Set−Up**

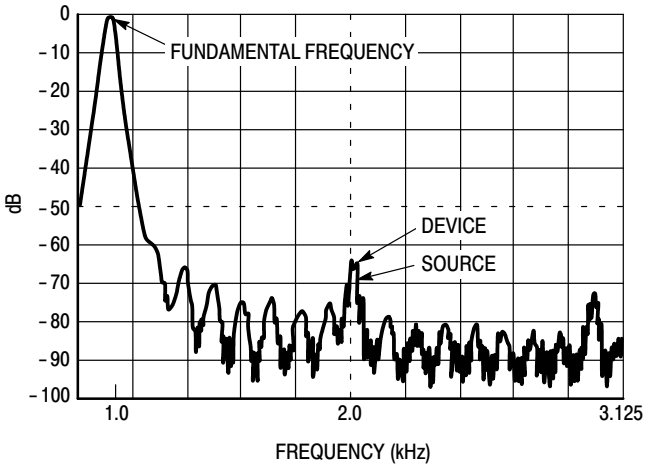


**Figure 27. Plot, Harmonic Distortion**

## APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at $V_{CC}$ or GND logic levels. $V_{CC}$ being recognized as a logic high and GND being recognized as a logic low. In this example:

$V_{CC}$ = +5V = logic high
GND = 0V = logic low

The maximum analog voltage swings are determined by the supply voltages $V_{CC}$ and $V_{EE}$. The positive peak analog voltage should not exceed $V_{CC}$. Similarly, the negative peak analog voltage should not go below $V_{EE}$. In this example, the difference between $V_{CC}$ and $V_{EE}$ is ten volts. Therefore, using the configuration of Figure 28, a maximum analog signal of ten volts peak−to−peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to $V_{CC}$ or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$V_{CC}$ − GND = 2 to 6 volts
$V_{EE}$ − GND = 0 to −6 volts
$V_{CC}$ − $V_{EE}$ = 2 to 12 volts
and $V_{EE} \leq$ GND

When voltage transients above $V_{CC}$ and/or below $V_{EE}$ are anticipated on the analog channels, external Germanium or Schottky diodes ($D_x$) are recommended as shown in Figure 29. These diodes should be able to absorb the maximum anticipated current surges during clipping.


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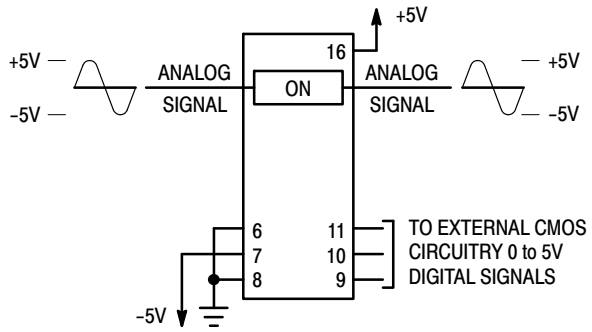



**Figure 28. Application Example**

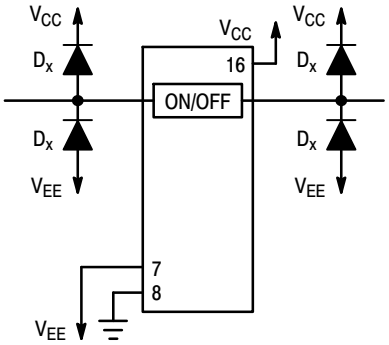
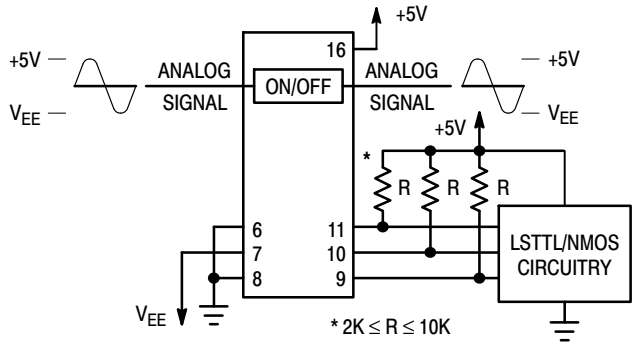
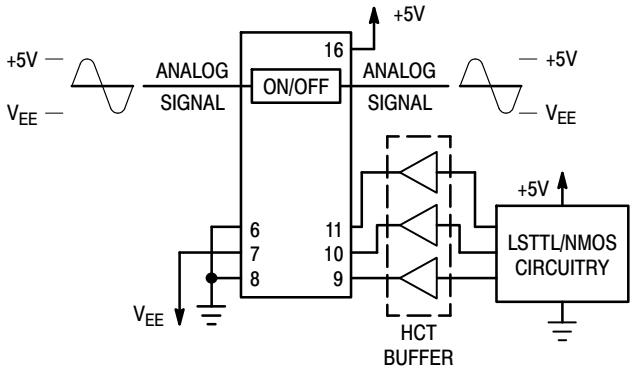



**Figure 29. External Germanium or Schottky Clipping Diodes**




**a. Using Pull–Up Resistors**




**b. Using HCT Interface**

**Figure 30. Interfacing LSTTL/NMOS to CMOS Inputs**



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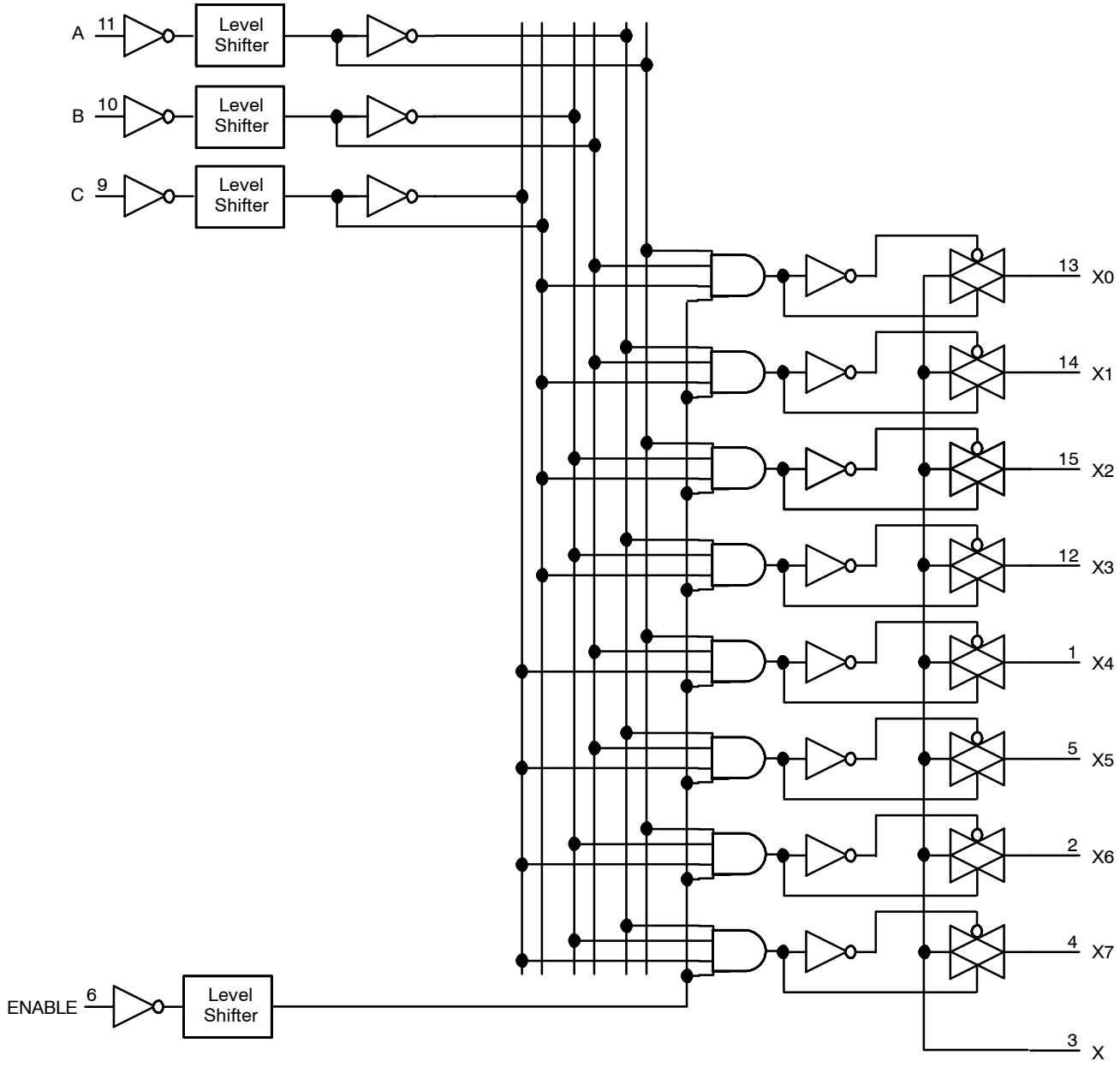


**Figure 31. Function Diagram, VHC4051**



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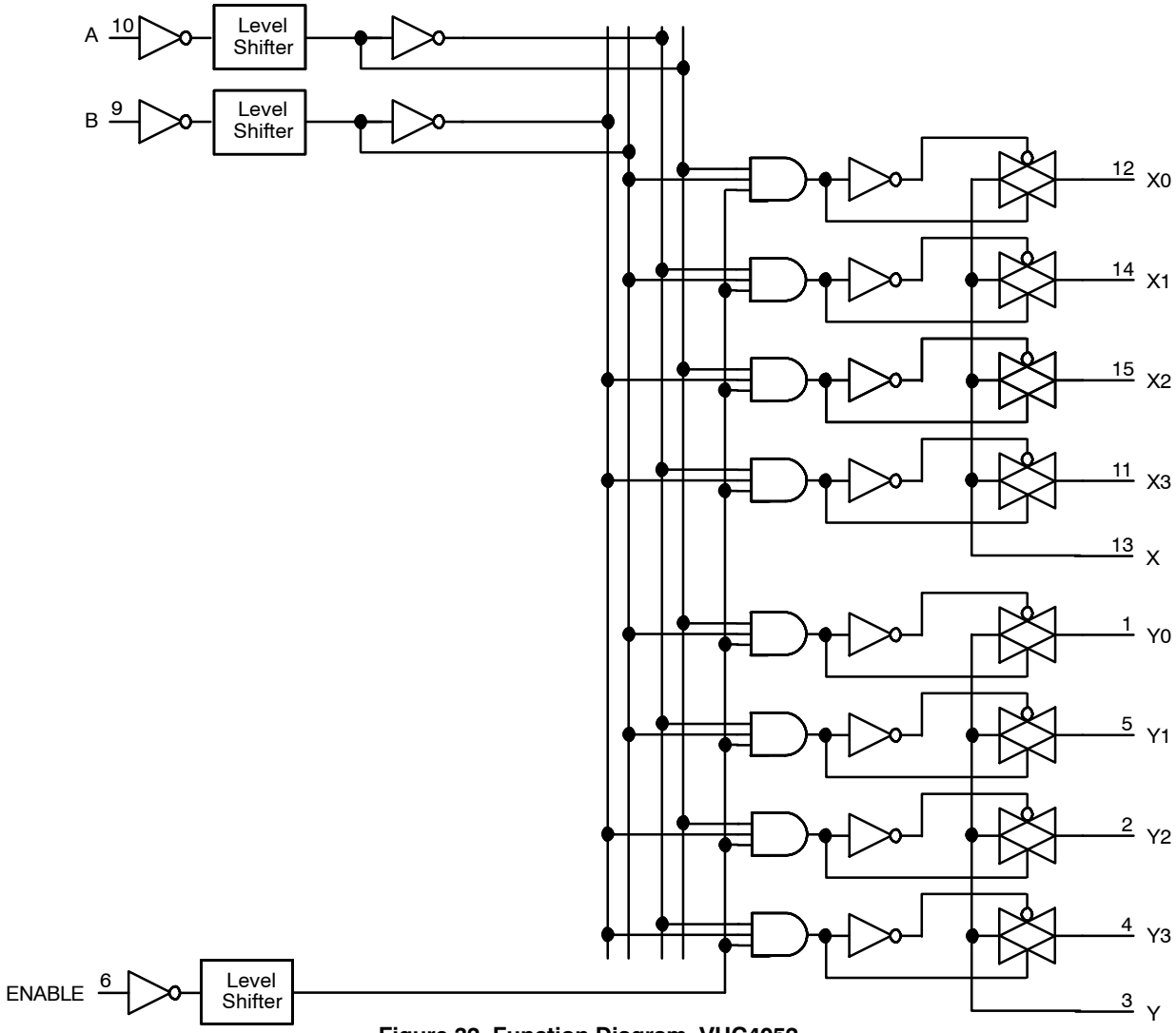


**Figure 32. Function Diagram, VHC4052**



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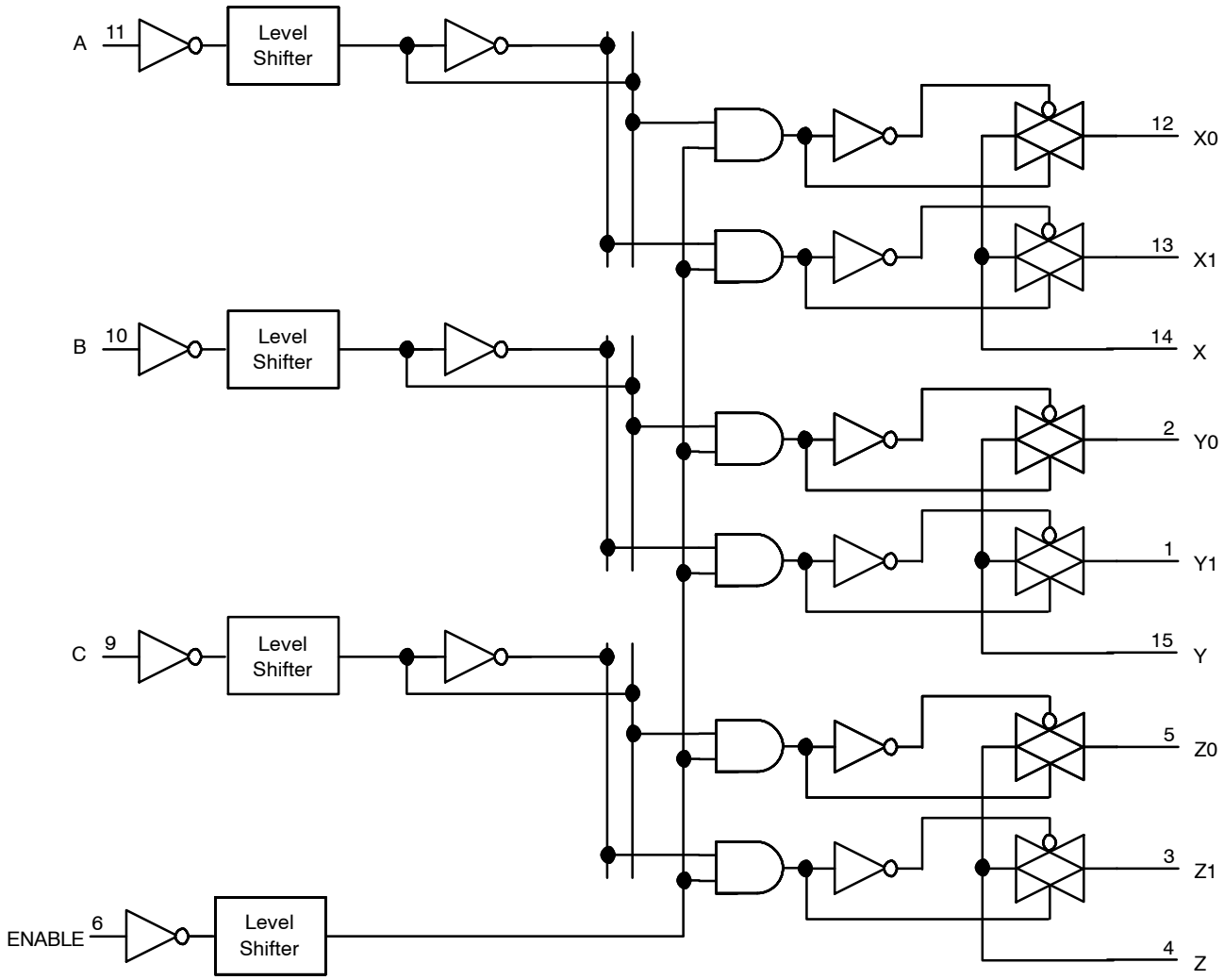


**Figure 33. Function Diagram, VHC4053**



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## ORDERING & SHIPPING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74VHC4051DR2G | SOIC−16 (Pb−Free) | 2500 / Tape & Reel |
| MC74VHC4052DR2G | | |
| MC74VHC4053DR2G | | |
| MC74VHC4051DTR2G | TSSOP−16 (Pb−Free) | 2500 / Tape & Reel |
| MC74VHC4052DTR2G | | |
| MC74VHC4053DTR2G | | |

**DISCONTINUED** (Note 1)

| | | |
|---|---|---|
| NLVVHC4051DTR2G* | TSSOP−16 (Pb−Free) | 2500 / Tape & Reel |
| NLVVHC4052DTR2G* | | |
| NLVVHC4053DTR2G* | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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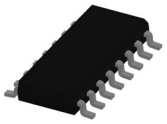
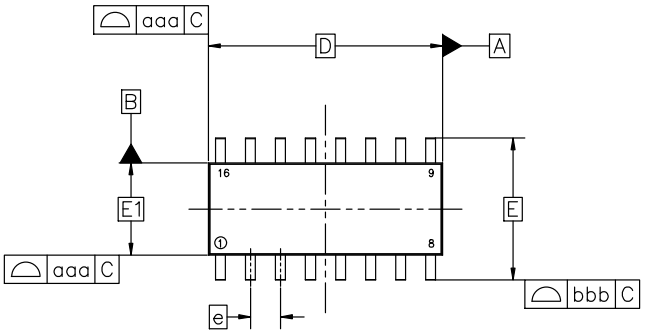


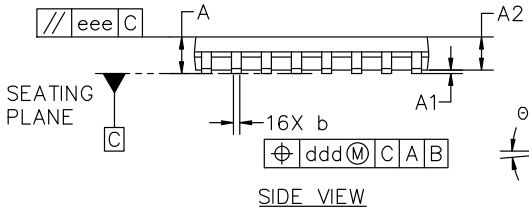
**SOIC−16 9.90x3.90x1.37 1.27P**
CASE 751B
ISSUE M

DATE 18 OCT 2024

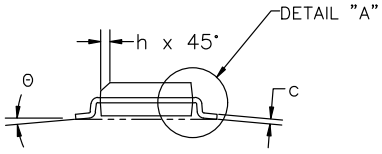
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



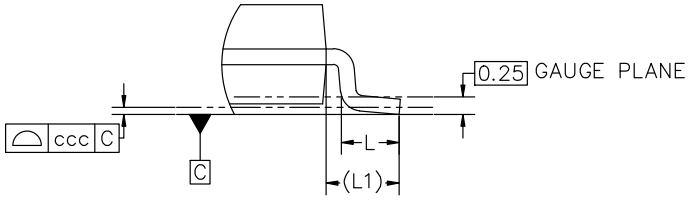

TOP VIEW




SIDE VIEW

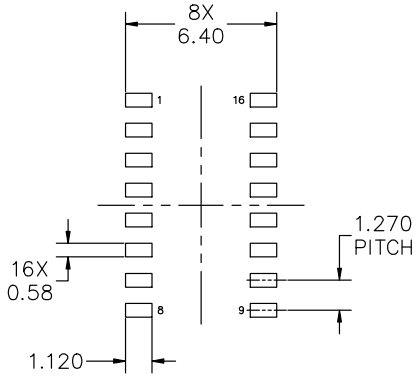



END VIEW




DETAIL "A"
Scale 3:1

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.10 | 0.18 | 0.25 |
| A2 | 1.25 | 1.37 | 1.50 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | −−− | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| Θ | 0° | −−− | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |




RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

| | | | |
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| **DESCRIPTION:** | **SOIC−16 9.90X3.90X1.37 1.27P** | | **PAGE 1 OF 2** |

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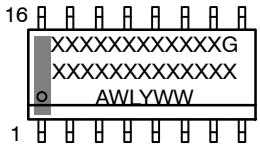
**SOIC−16 9.90x3.90x1.37 1.27P**
CASE 751B
ISSUE M

DATE 18 OCT 2024

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

| PIN | |
|---|---|
| 1. | COLLECTOR |
| 2. | BASE |
| 3. | EMITTER |
| 4. | NO CONNECTION |
| 5. | EMITTER |
| 6. | BASE |
| 7. | COLLECTOR |
| 8. | COLLECTOR |
| 9. | BASE |
| 10. | EMITTER |
| 11. | NO CONNECTION |
| 12. | EMITTER |
| 13. | BASE |
| 14. | COLLECTOR |
| 15. | EMITTER |
| 16. | COLLECTOR |

STYLE 2:

| PIN | |
|---|---|
| 1. | CATHODE |
| 2. | ANODE |
| 3. | NO CONNECTION |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | NO CONNECTION |
| 7. | ANODE |
| 8. | CATHODE |
| 9. | CATHODE |
| 10. | ANODE |
| 11. | NO CONNECTION |
| 12. | CATHODE |
| 13. | CATHODE |
| 14. | NO CONNECTION |
| 15. | ANODE |
| 16. | CATHODE |

STYLE 3:

| PIN | |
|---|---|
| 1. | COLLECTOR, DYE #1 |
| 2. | BASE, #1 |
| 3. | EMITTER, #1 |
| 4. | COLLECTOR, #1 |
| 5. | COLLECTOR, #2 |
| 6. | BASE, #2 |
| 7. | EMITTER, #2 |
| 8. | COLLECTOR, #2 |
| 9. | COLLECTOR, #3 |
| 10. | BASE, #3 |
| 11. | EMITTER, #3 |
| 12. | COLLECTOR, #3 |
| 13. | COLLECTOR, #4 |
| 14. | BASE, #4 |
| 15. | EMITTER, #4 |
| 16. | COLLECTOR, #4 |

STYLE 4:

| PIN | |
|---|---|
| 1. | COLLECTOR, DYE #1 |
| 2. | COLLECTOR, #1 |
| 3. | COLLECTOR, #2 |
| 4. | COLLECTOR, #2 |
| 5. | COLLECTOR, #3 |
| 6. | COLLECTOR, #3 |
| 7. | COLLECTOR, #4 |
| 8. | COLLECTOR, #4 |
| 9. | BASE, #4 |
| 10. | EMITTER, #4 |
| 11. | BASE, #3 |
| 12. | EMITTER, #3 |
| 13. | BASE, #2 |
| 14. | EMITTER, #2 |
| 15. | BASE, #1 |
| 16. | EMITTER, #1 |

STYLE 5:

| PIN | |
|---|---|
| 1. | DRAIN, DYE #1 |
| 2. | DRAIN, #1 |
| 3. | DRAIN, #2 |
| 4. | DRAIN, #2 |
| 5. | DRAIN, #3 |
| 6. | DRAIN, #3 |
| 7. | DRAIN, #4 |
| 8. | DRAIN, #4 |
| 9. | GATE, #4 |
| 10. | SOURCE, #4 |
| 11. | GATE, #3 |
| 12. | SOURCE, #3 |
| 13. | GATE, #2 |
| 14. | SOURCE, #2 |
| 15. | GATE, #1 |
| 16. | SOURCE, #1 |

STYLE 6:

| PIN | |
|---|---|
| 1. | CATHODE |
| 2. | CATHODE |
| 3. | CATHODE |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | CATHODE |
| 7. | CATHODE |
| 8. | CATHODE |
| 9. | ANODE |
| 10. | ANODE |
| 11. | ANODE |
| 12. | ANODE |
| 13. | ANODE |
| 14. | ANODE |
| 15. | ANODE |
| 16. | ANODE |

STYLE 7:

| PIN | |
|---|---|
| 1. | SOURCE N-CH |
| 2. | COMMON DRAIN (OUTPUT) |
| 3. | COMMON DRAIN (OUTPUT) |
| 4. | GATE P-CH |
| 5. | COMMON DRAIN (OUTPUT) |
| 6. | COMMON DRAIN (OUTPUT) |
| 7. | COMMON DRAIN (OUTPUT) |
| 8. | SOURCE P-CH |
| 9. | SOURCE P-CH |
| 10. | COMMON DRAIN (OUTPUT) |
| 11. | COMMON DRAIN (OUTPUT) |
| 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE N-CH |
| 14. | COMMON DRAIN (OUTPUT) |
| 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE N-CH |

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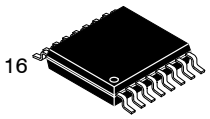
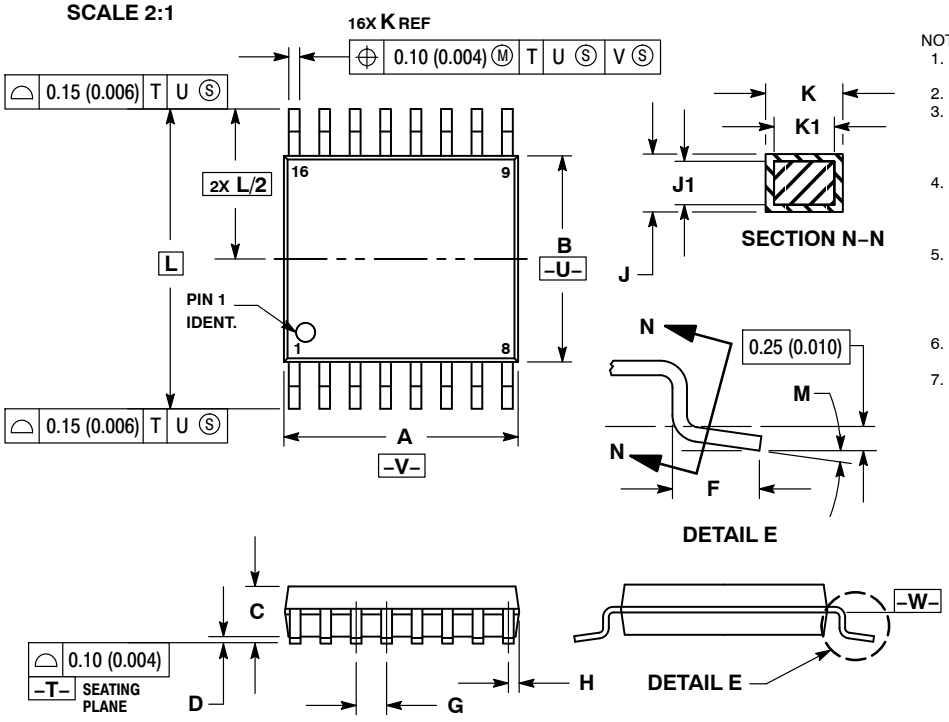



SCALE 2:1

**TSSOP−16 WB**
CASE 948F
ISSUE B

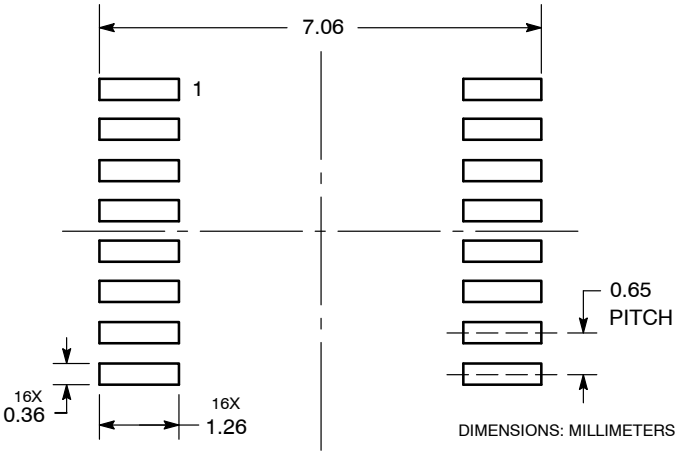
DATE 19 OCT 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

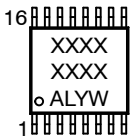
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
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