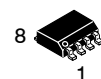


# Phase-Frequency Detector

## MCH12140, MCK12140



SOIC-8  
D SUFFIX  
CASE 751

### Description

The MCH/K12140 is a phase frequency-detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with high performance VCO such as the MC100EL1648, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase-frequency detector with the maximum frequency extending to 800 MHz.

When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO. See AND8040 for further information. The device is packaged in a small outline, surface mount 8-lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL™ 10H logic levels while the MCK12140 is compatible to 100 K ECL logic levels. This device can also be used in +5.0 V systems. See AND8020 for termination information

### Features

- 800 MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75 kΩ Internal Input Pulldown Resistors
- >1000 V ESD Protection
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

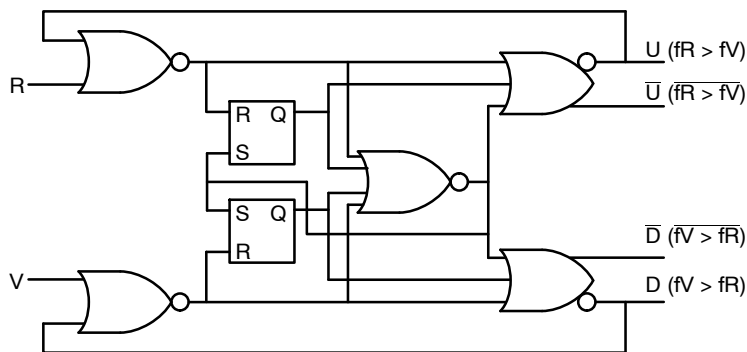
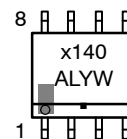


Figure 1. Logic Diagram

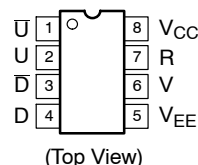
For proper operation, the input edge rate of the R and V inputs should be less than 5.0 ns.

### MARKING DIAGRAM



- x = H or K
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

| Device       | Package          | Shipping†          |
|--------------|------------------|--------------------|
| MCK12140DG   | SOIC-8 (Pb-Free) | 98 Units / Tube    |
| MCK12140DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |

### DISCONTINUED (Note 1)

|            |                  |                 |
|------------|------------------|-----------------|
| MCH12140DG | SOIC-8 (Pb-Free) | 98 Units / Tube |
|------------|------------------|-----------------|

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your onsemi representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).

# MCH12140, MCK12140

**Table 1. TRUTH TABLE\***

| Input |   | Output |   |   |   | Input |   | Output |   |   |   |
|-------|---|--------|---|---|---|-------|---|--------|---|---|---|
| R     | V | U      | D | U | D | R     | V | U      | D | U | D |
| 0     | 0 | X      | X | X | X | 1     | 1 | 0      | 0 | 1 | 1 |
| 0     | 1 | X      | X | X | X | 1     | 0 | 0      | 0 | 1 | 1 |
| 1     | 1 | X      | X | X | X | 1     | 1 | 0      | 1 | 1 | 0 |
| 0     | 1 | X      | X | X | X | 1     | 0 | 0      | 1 | 1 | 0 |
| 1     | 1 | 1      | 0 | 0 | 1 | 1     | 1 | 0      | 1 | 1 | 0 |
| 0     | 1 | 1      | 0 | 0 | 1 | 0     | 1 | 0      | 1 | 1 | 0 |
| 1     | 1 | 1      | 0 | 0 | 1 | 1     | 1 | 0      | 0 | 1 | 1 |
| 1     | 0 | 1      | 0 | 0 | 1 |       |   |        |   |   |   |

\*This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

**Table 2. H-SERIES DC CHARACTERISTICS** ( $V_{EE} = V_{EE(min)} - V_{EE(max)}$ ;  $V_{CC} = GND$  (Note 2), unless otherwise noted.)

| Symbol   | Characteristic      | -40°C |       | 0°C   |       | 25°C  |       | 70°C  |       | Unit |
|----------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
|          |                     | Min   | Max   | Min   | Max   | Min   | Max   | Min   | Max   |      |
| $V_{OH}$ | Output HIGH Voltage | -1080 | -890  | -1020 | -840  | -980  | -810  | -910  | -720  | mV   |
| $V_{OL}$ | Output LOW Voltage  | -1950 | -1650 | -1950 | -1630 | -1950 | -1630 | -1950 | -1595 | mV   |
| $V_{IH}$ | Input HIGH Voltage  | -1230 | -890  | -1170 | -840  | -1130 | -810  | -1060 | -720  | mV   |
| $V_{IL}$ | Input LOW Voltage   | -1950 | -1500 | -1950 | -1480 | -1950 | -1480 | -1950 | -1445 | mV   |
| $I_{IL}$ | Input LOW Current   | 0.5   | -     | 0.5   | -     | 0.5   | -     | 0.3   | -     | μA   |

**Table 3. K-SERIES DC CHARACTERISTICS** ( $V_{EE} = V_{EE(min)} - V_{EE(max)}$ ;  $V_{CC} = GND$  (Note 3), unless otherwise noted.)

| Symbol    | Characteristic      | -40°C |       |       | 0°C to 70°C |       |       | Condition                                  | Unit |
|-----------|---------------------|-------|-------|-------|-------------|-------|-------|--|------|
|           |                     | Min   | Typ   | Max   | Min         | Typ   | Max   |  |      |
| $V_{OH}$  | Output HIGH Voltage | -1085 | -1005 | -880  | -1025       | -955  | -880  | $V_{IN} = V_{IH(max)}$<br>or $V_{IL(min)}$ | mV   |
| $V_{OL}$  | Output LOW Voltage  | -1830 | -1695 | -1555 | -1810       | -1705 | -1620 |  | mV   |
| $V_{OHA}$ | Output HIGH Voltage | -1095 | -     | -     | -1035       | -     | -     | $V_{IN} = V_{IH(min)}$<br>or $V_{IL(max)}$ | mV   |
| $V_{OLA}$ | Output LOW Voltage  | -     | -     | -1555 | -           | -     | -1610 |  | mV   |
| $V_{IH}$  | Input HIGH Voltage  | -1165 | -     | -880  | -1165       | -     | -880  | -  | mV   |
| $V_{IL}$  | Input LOW Voltage   | -1810 | -     | -1475 | -1810       | -     | -1475 | -  | mV   |
| $I_{IL}$  | Input LOW Current   | 0.5   | -     | -     | 0.5         | -     | -     | $V_{IN} = V_{IL(max)}$                     | μA   |

# MCH12140, MCK12140

**Table 4. MAXIMUM RATINGS**

| Symbol    | Rating                                | Value        | Unit |
|-----------|---------------------------------------|--------------|------|
| $V_{EE}$  | Power Supply ( $V_{CC} = 0$ V)        | -8.0 to 0    | VDC  |
| $V_I$     | Input Voltage ( $V_{CC} = 0$ V)       | 0 to -6.0    | VDC  |
| $I_{out}$ | Output Current<br>Continuous<br>Surge | 50<br>100    | mA   |
| $T_A$     | Operating Temperature Range           | -40 to +70   | °C   |
| $V_{EE}$  | Operating Range (Note 4)              | -5.7 to -4.2 | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: ESD data available upon request.

- 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained. Outputs are terminated through a 50  $\Omega$  resistor to -2.0 V except where otherwise specified on the individual data sheets.
- This table replaces the three tables traditionally seen in ECL 100 K data books. The same DC parameter values at  $V_{EE} = -4.5$  V now apply across the full  $V_{EE}$  range of -4.2 V to -5.5 V. Outputs are terminated through a 50  $\Omega$  resistor to -2.0 V except where otherwise specified on the individual data sheets.
- Parametric values specified at:  
H-Series: -4.20 V to -5.50 V  
K-Series: -4.94 V to -5.50 V

**Table 5. DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min}) - V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}$ , unless otherwise noted.)

| Symbol   | Characteristic                 | -40°C |      |      | 0°C   |      |      | 25°C  |      |      | 70°C  |      |      | Unit    |
|----------|--------------------------------|-------|------|------|-------|------|------|-------|------|------|-------|------|------|---------|
|          |                                | Min   | Typ  | Max  | Min   | Typ  | Max  | Min   | Typ  | Max  | Min   | Typ  | Max  |         |
| $I_{EE}$ | Power Supply Current<br>H<br>K | -     | 45   | -    | 38    | 45   | 52   | 38    | 45   | 52   | 38    | 45   | 52   | mA      |
|          |                                | -     | 45   | -    | 38    | 45   | 52   | 38    | 45   | 52   | 42    | 50   | 58   |         |
| $V_{EE}$ | Power Supply Voltage<br>H<br>K | -4.75 | -5.2 | -5.5 | -4.75 | -5.2 | -5.5 | -4.75 | -5.2 | -5.5 | -4.75 | -5.2 | -5.5 | V       |
|          |                                | -4.20 | -4.5 | -5.5 | -4.20 | -4.5 | -5.5 | -4.20 | -4.5 | -5.5 | -4.20 | -4.5 | -5.5 |         |
| $I_{IH}$ | Input HIGH Current             | -     | -    | 150  | -     | -    | 150  | -     | -    | 150  | -     | -    | 150  | $\mu$ A |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

**Table 6. AC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min}) - V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}$ , unless otherwise noted.)

| Symbol                 | Characteristic                              | -40°C |     |     | 0°C |     |     | 25°C |     |     | 70°C |     |     | Unit |
|------------------------|---|-------|-----|-----|-----|-----|-----|------|-----|-----|------|-----|-----|------|
|                        |   | Min   | Typ | Max | Min | Typ | Max | Min  | Typ | Max | Min  | Typ | Max |      |
| $F_{MAX}$              | Maximum Toggle Frequency                    | -     | 800 | -   | 650 | 800 | -   | 650  | 800 | -   | 650  | 800 | -   | -    |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay-to-Output<br>R, V to D, U | 250   | 375 | 500 | 250 | 375 | 500 | 250  | 375 | 500 | 250  | 375 | 500 | ps   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times<br>Q (20 to 80%)     | -     | 225 | -   | 100 | 225 | 350 | 100  | 225 | 350 | 100  | 225 | 350 | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

APPLICATIONS INFORMATION

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the “lead” or “lag” phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

The operation of the 12140 can best be described using the plots of Figure 2. Figure 2 plots the average value of  $\bar{U}$ ,  $\bar{D}$  and the difference between  $\bar{U}$  and  $\bar{D}$  versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:

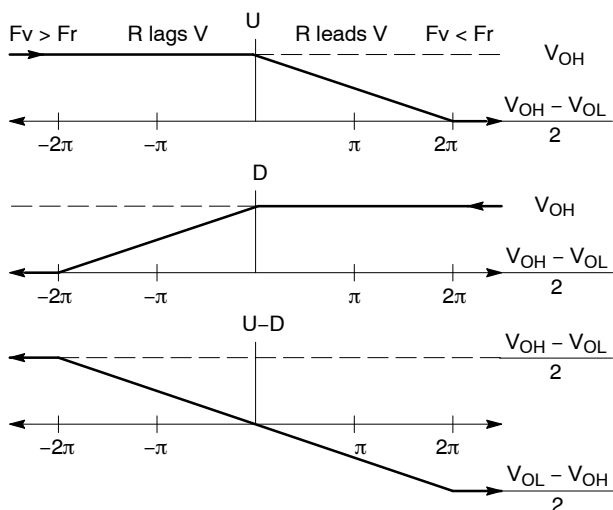


Figure 2. Average Output Voltage vs. Phase Difference

**R lags V in phase**

When the R and V inputs are equal in frequency and the phase of R lags that of V the  $\bar{U}$  output will stay HIGH while the  $\bar{D}$  output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a  $180^\circ$  out of phase condition. The signal on  $\bar{D}$  indicates to the VCO to decrease in frequency to bring the loop into lock.

**V frequency > R frequency**

When the frequency of V is greater than that of R the 12140 behaves in a similar fashion as above. Again the signal on  $\bar{D}$  indicates that the VCO frequency must be decreased to bring the loop into lock.

**R leads V in phase**

When the R and V inputs are equal in frequency and the phase of R leads that of V the  $\bar{D}$  output will stay HIGH while the  $\bar{U}$  output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a  $180^\circ$  out of phase condition. The signal on  $\bar{U}$  indicates to the VCO to increase in frequency to bring the loop into lock.

**V frequency < R frequency**

When the frequency of V is less than that of R the 12140 behaves in a similar fashion as above. Again the signal on  $\bar{U}$  indicates that the VCO frequency must be decreased to bring the loop into lock.

From Figure 2 when V and R are at the same frequency and in phase the value of  $\bar{U} - \bar{D}$  is zero thus providing a zero error voltage to the VCO. This situation indicates the loop is in lock and the 12140 action will maintain the loop in its locked state.



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |  |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2  |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p><b>STYLE 2:</b><br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p><b>STYLE 6:</b><br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p><b>STYLE 7:</b><br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p><b>STYLE 11:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p><b>STYLE 14:</b><br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p><b>STYLE 18:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p><b>STYLE 19:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p><b>STYLE 26:</b><br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p><b>STYLE 27:</b><br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p><b>STYLE 28:</b><br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p><b>STYLE 29:</b><br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |   |   |

|                         |                    |   |
|-------------------------|--------------------|---|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42564B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-8 NB</b>   | <b>PAGE 2 OF 2</b>  |

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

