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Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N-Channel Enhancement-Mode Silicon Gate

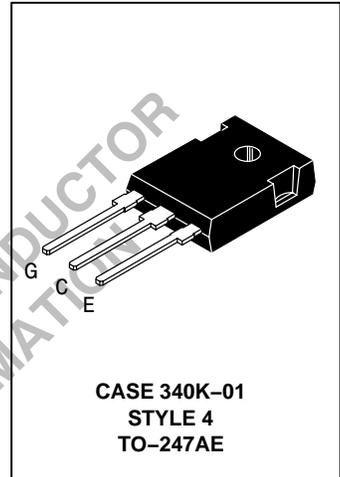
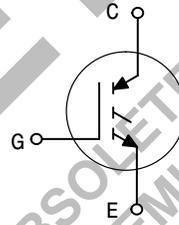
MGW20N120

Motorola Preferred Device

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

IGBT IN TO-247
20 A @ 90°C
28 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

- Industry Standard High Power TO-247 Package with Isolated Mounting Hole
- High Speed E_{off} : 160 μ J/A typical at 125°C
- High Short Circuit Capability – 10 μ s minimum
- Robust High Voltage Termination



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	1200	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V_{CGR}	1200	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$	I_{C25}	28	Adc
— Continuous @ $T_C = 90^\circ\text{C}$	I_{C90}	20	
— Repetitive Pulsed Current (1)	I_{CM}	56	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	174	Watts
Derate above 25°C		1.39	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Short Circuit Withstand Time ($V_{CC} = 720 \text{ Vdc}, V_{GE} = 15 \text{ Vdc}, T_J = 125^\circ\text{C}, R_G = 20 \Omega$)	t_{sc}	10	μ s
Thermal Resistance — Junction to Case – IGBT	$R_{\theta JC}$	0.7	°C/W
— Junction to Ambient	$R_{\theta JA}$	35	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C
Mounting Torque, 6-32 or M3 screw		10 lbf•in (1.13 N•m)	

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

MGW20N120

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage (V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positive)	V _{(BR)CES}	1200 —	— 870	— —	Vdc mV/°C
Emitter-to-Collector Breakdown Voltage (V _{GE} = 0 Vdc, I _{EC} = 100 mAdc)	V _{(BR)ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current (V _{CE} = 1200 Vdc, V _{GE} = 0 Vdc) (V _{CE} = 1200 Vdc, V _{GE} = 0 Vdc, T _J = 125°C)	I _{CES}	— —	— —	100 2500	μAdc
Gate-Body Leakage Current (V _{GE} = ± 20 Vdc, V _{CE} = 0 Vdc)	I _{GES}	—	—	250	nAdc

ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage (V _{GE} = 15 Vdc, I _C = 10 Adc) (V _{GE} = 15 Vdc, I _C = 10 Adc, T _J = 125°C) (V _{GE} = 15 Vdc, I _C = 20 Adc)	V _{CE(on)}	— — —	2.42 2.36 2.90	3.54 — 4.99	Vdc
Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V _{CE} = 10 Vdc, I _C = 20 Adc)	g _{fe}	—	12	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	1860	—	pF
Output Capacitance		C _{oes}	—	122	—	
Transfer Capacitance		C _{res}	—	29	—	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{CC} = 720 Vdc, I _C = 20 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω) Energy losses include "tail"	t _{d(on)}	—	88	—	ns
Rise Time		t _r	—	103	—	
Turn-Off Delay Time		t _{d(off)}	—	190	—	
Fall Time		t _f	—	284	—	
Turn-Off Switching Loss		E _{off}	—	1.65	2.75	
Turn-On Delay Time	(V _{CC} = 720 Vdc, I _C = 20 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω, T _J = 125°C) Energy losses include "tail"	t _{d(on)}	—	83	—	ns
Rise Time		t _r	—	107	—	
Turn-Off Delay Time		t _{d(off)}	—	216	—	
Fall Time		t _f	—	494	—	
Turn-Off Switching Loss		E _{off}	—	3.19	—	
Gate Charge	(V _{CC} = 720 Vdc, I _C = 20 Adc, V _{GE} = 15 Vdc)	Q _T	—	62	—	nC
		Q ₁	—	21	—	
		Q ₂	—	25	—	

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L _E	—	13	—	nH
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(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

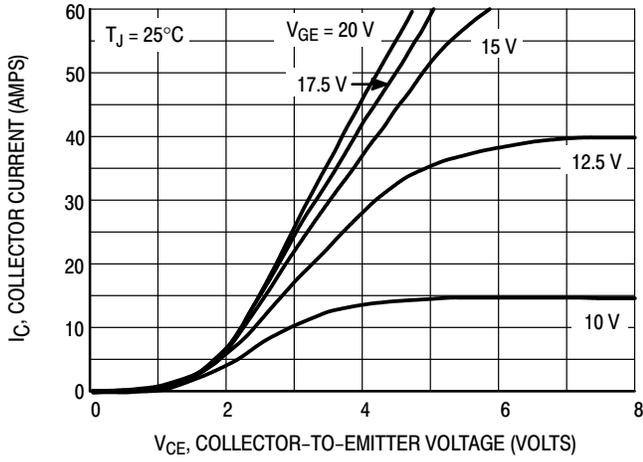


Figure 1. Output Characteristics

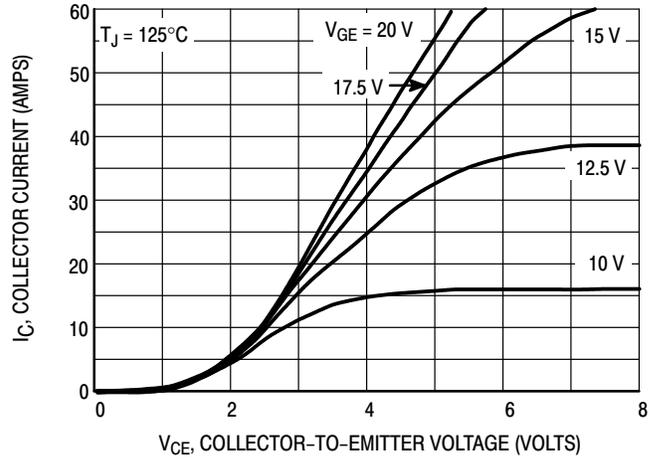


Figure 2. Output Characteristics

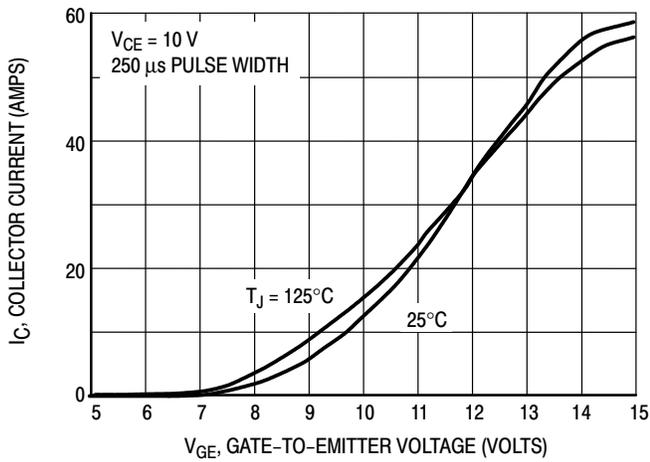


Figure 3. Transfer Characteristics

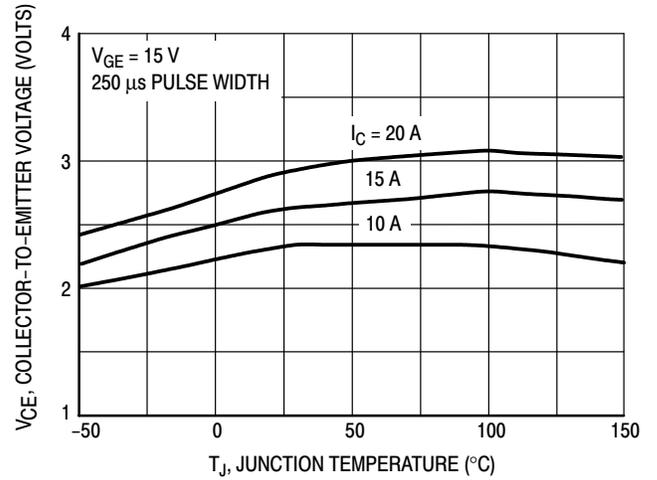


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

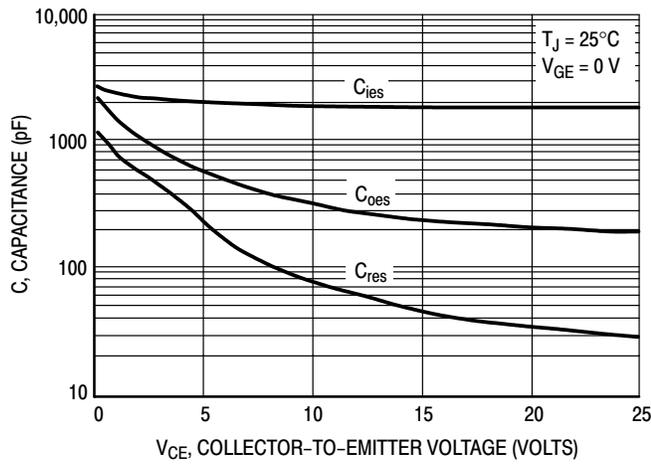


Figure 5. Capacitance Variation

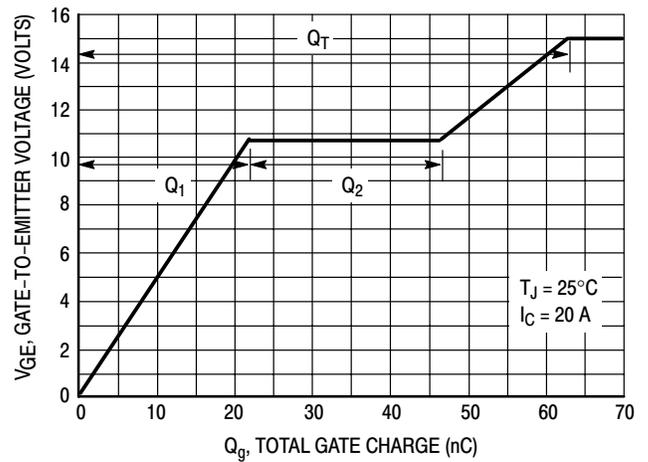


Figure 6. Gate-to-Emitter Voltage versus Total Charge

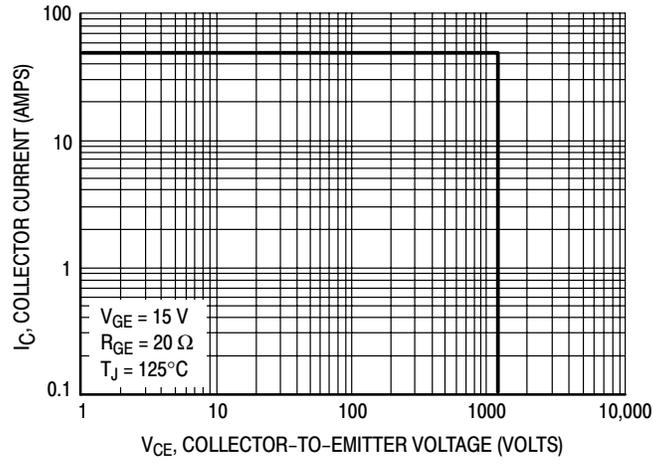


Figure 7. Reverse Biased Safe Operating Area

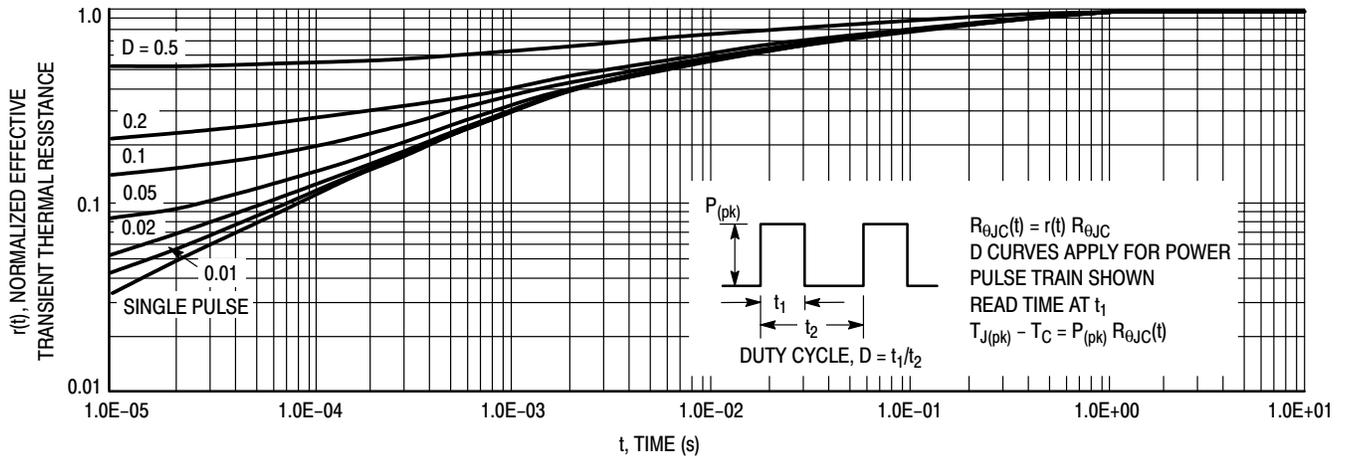
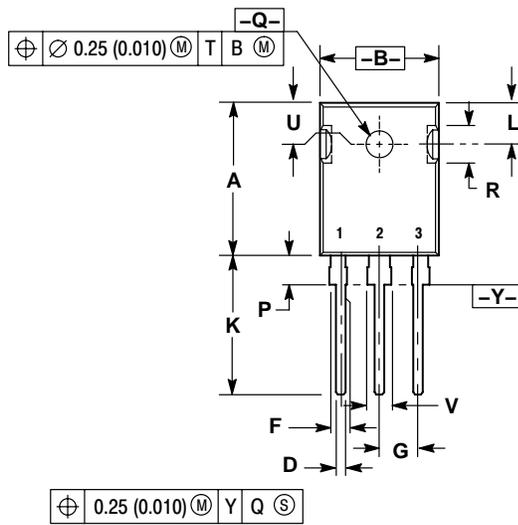


Figure 8. Thermal Response

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

CASE 340K-01
 TO-247AE
 ISSUE A

- STYLE 4:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

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