

# Complementary Darlington Silicon Power Transistors

## MJ11021 (PNP) MJ11022 (NPN)

Complementary Darlington Silicon Power Transistors are designed for use as general purpose amplifiers, low frequency switching and motor control applications.

### Features

- High dc Current Gain @ 10 Adc –  $h_{FE} = 400$  Min (All Types)
- Collector-Emitter Sustaining Voltage  
 $V_{CEO(sus)} = 250$  Vdc (Min) – MJ11022, 21
- Low Collector-Emitter Saturation  
 $V_{CE(sat)} = 1.0$  V (Typ) @  $I_C = 5.0$  A  
 $= 1.8$  V (Typ) @  $I_C = 10$  A
- 100% SOA Tested @  $V_{CE} = 44$  V  
 $I_C = 4.0$  A  
 $t = 250$  ms
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	Vdc
Collector-Base Voltage	$V_{CBO}$	250	Vdc
Emitter-Base Voltage	$V_{EBO}$	50	Vdc
Collector Current – Continuous – Peak (Note 2)	$I_C$	15 30	Adc
Base Current	$I_B$	0.5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	175 1.16	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +175 -65 to +200	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

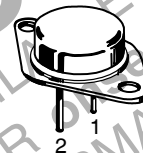
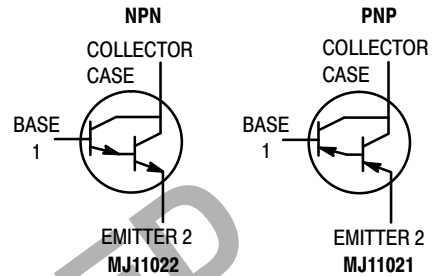
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.86	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq 10\%$ .

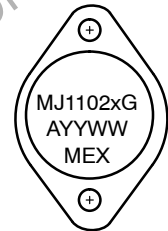
\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

## 15 AMPERE COMPLEMENTARY DARLINGTON POWER TRANSISTORS 250 VOLTS, 175 WATTS



TO-204 (TO-3)  
CASE 1-07  
STYLE 1

### MARKING DIAGRAM



MJ1102x = Device Code  
x = 1 or 2  
G = Pb-Free Package  
A = Location Code  
YY = Year  
WW = Work Week  
MEX = Country of Origin

### ORDERING INFORMATION

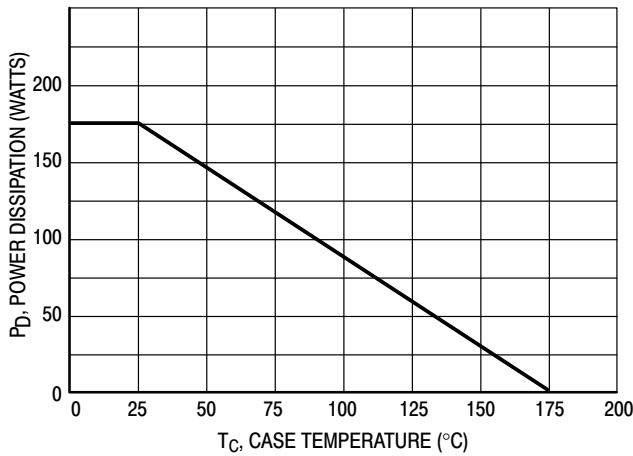
Device	Package	Shipping
MJ11021G	TO-3 (Pb-Free)	100 Units/Tray
MJ11022G	TO-3 (Pb-Free)	100 Units/Tray

### DISCONTINUED (Note 1)

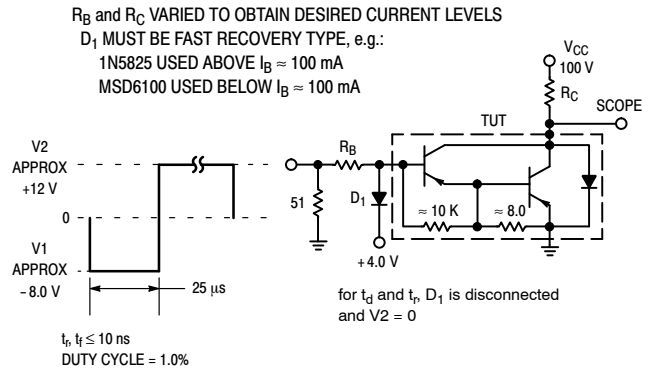
MJ11021	TO-3	100 Units/Tray
MJ11022	TO-3	100 Units/Tray

1. **DISCONTINUED:** These devices are not available. Please contact your onsemi representative for information. The most current information on these devices may be available on [www.onsemi.com](#).

# MJ11021 (PNP) MJ11022 (NPN)



**Figure 1. Power Derating**



For NPN test circuit reverse diode and voltage polarities.

**Figure 2. Switching Times Test Circuit**

**ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Sustaining Voltage (Note 2) (I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)	MJ11021, MJ11022	V <sub>CEQ(sus)</sub>	250	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 125, I <sub>B</sub> = 0)	MJ11021, MJ11022	I <sub>CEO</sub>	–	1.0	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>J</sub> = 150 °C)		I <sub>CEV</sub>	–	0.5 5.0	mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)		I <sub>EBO</sub>	–	2.0	mAdc
<b>ON CHARACTERISTICS</b> (Note 2)					
DC Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 5.0 Vdc) (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 5.0 Vdc)		h <sub>FE</sub>	400 100	15,000 –	–
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 100 mA) (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 150 mA)		V <sub>CE(sat)</sub>	–	2.0 3.4	Vdc
Base-Emitter On Voltage (I <sub>C</sub> = 10 A, V <sub>CE</sub> = 5.0 Vdc)		V <sub>BE(on)</sub>	–	2.8	Vdc
Base-Emitter Saturation Voltage (I <sub>C</sub> = 15 Adc, I <sub>B</sub> = 150 mA)		V <sub>BE(sat)</sub>	–	3.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current-Gain Bandwidth Product (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz)		[h <sub>fe</sub> ]	3.0	–	Mhz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz) MJ11022 MJ11021		C <sub>ob</sub>	–	400 600	pF
Small-Signal Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)		h <sub>fe</sub>	75	–	–
<b>SWITCHING CHARACTERISTICS</b>					
			<b>Typical</b>		
			<b>NPN</b>	<b>PNP</b>	
Delay Time	(V <sub>CC</sub> = 100 V, I <sub>C</sub> = 10 A, I <sub>B</sub> = 100 mA V <sub>BE(off)</sub> = 50 V) (See Figure 2)	t <sub>d</sub>	150	75	ns
Rise Time		t <sub>r</sub>	1.2	0.5	µs
Storage Time		t <sub>s</sub>	4.4	2.7	µs
Fall Time		t <sub>f</sub>	10.0	2.5	µs

1. Pulsed Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.

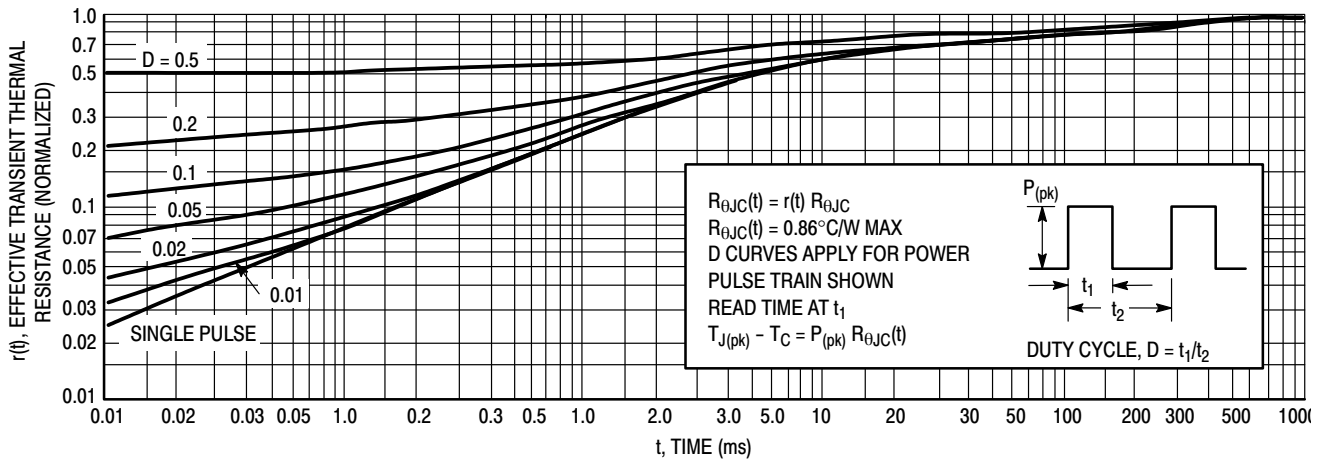


Figure 3. Thermal Response

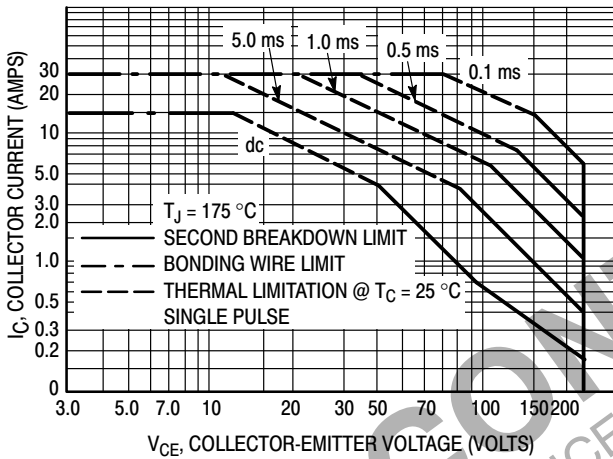


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

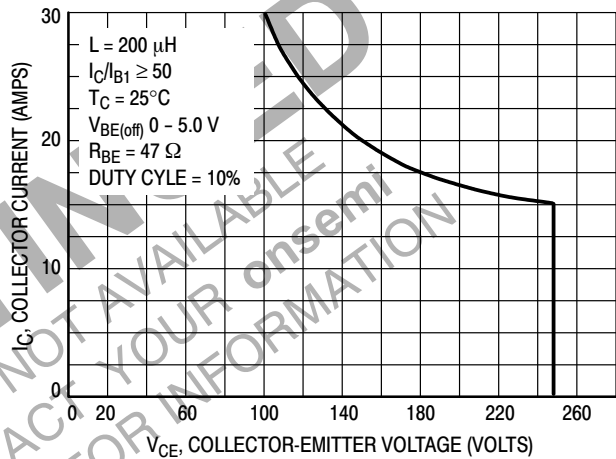


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on  $T_{J(pk)} = 175^\circ\text{C}$ ,  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 175^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

MJ11021 (PNP) MJ11022 (NPN)

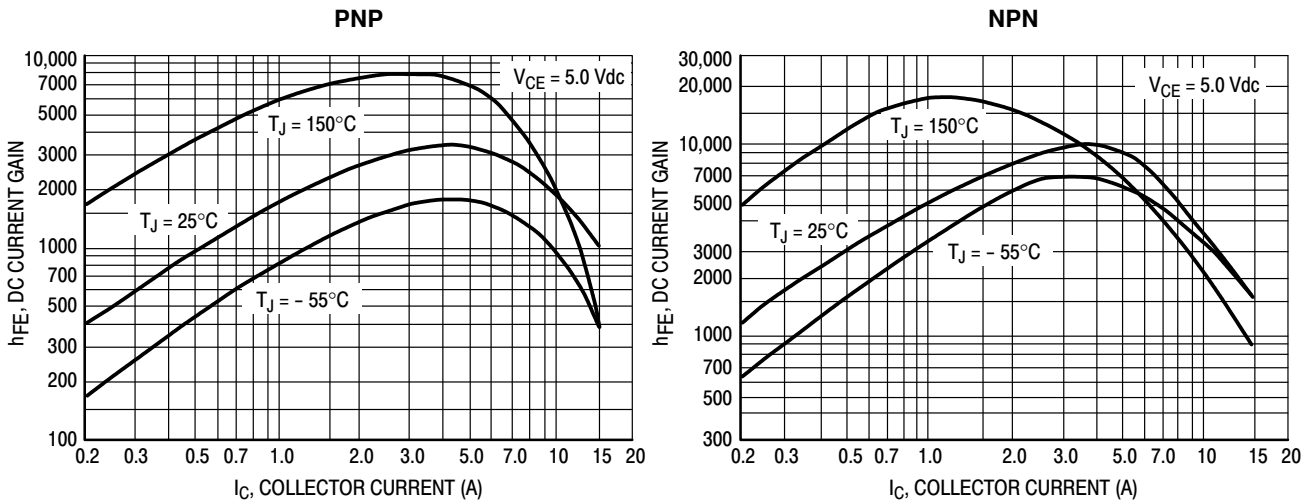


Figure 6. DC Current Gain

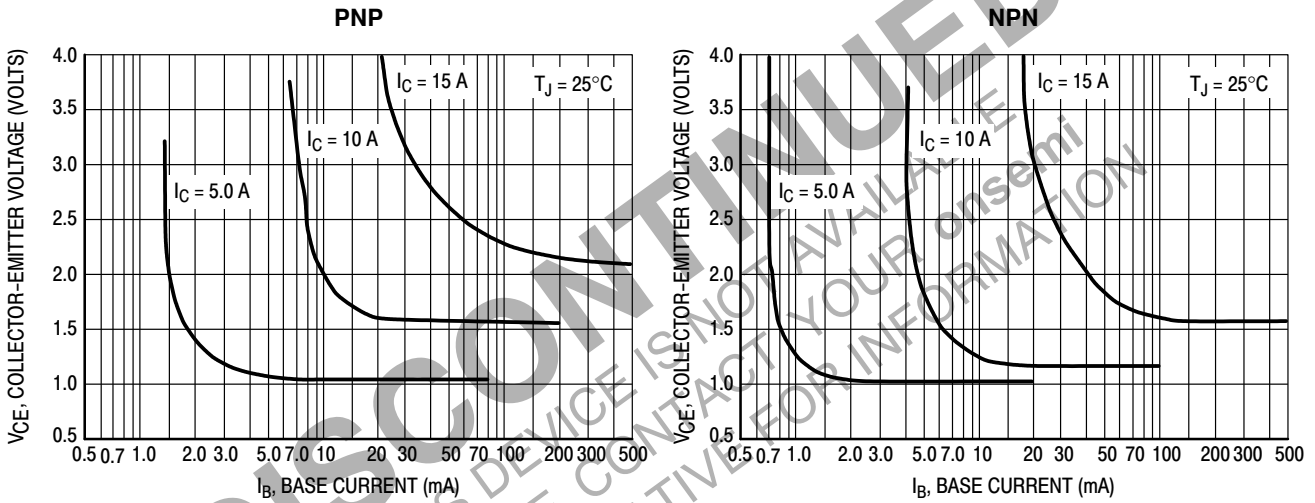


Figure 7. Collector Saturation Region

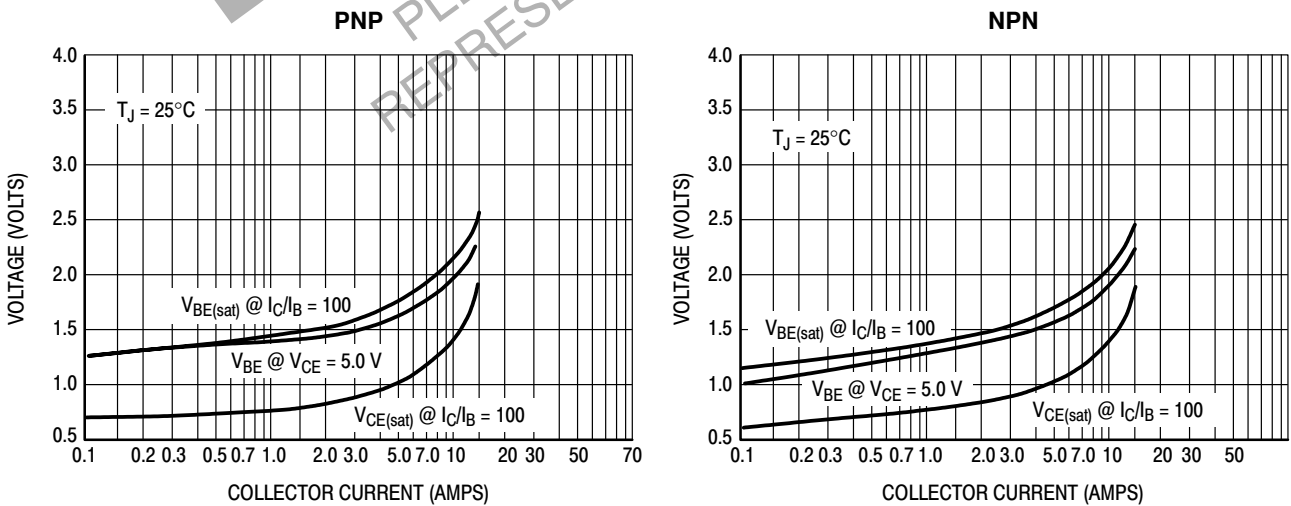


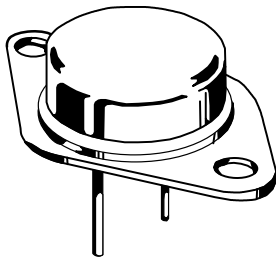
Figure 8. "On" Voltages

REVISION HISTORY

Revision	Description of Changes	Date
5	Data Sheet Discontinued.	1/14/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

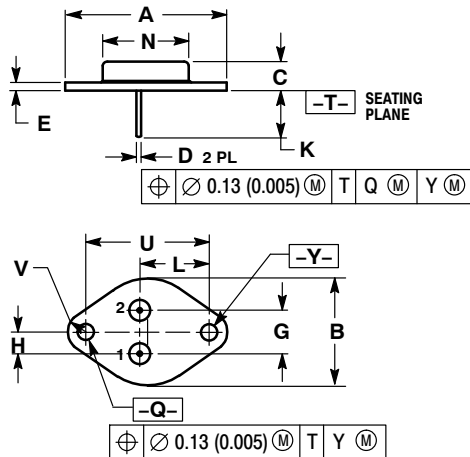
**DISCONTINUED**  
THIS DEVICE IS NOT AVAILABLE  
PLEASE CONTACT YOUR onsemi  
REPRESENTATIVE FOR INFORMATION



TO-204 (TO-3)  
CASE 1-07  
ISSUE Z

DATE 10 MAR 2000

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

- |  |  |   |   |   |
|--|--|---|---|---|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. EMITTER<br/>CASE: COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>CASE: EMITTER</p> | <p>STYLE 3:<br/>PIN 1. GATE<br/>2. SOURCE<br/>CASE: DRAIN</p>           | <p>STYLE 4:<br/>PIN 1. GROUND<br/>2. INPUT<br/>CASE: OUTPUT</p>       | <p>STYLE 5:<br/>PIN 1. CATHODE<br/>2. EXTERNAL TRIP/DELAY<br/>CASE: ANODE</p> |
| <p>STYLE 6:<br/>PIN 1. GATE<br/>2. EMITTER<br/>CASE: COLLECTOR</p> | <p>STYLE 7:<br/>PIN 1. ANODE<br/>2. OPEN<br/>CASE: CATHODE</p>     | <p>STYLE 8:<br/>PIN 1. CATHODE #1<br/>2. CATHODE #2<br/>CASE: ANODE</p> | <p>STYLE 9:<br/>PIN 1. ANODE #1<br/>2. ANODE #2<br/>CASE: CATHODE</p> |   |

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DESCRIPTION:	TO-204 (TO-3)	PAGE 1 OF 1

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