

MJD18002D2

Bipolar NPN Transistor High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector–Emitter Diode and Built–In Efficient Antisaturation Network

The MJD18002D2 is a state-of-the-art high speed, high gain bipolar transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (± 150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no longer a need to guarantee an h_{FE} window.

Features

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ $I_C = 100$ mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic V_{CEsat}
- Characteristics Make It Suitable for PFC Application
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Six Sigma® Process Providing Tight and Reproducible Parameter Spreads
- Pb–Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	11	Vdc
Collector Current – Continuous	I_C	2.0	Adc
– Peak (Note 1)	I_{CM}	5.0	
Base Current – Continuous	I_B	1.0	Adc
– Peak (Note 1)	I_{BM}	2.0	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50 0.4	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

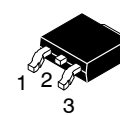
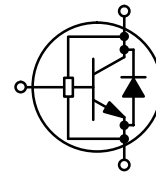
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%.



ON Semiconductor®

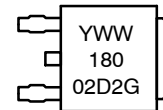
<http://onsemi.com>

POWER TRANSISTOR
2 AMPERES
1000 VOLTS, 50 WATTS



DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week
18002D2 = Device Code
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJD18002D2T4	DPAK	3000/Tape & Reel
MJD18002D2T4G	DPAK (Pb–Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit		
OFF CHARACTERISTICS							
Collector-Emitter Sustaining Voltage (I _C = 100 mA, L = 25 mH)	V _{CEO(sus)}	450	570	–	Vdc		
Collector-Base Breakdown Voltage (I _{CBO} = 1 mA)	V _{CB0}	1000	1100	–	Vdc		
Emitter-Base Breakdown Voltage (I _{EBO} = 1 mA)	V _{EBO}	11	14	–	Vdc		
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	I _{CEO}	–	–	100	μAdc		
Collector Cutoff Current (V _{CE} = Rated V _{CEs} , V _{EB} = 0) (V _{CE} = 500 V, V _{EB} = 0)	I _{CES}	–	–	100 500 100	μAdc		
Emitter-Cutoff Current (V _{EB} = 10 Vdc, I _C = 0)	I _{EBO}	–	–	500	μAdc		
ON CHARACTERISTICS							
Base-Emitter Saturation Voltage (I _C = 0.4 Adc, I _B = 40 mAdc) (I _C = 1.0 Adc, I _B = 0.2 Adc)	V _{BE(sat)}	–	0.78 0.87	1.0 1.1	Vdc		
Collector-Emitter Saturation Voltage (I _C = 0.4 Adc, I _B = 40 mAdc) (I _C = 1.0 Adc, I _B = 0.2 Adc)	V _{CE(sat)}	–	0.36 0.50 0.40 0.65	0.6 1.0 0.75 1.2	Vdc		
DC Current Gain (I _C = 0.4 Adc, V _{CE} = 1.0 Vdc) (I _C = 1.0 Adc, V _{CE} = 1.0 Vdc)	h _{FE}	14 8.0	25 15	– –	–		
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I _C = 0.5 Adc, V _{CE} = 10 Vdc, f = 1 MHz)	f _t	–	13	–	MHz		
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1 MHz)	C _{ob}	–	50	100	pF		
Input Capacitance (V _{EB} = 8 Vdc)	C _{ib}	–	340	500	pF		
DIODE CHARACTERISTICS							
Forward Diode Voltage (I _{EC} = 1.0 Adc) (I _{EC} = 0.4 Adc)	V _{EC}	–	1.2 1.0 0.6	1.5 1.3	Vdc		
Forward Recovery Time (I _F = 0.4 Adc, di/dt = 10 A/μs) (I _F = 1.0 Adc, di/dt = 10 A/μs)	t _{fr}	–	517 480	–	ns		
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage Determined 1 μs and 3 μs respectively after rising I _{B1} reaches 90% of final I _{B1}	I _C = 0.4 Adc I _{B1} = 40 mA V _{CC} = 300 Vdc	@ 1 μs @ T _C = 25°C	V _{CE(dsat)}	–	7.4	–	V
		@ 3 μs @ T _C = 25°C		–	2.5	–	
	I _C = 1 Adc I _{B1} = 0.2 A V _{CC} = 300 Vdc	@ 1 μs @ T _C = 25°C		–	11.7	–	
		@ 3 μs @ T _C = 25°C		–	1.3	–	

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS: Resistive Load (D.C.S. 10%, Pulse Width = 40 μs)							
Turn-on Time	$I_C = 0.4 \text{ Adc}$, $I_{B1} = 40 \text{ mA dc}$ $I_{B2} = 200 \text{ mA dc}$ $V_{CC} = 300 \text{ V dc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	-	225	350	ns
		@ $T_C = 125^\circ\text{C}$		-	375	-	
Turn-off Time	$I_C = 0.4 \text{ Adc}$, $I_{B1} = 40 \text{ mA dc}$ $I_{B2} = 200 \text{ mA dc}$ $V_{CC} = 300 \text{ V dc}$	@ $T_C = 25^\circ\text{C}$	t_{off}	0.8	-	1.1	μs
		@ $T_C = 125^\circ\text{C}$		-	1.5	-	
Turn-on Time	$I_C = 1.0 \text{ Adc}$, $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ V dc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	-	100	150	ns
		@ $T_C = 125^\circ\text{C}$		-	94	-	
Turn-off Time	$I_C = 1.0 \text{ Adc}$, $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ V dc}$	@ $T_C = 25^\circ\text{C}$	t_{off}	0.95	-	1.25	μs
		@ $T_C = 125^\circ\text{C}$		-	1.5	-	
SWITCHING CHARACTERISTICS: Inductive Load ($V_{clamp} = 300 \text{ V}$, $V_{CC} = 15 \text{ V}$, $L = 200 \mu\text{H}$)							
Fall Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mA dc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_f	-	130	175	ns
		@ $T_C = 125^\circ\text{C}$		-	120	-	
Storage Time		@ $T_C = 25^\circ\text{C}$	t_s	0.4	-	0.7	μs
		@ $T_C = 125^\circ\text{C}$		-	-		
Cross-over Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mA dc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_c	-	110	175	ns
		@ $T_C = 125^\circ\text{C}$		-	100	-	
Fall Time		@ $T_C = 25^\circ\text{C}$	t_f	-	130	175	ns
		@ $T_C = 125^\circ\text{C}$		-	140	-	
Storage Time	$I_C = 0.8 \text{ Adc}$ $I_{B1} = 160 \text{ mA dc}$ $I_{B2} = 160 \text{ mA dc}$	@ $T_C = 25^\circ\text{C}$	t_s	2.1	-	2.4	μs
		@ $T_C = 125^\circ\text{C}$		-	3.0	-	
Cross-over Time		@ $T_C = 25^\circ\text{C}$	t_c	-	275	350	ns
		@ $T_C = 125^\circ\text{C}$		-	350	-	
Fall Time	$I_C = 1.0 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_f	-	100	150	ns
		@ $T_C = 125^\circ\text{C}$		-	100	-	
Storage Time		@ $T_C = 25^\circ\text{C}$	t_s	-	1.05	1.2	μs
		@ $T_C = 125^\circ\text{C}$		-	1.45	-	
Cross-over Time	$I_C = 1.0 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_c	-	100	150	ns
		@ $T_C = 125^\circ\text{C}$		-	115	-	

TYPICAL STATIC CHARACTERISTICS

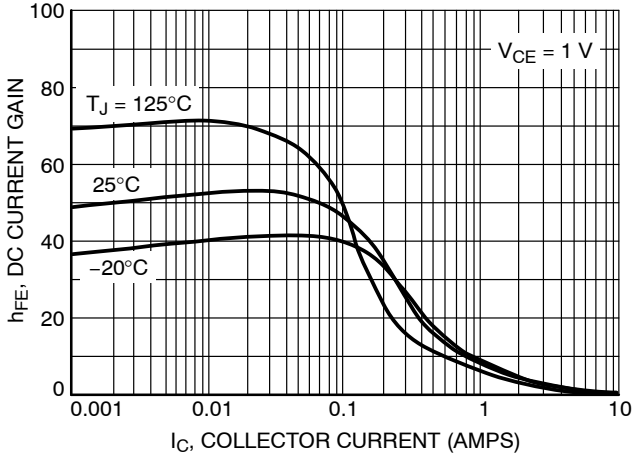


Figure 1. DC Current Gain @ 1 V

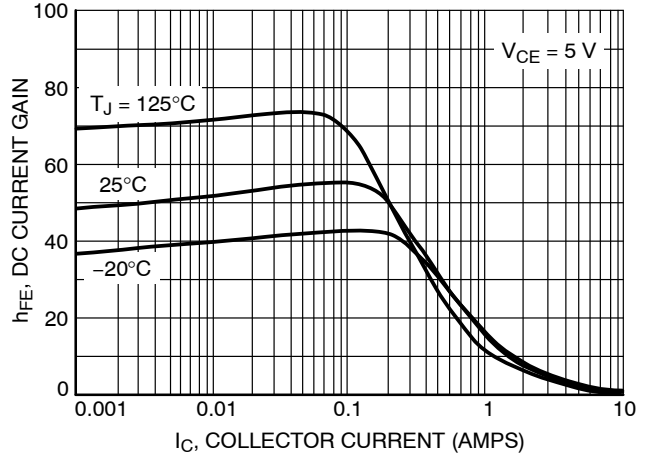


Figure 2. DC Current Gain @ 5 V

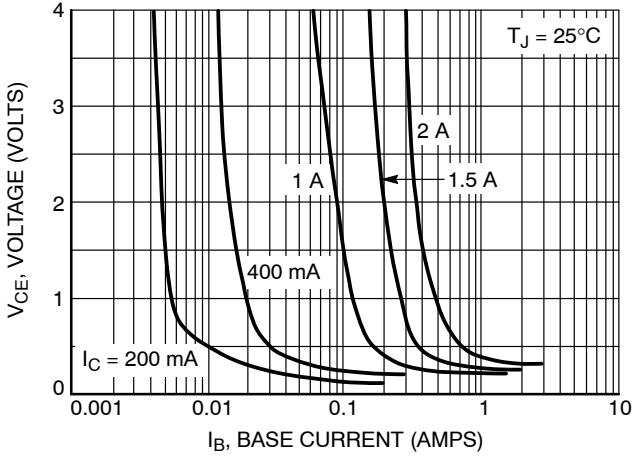


Figure 3. Collector Saturation Region

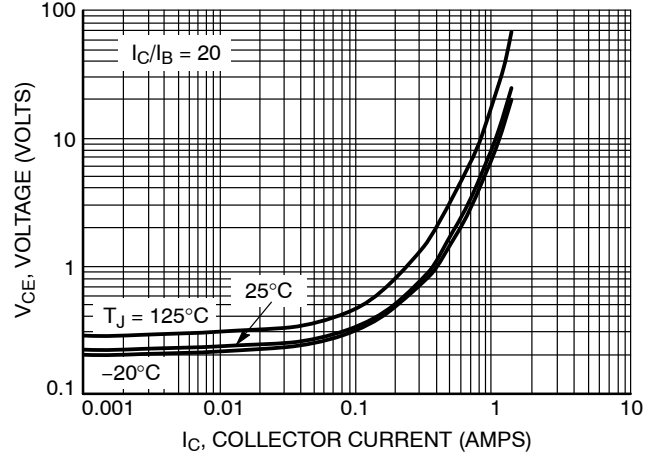


Figure 4. Collector-Emitter Saturation Voltage

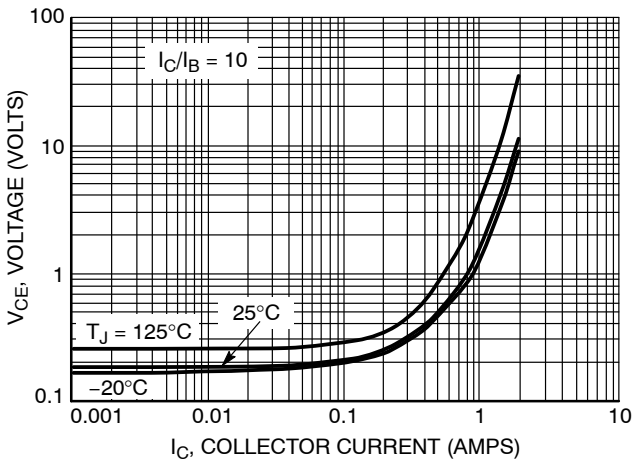


Figure 5. Collector-Emitter Saturation Voltage

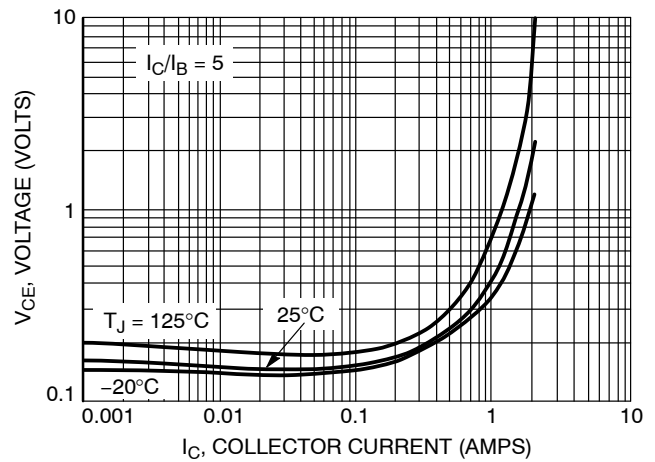


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

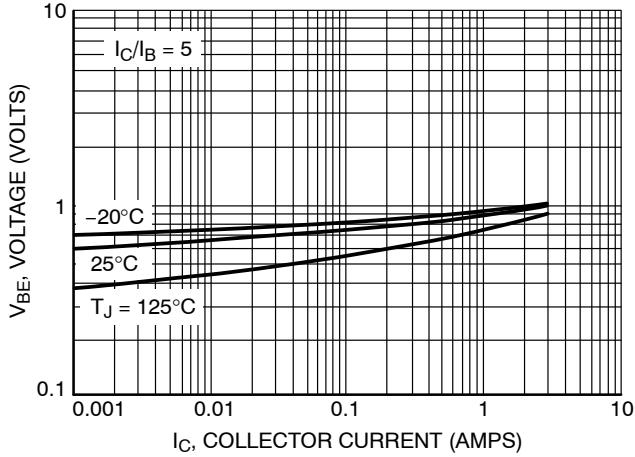


Figure 7. Base-Emitter Saturation Region
 $I_C/I_B = 5$

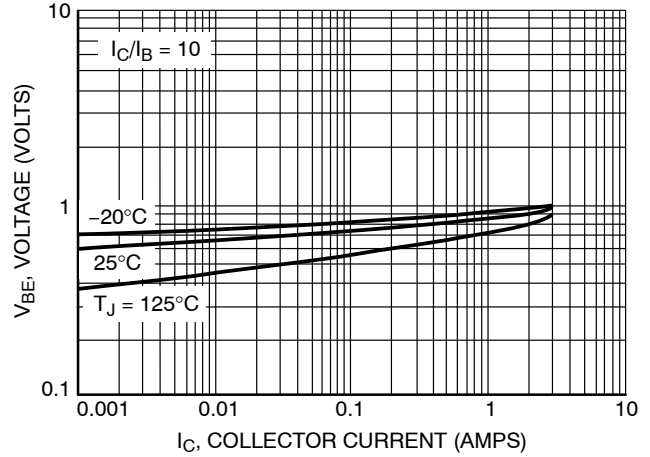


Figure 8. Base-Emitter Saturation Region
 $I_C/I_B = 10$

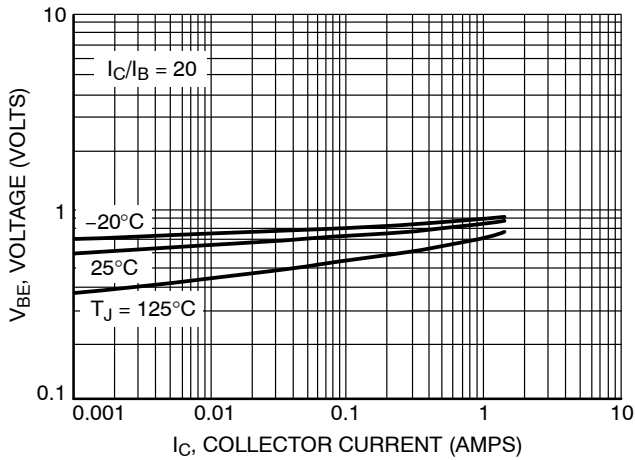


Figure 9. Base-Emitter Saturation Region
 $I_C/I_B = 20$

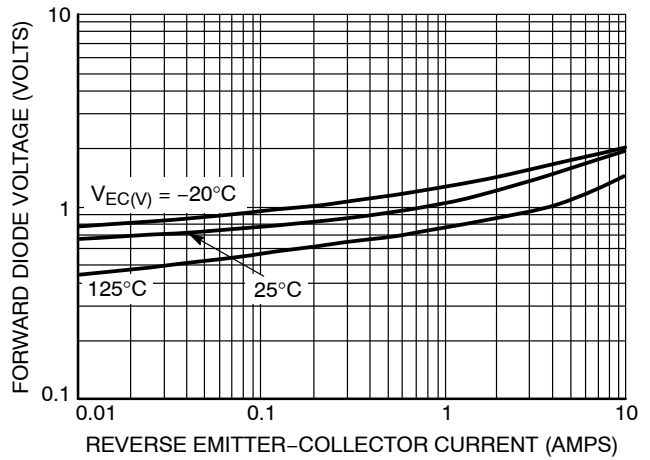


Figure 10. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

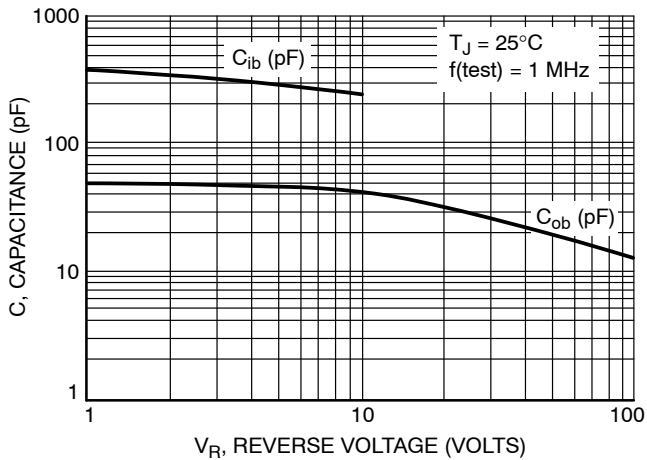


Figure 11. Capacitance

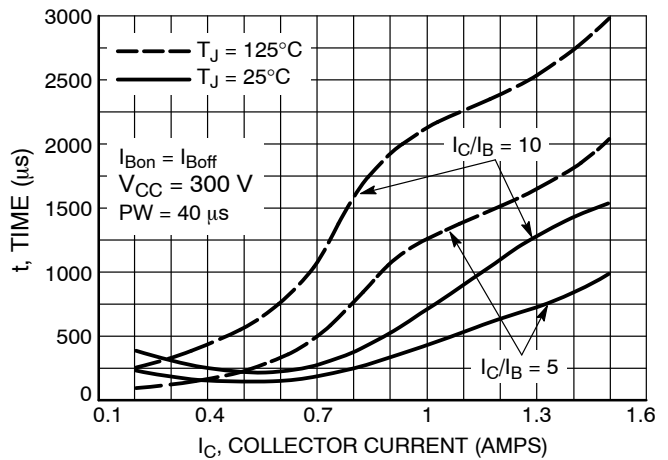


Figure 12. Resistive Switch Time, t_{on}

TYPICAL SWITCHING CHARACTERISTICS

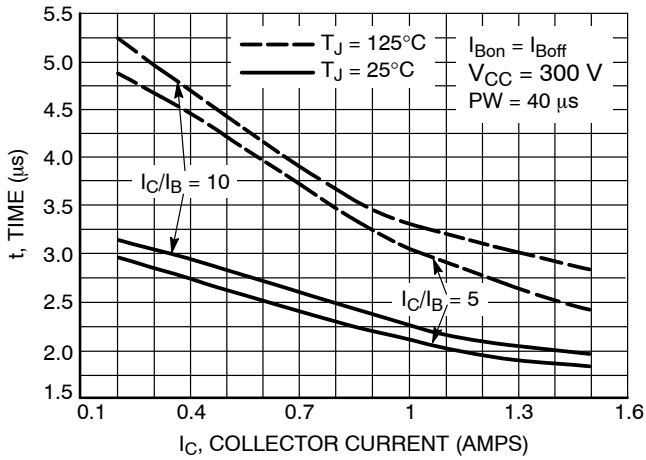


Figure 13. Resistive Switch Time, t_{off}

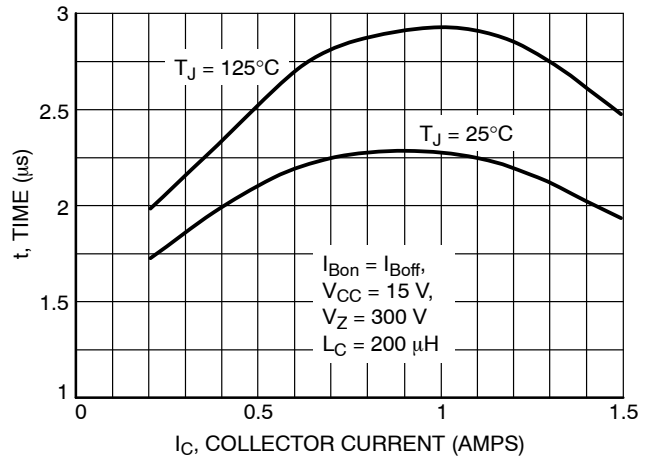


Figure 14. Inductive Storage Time, t_{si} @ $I_C/I_B = 5$

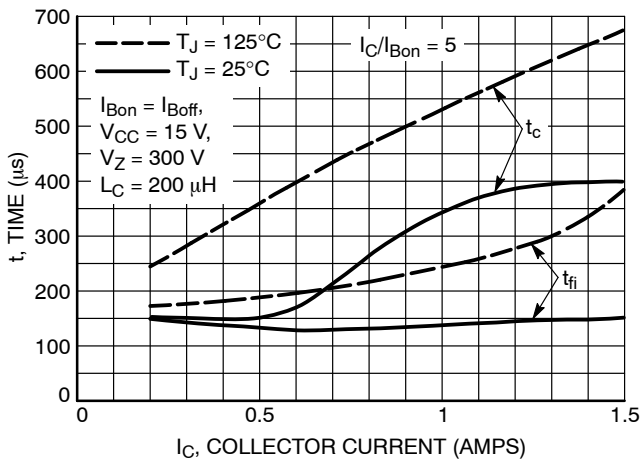


Figure 15. Inductive Switching, t_c & t_{fi} @ $I_C/I_B = 5$

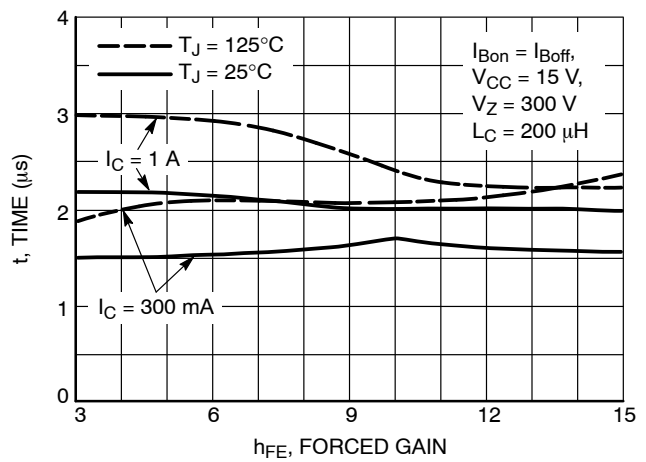


Figure 16. Inductive Storage Time

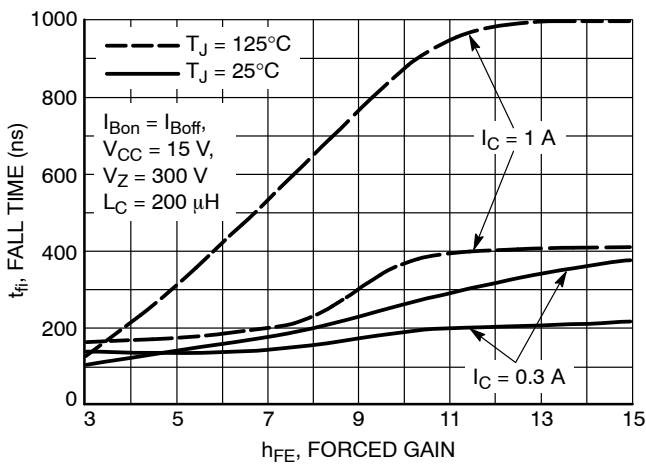


Figure 17. Inductive Fall Time

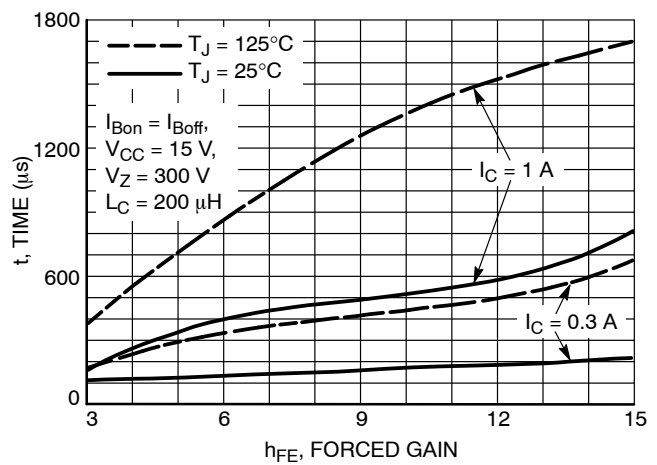


Figure 18. Inductive Cross-Over Time

TYPICAL SWITCHING CHARACTERISTICS

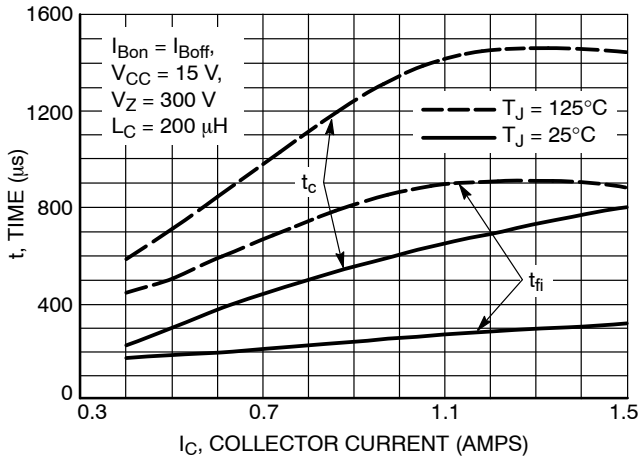


Figure 19. Inductive Switching Time, t_{fi} & T_C @ $G = 10$

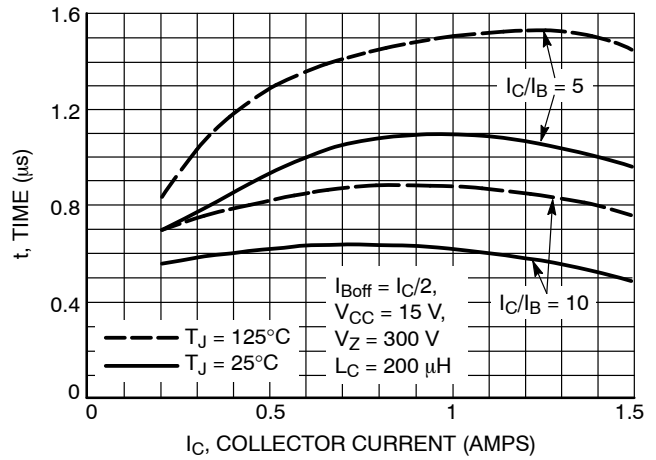


Figure 20. Inductive Switching Time, t_{si}

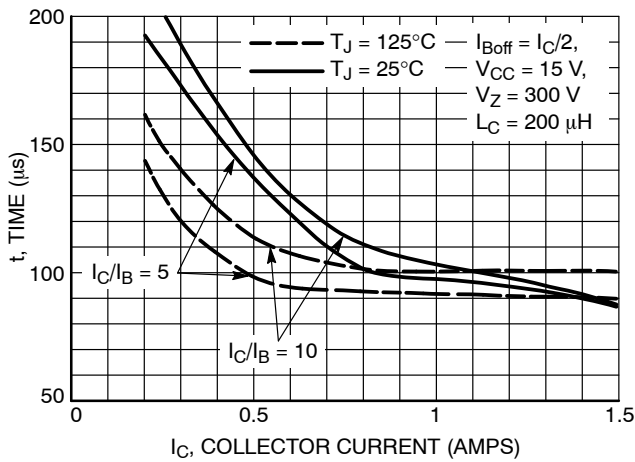


Figure 21. Inductive Storage Time, t_{fi}

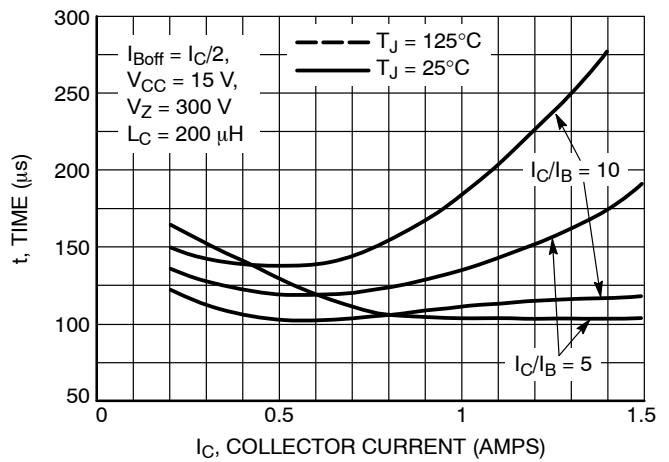


Figure 22. Inductive Storage Time, t_c

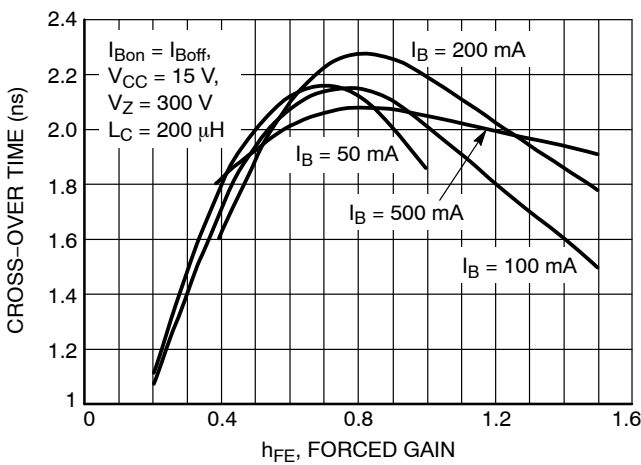


Figure 23. Inductive Storage Time, t_{si}

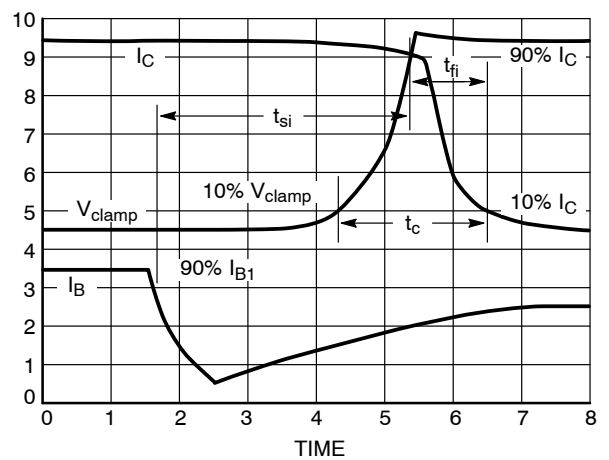


Figure 24. Inductive Switching Measurements

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Figure 25. Inductive Load Switching Drive Circuit

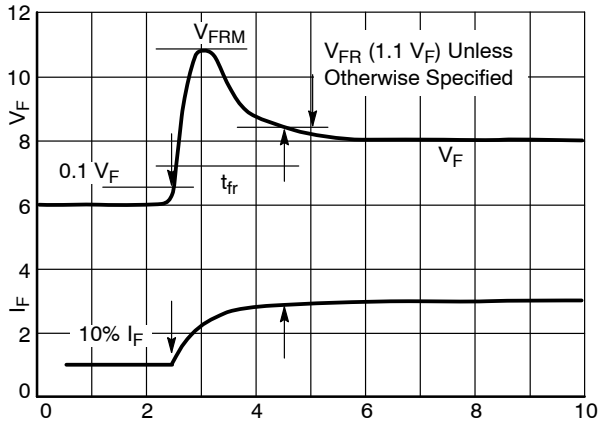
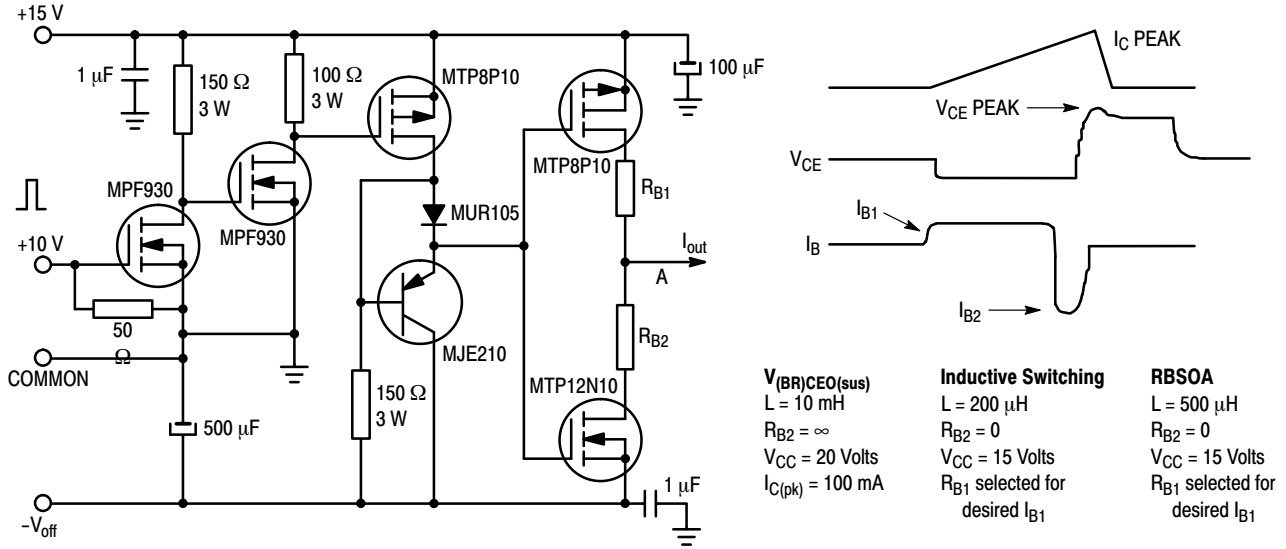


Figure 26. t_{fr} Measurement

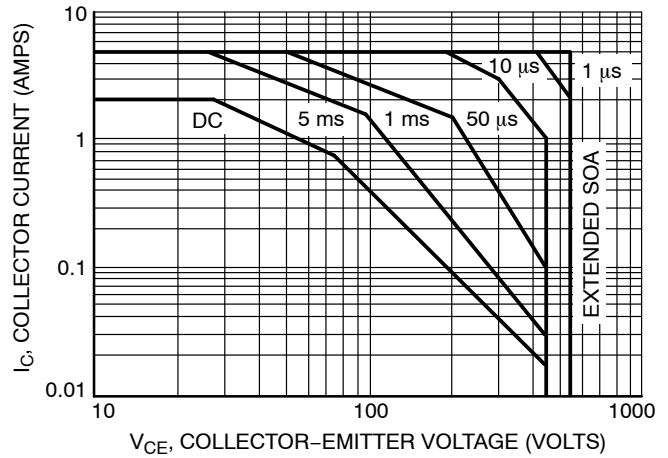


Figure 27. Forward Bias Safe Operating Area

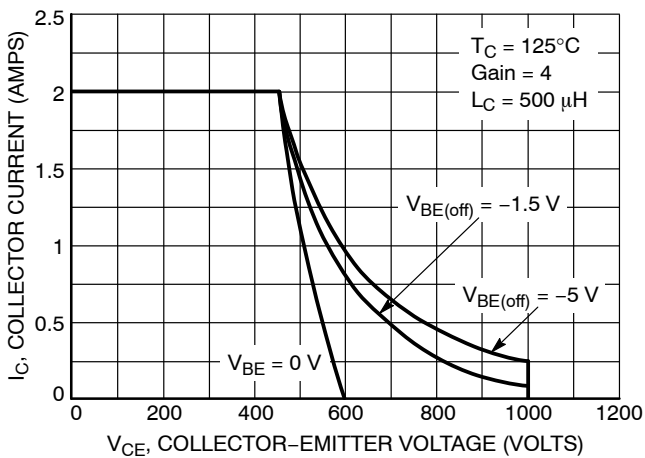


Figure 28. Reverse Bias Safe Operating Area

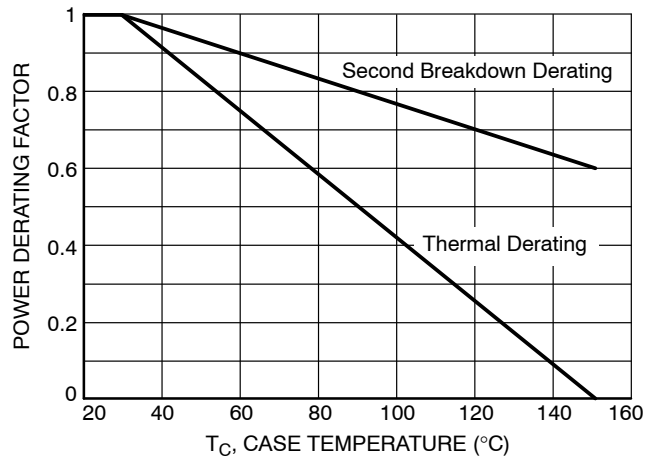


Figure 29. Forward Bias Power Derating

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There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 27 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second Breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on

Figure 27 may be found at any case temperature by using the appropriate curve on Figure 29.

$T_{J(pk)}$ may be calculated from the data in Figure 30. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 28). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

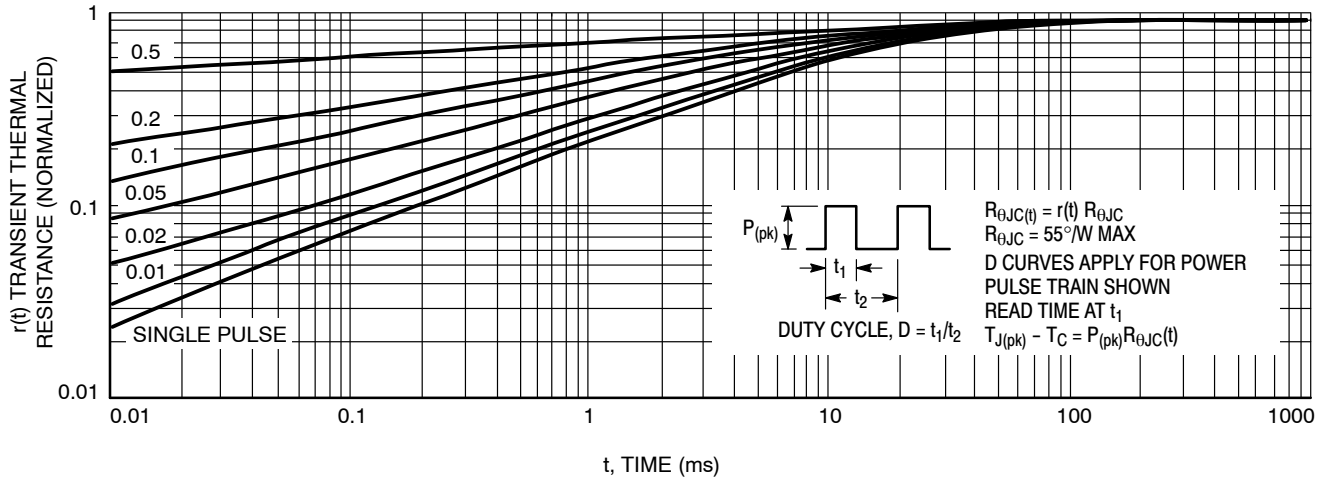


Figure 30. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJD18002D2

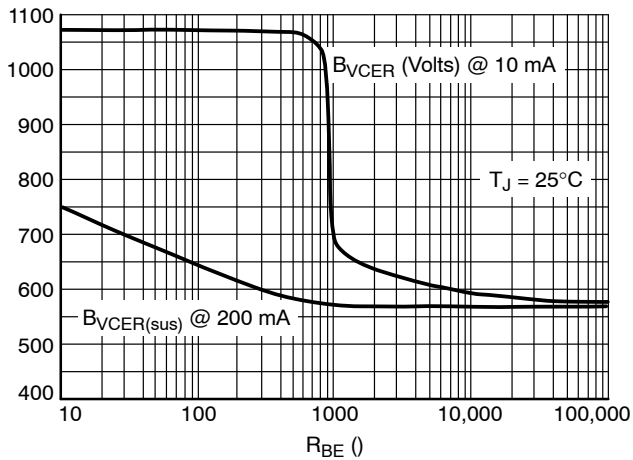


Figure 31. $B_{V_{CE}}$

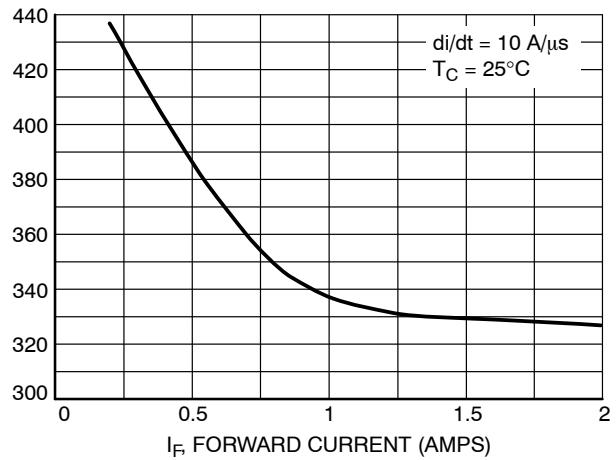


Figure 32. Forward Recovery Time, t_{fr}

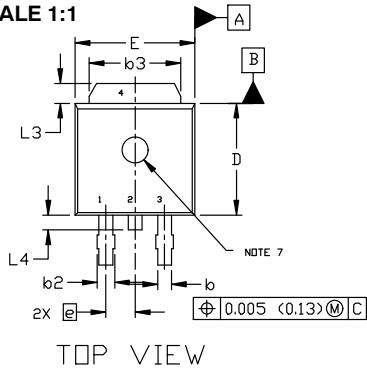
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



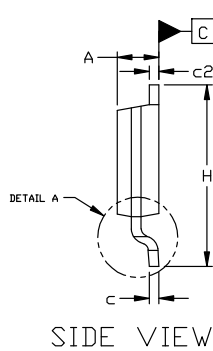
DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

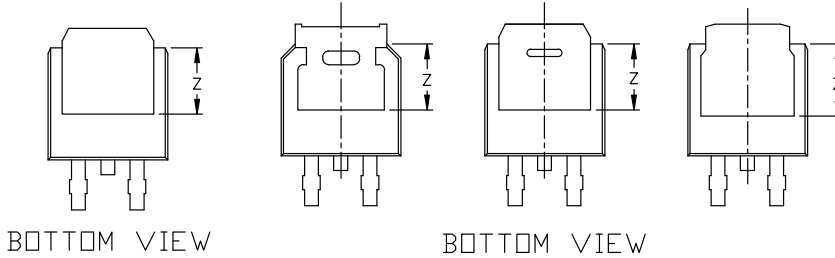


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

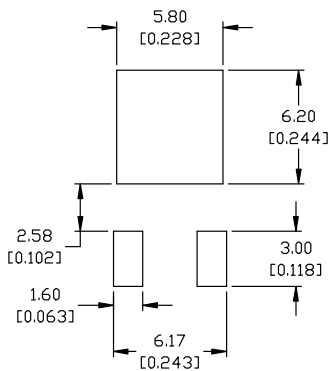
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

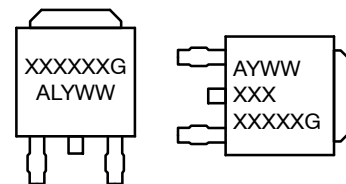


RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> |
| <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE</p> | <p>STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> |

GENERIC MARKING DIAGRAM*



IC

Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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