Complementary Silicon Power Plastic Transistors

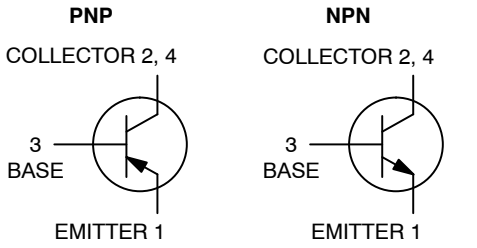
MJE200G (NPN), MJE210G (PNP)

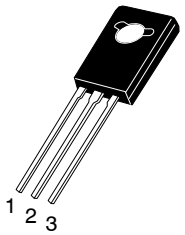
These devices are designed for low voltage, low−power, high−gain audio amplifier applications.

Features

- High DC Current Gain
- Low Collector−Emitter Saturation Voltage
- High Current−Gain − Bandwidth Product
- Annular Construction for Low Leakage
- These Devices are Pb−Free and are RoHS Compliant*

5.0 AMPERES
POWER TRANSISTORS
COMPLEMENTARY SILICON
25 VOLTS, 15 WATTS





TO−225
CASE 77−09
STYLE 1

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CEO}	Collector−Emitter Voltage	40	Vdc
V_{CB}	Collector−Base Voltage	25	Vdc
V_{EB}	Emitter−Base Voltage	8.0	Vdc
I_C	Collector Current − Continuous	5.0	Adc
I_{CM}	Collector Current − Peak	10	Adc
I_B	Base Current	1.0	Adc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	 15 0.12	 W mW/°C
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	 1.5 0.012	 W mW/°C
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−65 to +150	°C

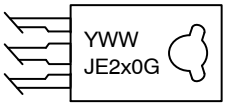
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	8.34	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	83.4	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



Y = Year
WW = Work Week
JE2x0 = Device Code
x = 0 or 1
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet ha **DISCONTINUED**. Please refer to the table on page 5.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit
OFF CHARACTERISTICS				
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 1) (I_C = 10 mAdc, I_B = 0)	 25	 –	Vdc
I_{CBO}	Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	 – –	 100 100	 nAdc μAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	 –	 100	nAdc
ON CHARACTERISTICS				
h_{FE}	DC Current Gain (Note 1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	 70 45 10	 – 180 –	–
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (Note 1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	 – – –	 0.3 0.75 1.8	Vdc
$V_{BE(sat)}$	Base−Emitter Saturation Voltage (Note 1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	 –	 2.5	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (Note 1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	 –	 1.6	Vdc
DYNAMIC CHARACTERISTICS				
f_T	Current−Gain − Bandwidth Product (Note 2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	 65	 –	MHz
C_{ob}	Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200G MJE210G	 – –	 80 120	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

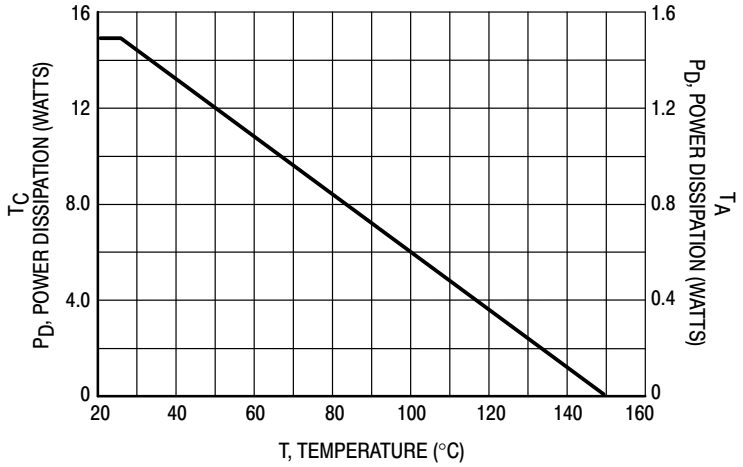

Figure 1. Power Derating

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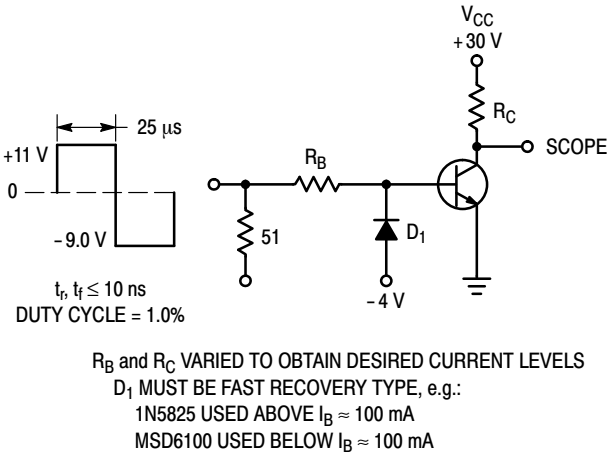

Figure 2. Switching Time Test Circuit

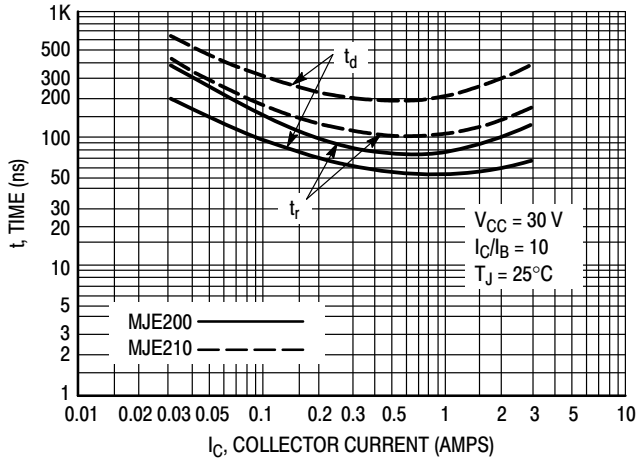

Figure 3. Turn−On Time

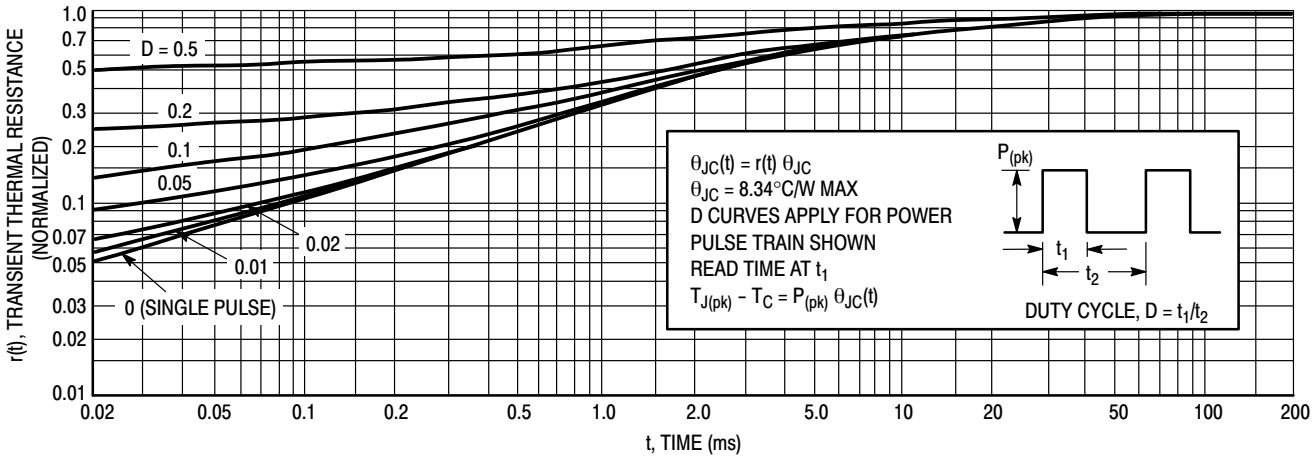

Figure 4. Thermal Response

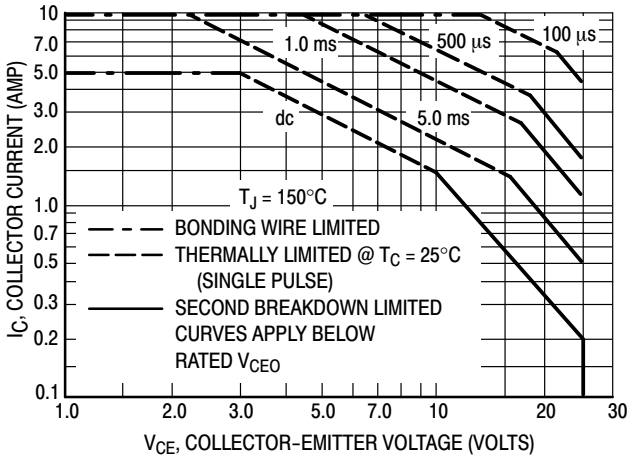

Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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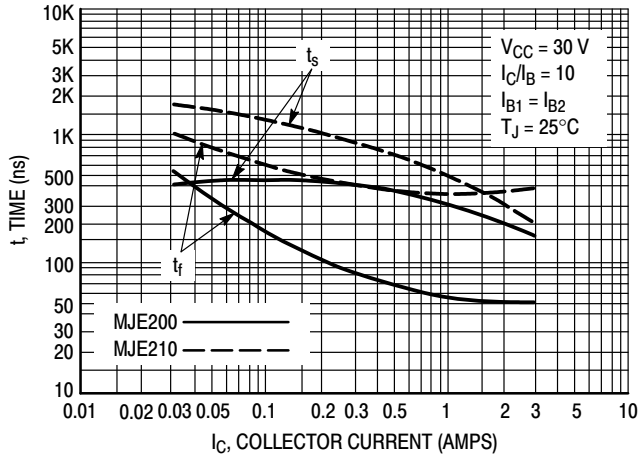

Figure 6. Turn−Off Time

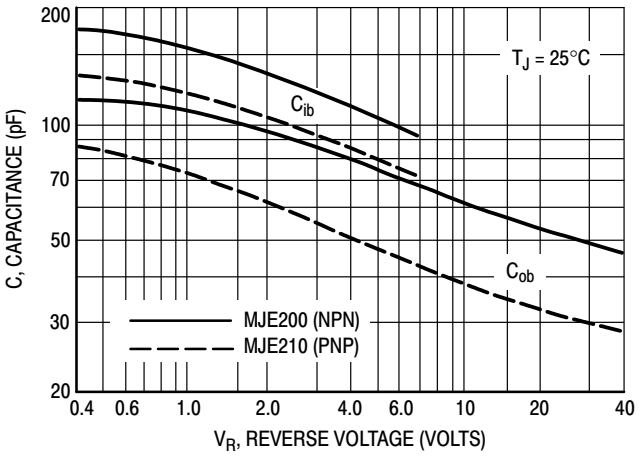

Figure 7. Capacitance

NPN
MJE200

PNP
MJE210

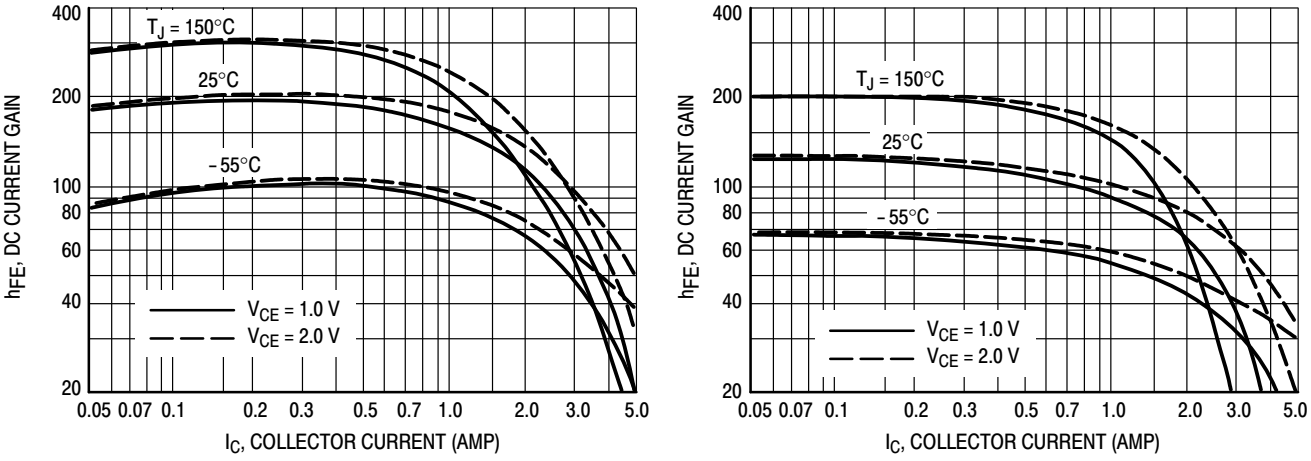

Figure 8. DC Current Gain

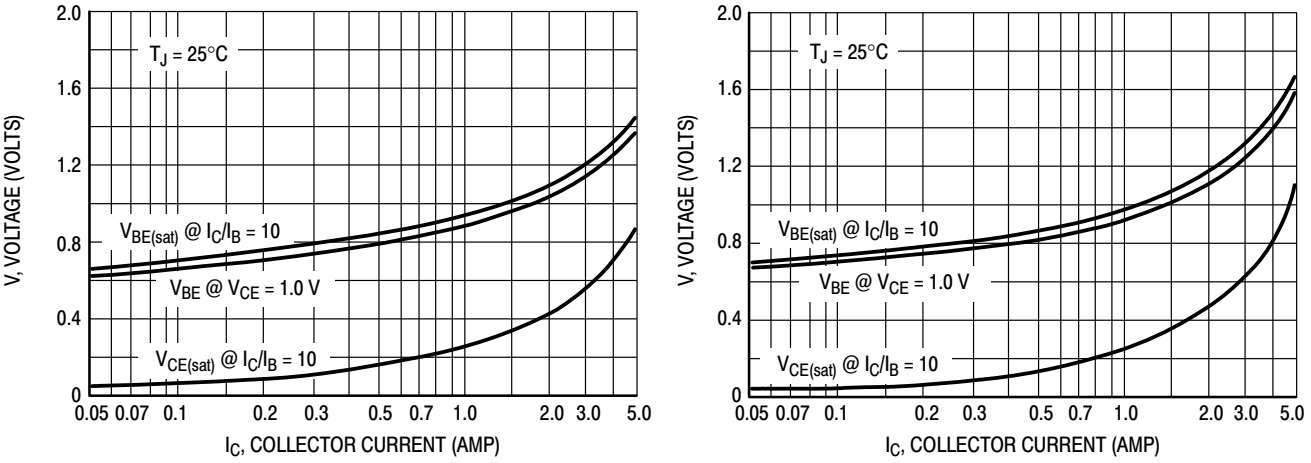

Figure 9. “On” Voltage

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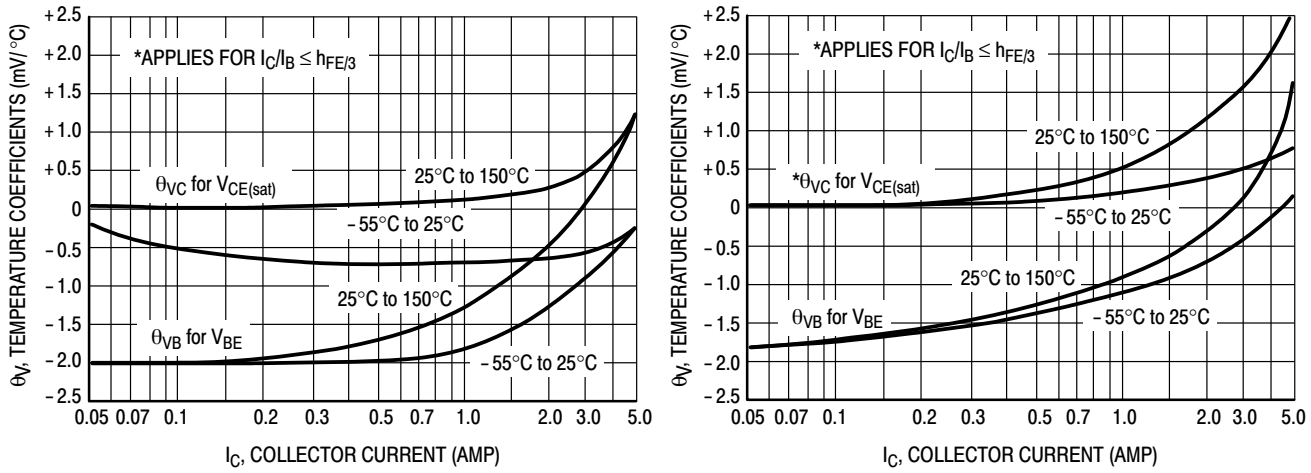

Figure 10. Temperature Coefficients

DEVICE ORDERING INFORMATION

Device	Package	Shipping
MJE200G	TO−225 (Pb−Free)	500 Bulk / Box

DISCONTINUED (Note 3)

MJE210G	TO−225 (Pb−Free)	500 Bulk / Box
MJE210TG	TO−225 (Pb−Free)	500 Bulk / Box

3. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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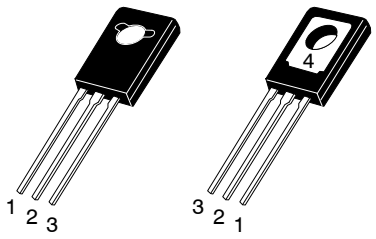
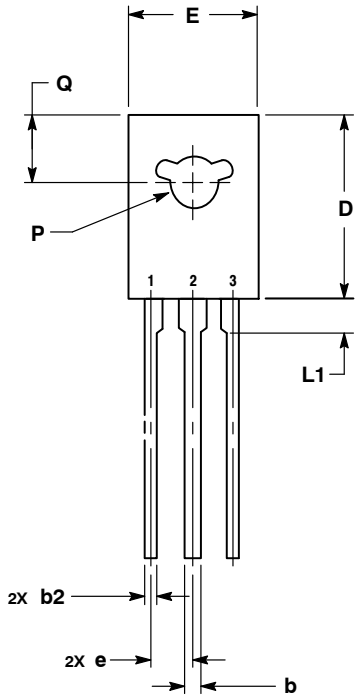
TO−225
CASE 77−09
ISSUE AD

DATE 25 MAR 2015

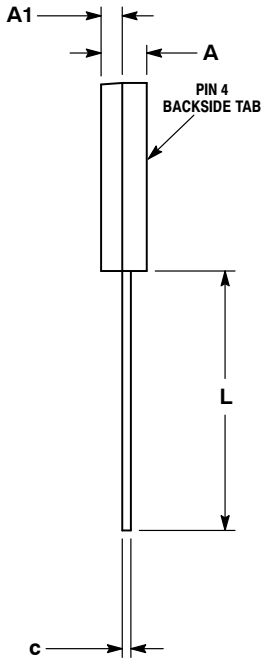


FRONT VIEW **BACK VIEW**

SCALE 1:1



FRONT VIEW

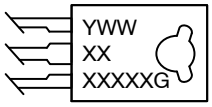


SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

GENERIC MARKING DIAGRAM*



Y = Year
WW = Work Week
XXXXX = Device Code
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE

STYLE 2:
PIN 1. CATHODE
2., 4. ANODE
3. GATE

STYLE 3:
PIN 1. BASE
2., 4. COLLECTOR
3. EMITTER

STYLE 4:
PIN 1. ANODE 1
2., 4. ANODE 2
3. GATE

STYLE 5:
PIN 1. MT 1
2., 4. MT 2
3. GATE

STYLE 6:
PIN 1. CATHODE
2., 4. GATE
3. ANODE

STYLE 7:
PIN 1. MT 1
2., 4. GATE
3. MT 2

STYLE 8:
PIN 1. SOURCE
2., 4. GATE
3. DRAIN

STYLE 9:
PIN 1. GATE
2., 4. DRAIN
3. SOURCE

STYLE 10:
PIN 1. SOURCE
2., 4. DRAIN
3. GATE

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