# onsemi

# Inverting Octal 3-STATE Buffer, Octal 3-STATE Buffer

# MM74HC540, MM74HC541

# **General Description**

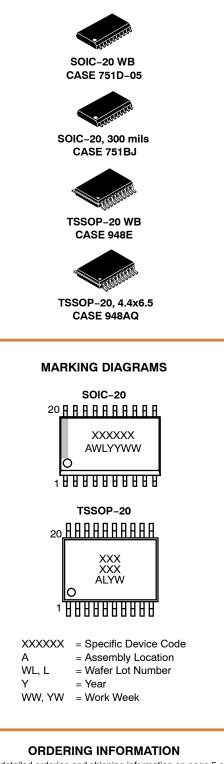
The MM74HC540 and MM74HC541 3–STATE buffers utilize advanced silicon–gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS–TTL equivalent inputs.

The MM74HC540 is an inverting buffer and the MM74HC541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input NOR such that if either  $\overline{G1}$  or  $\overline{G2}$  are HIGH, all eight outputs are in the high-impedance state.

In order to enhance PC board layout, the MM74HC540 and MM74HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

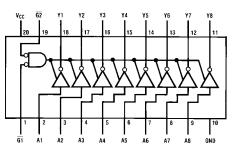
# Features

- Typical Propagation Delay: 12 ns
- 3-STATE Outputs for Connection to System Buses
- Wide Power Supply Range: 2–6 V
- Low Quiescent Current: 160 µA Maximum (74HC Series)
- Output Current: 6 mA
- These are Pb-Free Devices

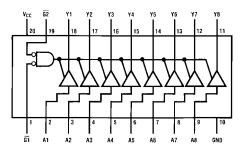


See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.



MM74HC540 (Top View)



MM74HC541 (Top View)

Figure 1. Connection Diagrams

(Pin Assignments for SOIC and TSSOP)

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage	–0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage	–0.5 to V <sub>CC</sub> +0.5	V
I <sub>CD</sub>	Clamp Diode Current	±20	mA
I <sub>OUT</sub>	DC Output Current, per pin	±35	mA
I <sub>CC</sub>	DC V <sub>CC</sub> or GND Current, per pin	±70	mA
T <sub>STG</sub>	Storage Temperature Range	–65 to +150	°C
P <sub>D</sub>	Power Dissipation SOIC TSSOP	1302 833	mW
ΤL	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Unless otherwise specified all voltages are referenced to ground.

# **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub>	Supply Voltage		2	6	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input or Output Voltage		0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range		-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Times	V <sub>CC</sub> = 2.0 V	-	1000	ns
		V <sub>CC</sub> = 4.5 V	-	500	ns
		V <sub>CC</sub> = 6.0 V	-	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS (Note 2)

				T <sub>A</sub> =	25°C	T <sub>A</sub> = −40 to 85°C	T <sub>A</sub> = −55 to 125°C	
Symbol	Parameter	Conditions	V <sub>cc</sub>	Тур		Guaranteed L	.imits	Unit
V <sub>IH</sub>	Minimum HIGH Level Input Voltage		2.0 V 4.5 V 6.0 V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V <sub>IL</sub>	Maximum LOW Level Input Voltage		2.0 V 4.5 V 6.0 V		0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V V V
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	$ \begin{aligned} V_{IN} &= V_{IH} \text{ or } V_{IL} \\  I_{OUT}  &\leq 20 \ \mu A \end{aligned} $	2.0 V 4.5 V 6.0 V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
		$\label{eq:VIN} \begin{split} V_{IN} &= V_{IH} \text{ or } V_{IL} \\ \left  I_{OUT} \right  &\leq 6.0 \text{ mA} \\ \left  I_{OUT} \right  &\leq 7.8 \text{ mA} \end{split}$	4.5 V 6.0 V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V <sub>OL</sub>	Maximum LOW Level Output Voltage		2.0 V 4.5 V 6.0 V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
		$\label{eq:VIN} \begin{split} V_{IN} &= V_{IH} \text{ or } V_{IL} \\ \left  I_{OUT} \right  &\leq 6.0 \text{ mA} \\ \left  I_{OUT} \right  &\leq 7.8 \text{ mA} \end{split}$	4.5 V 6.0 V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I <sub>IN</sub>	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0 V		±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $\overline{G} = V_{IH}$ $V_{OUT} = V_{CC} \text{ or } GND$	6.0 V		±0.5	±5	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0 V		8.0	80	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V  $\pm$ 10% the worst case output voltages (V<sub>OH</sub>, and V<sub>OL</sub>) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5 V and 4.5 V respectively. (The V<sub>IH</sub> value at 5.5 V is 3.85 V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

# AC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 5 \text{ V}, \text{ } \text{T}_{\text{A}} = 25^{\circ}\text{C}, \text{ } \text{t}_{\text{r}} = \text{t}_{\text{f}} = 6 \text{ ns})$ 

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay (540)	C <sub>L</sub> = 45 pF	12	18	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay (541)	C <sub>L</sub> = 45 pF	14	20	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Output Enable Time	$R_L = 1 k\Omega$ $C_L = 45 pF$	17	28	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Output Disable Time	$R_L = 1 kΩ$ $C_L = 5 pF$	15	25	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### **AC ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 2.0 V to 6.0. V, C<sub>L</sub> = 50 pF,  $t_r = t_f = 6$  ns, unless otherwise specified)

				T <sub>A</sub> =	25°C	T <sub>A</sub> = −40 to 85°C	T <sub>A</sub> = −55 to 125°C	
Symbol	Parameter	Conditions	V <sub>cc</sub>	Тур		Guaranteed L	imits	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay (540)	C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	2.0 V 2.0 V	55 83	100 150	126 190	149 224	ns ns
		$C_{L} = 50 \text{ pF}$ $C_{L} = 150 \text{ pF}$	4.5 V 4.5 V	12 22	20 30	25 38	30 45	ns ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	6.0 V 6.0 V	11 18	17 26	21 32	25 38	ns ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay (541)	C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	2.0 V 2.0 V	58 83	115 165	145 208	171 246	ns ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	4.5 V 4.5 V	14 17	23 33	29 42	34 49	ns ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	6.0 V 6.0 V	11 14	20 28	25 35	29 42	ns ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Output Enable Time	$\begin{aligned} R_L &= 1 \ k\Omega \\ C_L &= 50 \ pF \\ C_L &= 150 \ pF \end{aligned}$	2.0 V 4.5 V	75 100	150 200	189 252	224 298	ns ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	4.5 V 4.5 V	15 30	30 40	38 50	45 60	ns ns
		C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	6.0 V 6.0 V	13 17	26 34	32 43	38 51	ns ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Output Disable Time	$R_L = 1 k\Omega$ $C_L = 50 pF$	2.0 V 4.5 V 6.0 V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise and Fall Time	C <sub>L</sub> = 50 pF	2.0 V 4.5 V 6.0 V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
C <sub>PD</sub>	Power Dissipation Capacitance (Note 3)	<del>G</del> = V <sub>IH</sub> G = V <sub>IL</sub>		10 50				pF
C <sub>IN</sub>	Maximum Input Capacitance			5	10	10	10	pF
C <sub>OUT</sub>	Maximum Output Capacitance			15	20	20	20	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
C<sub>PD</sub> determines the no load dynamic power consumption, P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>, and the no load dynamic current consumption, I<sub>S</sub> = C<sub>PD</sub> V<sub>CC</sub> f + I<sub>CC</sub>.

## **ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
MM74HC540WM	HC540A	SOIC-20 WB	38 Units / Tube
MM74HC540WMX	HC540A	(Pb-Free and Halide Free)	1000 / Tape & Reel
MM74HC540MTCX	HC 540A	TSSOP-20 WB (Pb-Free)	2500 / Tape & Reel
MM74HC541WM	HC541A	SOIC-20 WB (Pb-Free and Halide Free)	38 Units / Tube
MM74HC541WMX	HC541A	SOIC–20, 300 mils (Pb–Free and Halide Free)	1000 / Tape & Reel
MM74HC541MTC	HC 541A	TSSOP-20 WB (Pb-Free)	75 Units / Tube
MM74HC541MTCX	HC 541A	TSSOP20, 4.4 × 6.5 (Pb-Free)	2500 / Tape & Reel

#### **DISCONTINUED** (Note 4)

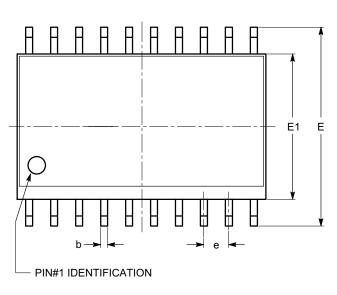
MM74HC540MTC	HC 540A	TSSOP-20 WB (Pb-Free)	75 Units / Tube
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.
4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on <u>www.onsemi.com</u>.

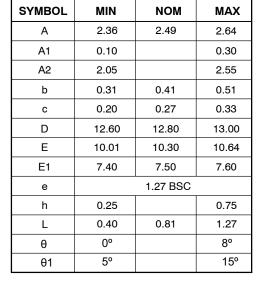


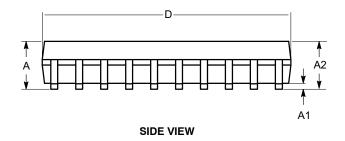
SOIC-20, 300 mils CASE 751BJ ISSUE O

DATE 19 DEC 2008



TOP VIEW

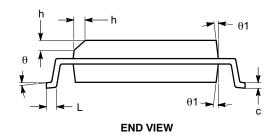




#### Notes:

(1) All dimensions are in millimeters. Angles in degrees.

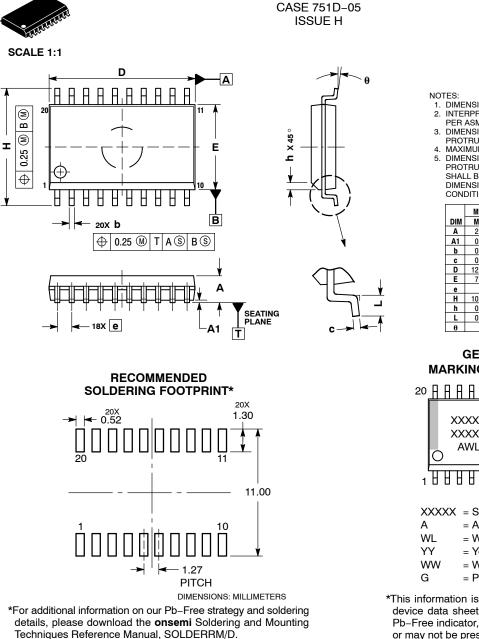
(2) Complies with JEDEC MS-013.



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SOIC-20 WB

DATE 22 APR 2015

- NOTES:
   DIMENSIONS ARE IN MILLIMETERS.
   INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
   DIMENSIONS D AND E DO NOT INCLUDE MOLD
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		
DIM	MIN	MAX	
Α	2.35	2.65	
A1	0.10	0.25	
b	0.35	0.49	
C	0.23	0.32	
D	12.65	12.95	
E	7.40	7.60	
е	1.27	BSC	
н	10.05	10.55	
h	0.25	0.75	
L	0.50	0.90	
θ	0 °	7 °	

GENERIC **MARKING DIAGRAM\*** 

ХХХХХХХХХ ХХХХХХХХХ AWLYYWWG О
XXXXX = Specific Device Code A = Assembly Location WL = Wafer Lot YY = Year WW = Work Week

= Pb-Free Package

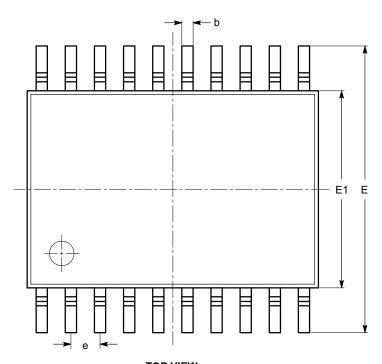
\*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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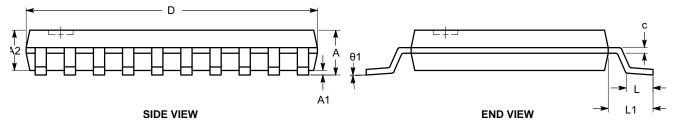
TSSOP20, 4.4x6.5 CASE 948AQ ISSUE A

DATE 19 MAR 2009



SYMBOL	MIN	NOM	MAX
STWBOL			
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
С	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
е		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°





#### Notes:

All dimensions are in millimeters. Angles in degrees.
 Complies with JEDEC MO-153.

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