MMBTA05L, MMBTA06L

Driver Transistors

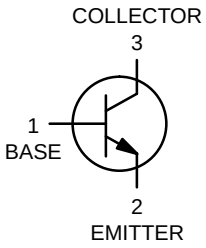
NPN Silicon

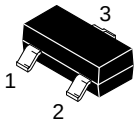
ON Semiconductor®

www.onsemi.com

Features

- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant





SOT−23
CASE 318
STYLE 6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage MMBTA05L MMBTA06L	V_{CEO}	 60 80	Vdc
Collector−Base Voltage MMBTA05L MMBTA06L	V_{CBO}	 60 80	Vdc
Emitter−Base Voltage	V_{EBO}	4.0	Vdc
Collector Current − Continuous	I_C	500	mAdc
Electrostatic Discharge	ESD	HBM Class 3B MM Class C CDM Class IV	

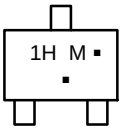
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

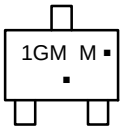
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

MARKING DIAGRAMS



MMBTA05LT1



MMBTA06LT1,
SMMBTA06L

1H, 1GM = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

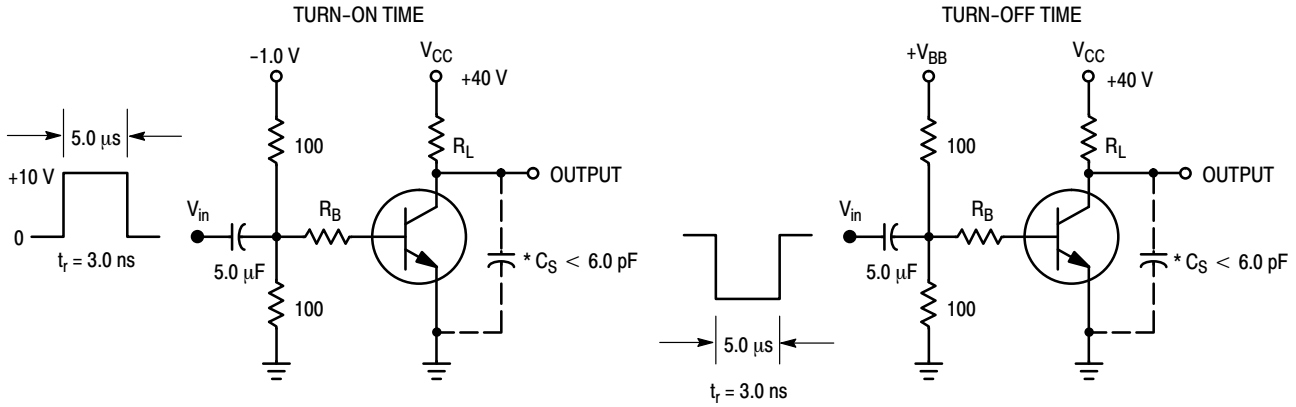
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 1.0 mAdc, I_B = 0)	MMBTA05L MMBTA06L	$V_{(BR)CEO}$	 60 80	 − −	Vdc
Emitter−Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	4.0	−	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)		I_{CES}	−	0.1	μAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 MMBTA05L MMBTA06L	I_{CBO}	 − −	 0.1 0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	 100 100	 − −	−
Collector−Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	−	0.25	Vdc
Base−Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	−	1.2	Vdc
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 4) (I_C = 10 mA, V_{CE} = 2.0 V, f = 100 MHz)		f_T	100	−	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



*Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

Figure 1. Switching Time Test Circuits

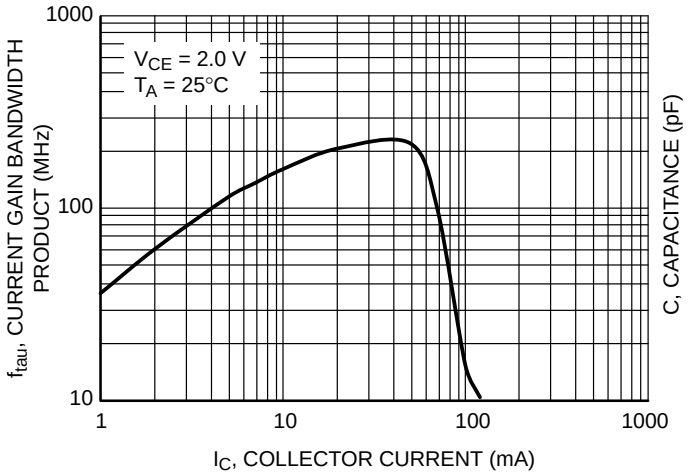


Figure 2. Current Gain Bandwidth Product vs. Collector Current

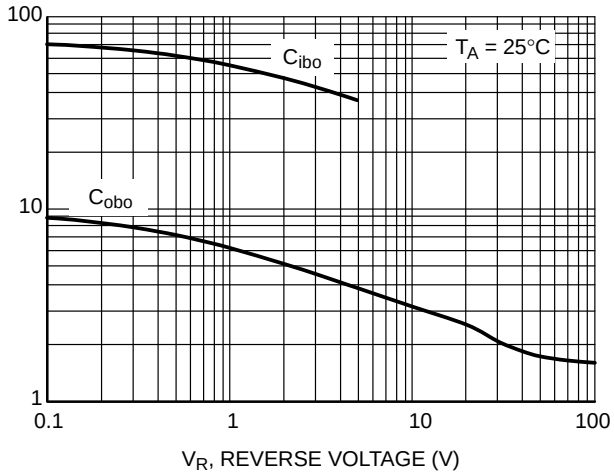


Figure 3. Capacitance

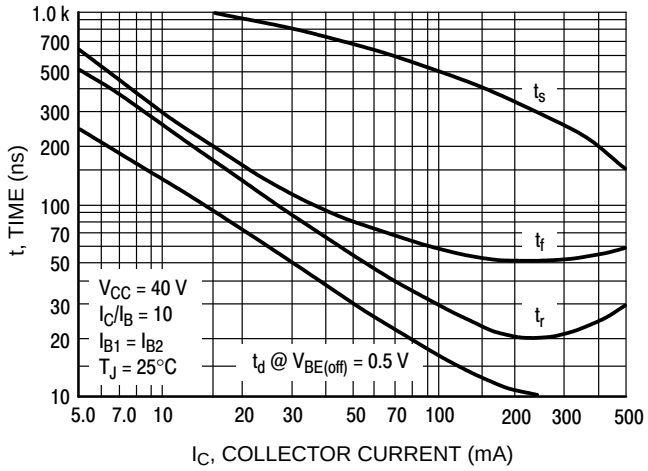


Figure 4. Switching Time

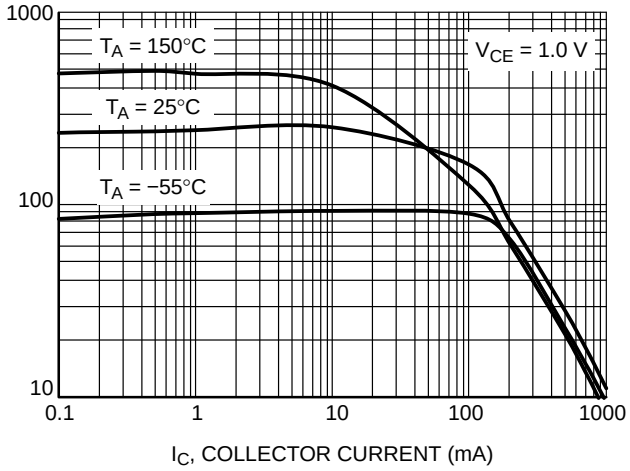


Figure 5. DC Current Gain vs. Collector Current

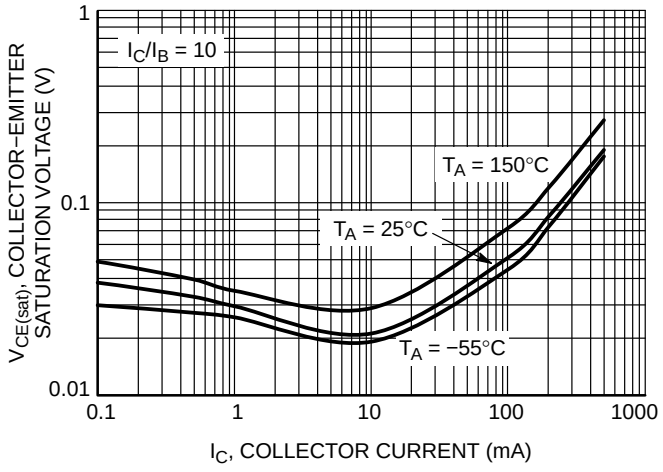


Figure 6. Collector Emitter Saturation Voltage vs. Collector Current

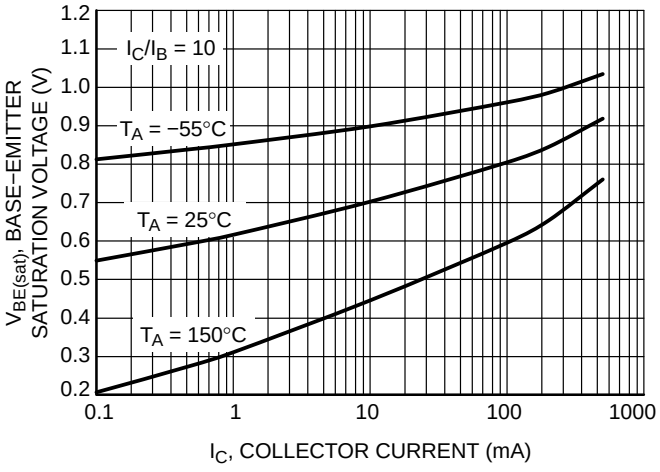


Figure 7. Base Emitter Saturation Voltage vs. Collector Current

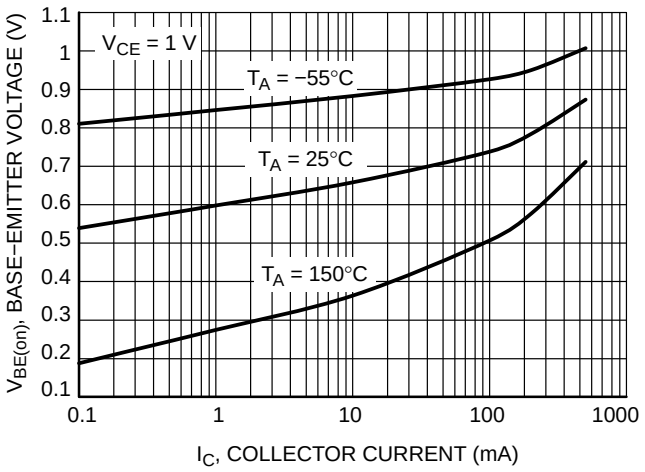


Figure 8. Base Emitter Turn−ON Voltage vs. Collector Current

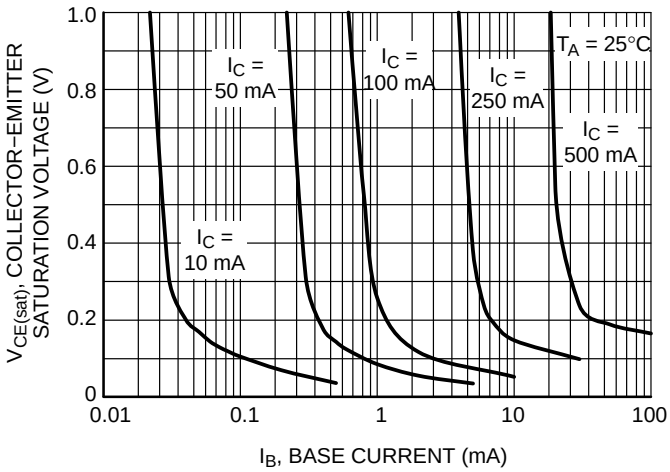


Figure 9. Saturation Region

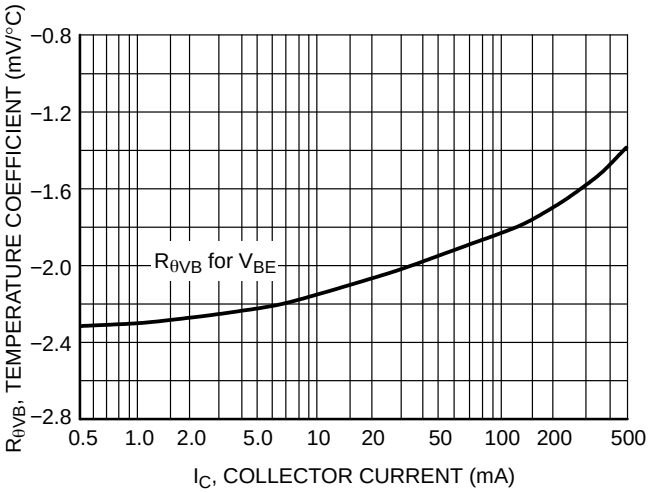


Figure 10. Base−Emitter Temperature Coefficient

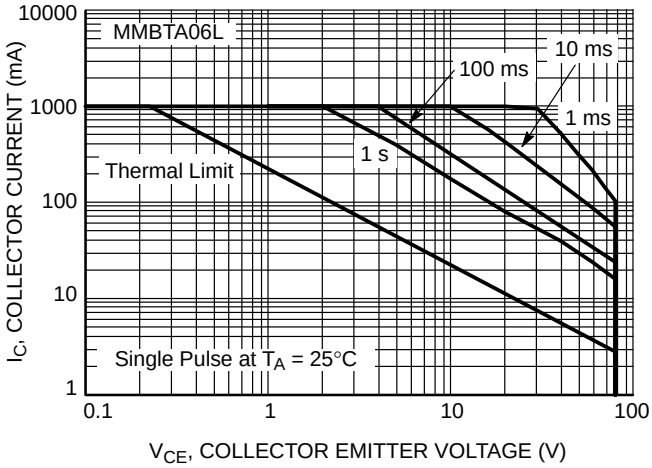


Figure 11. Safe Operating Area

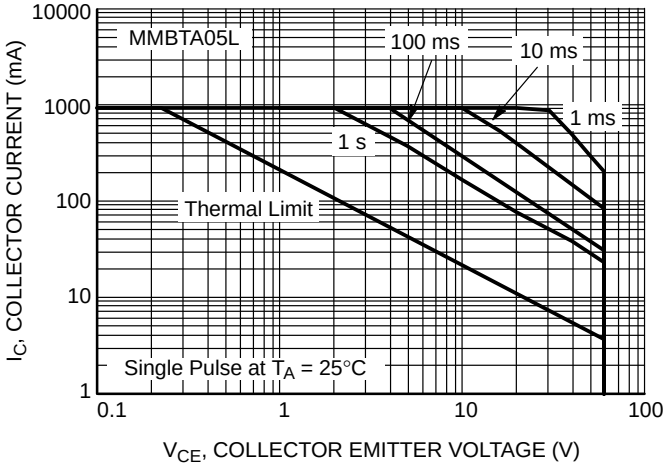


Figure 12. Safe Operating Area

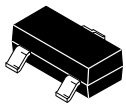
ORDERING INFORMATION

Device	Package	Shipping†
MMBTA05LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
NSVMMBTA05LT1G*	SOT−23 (Pb−Free)	3,000 / Tape & Reel
MMBTA05LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel
MMBTA06LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel
SMMBTA06LT1G*	SOT−23 (Pb−Free)	3,000 / Tape & Reel
MMBTA06LT3G	SOT−23 (Pb−Free)	10,000 / Tape & Reel
SMMBTA06LT3G*	SOT−23 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

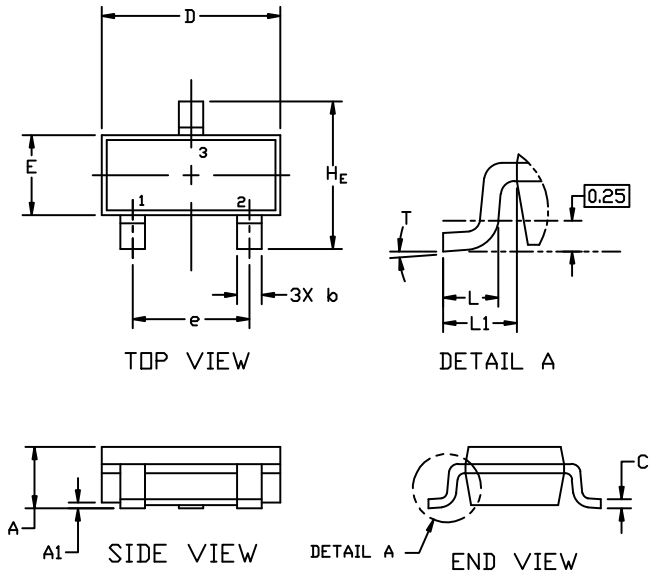
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

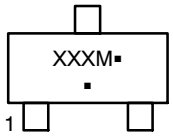


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

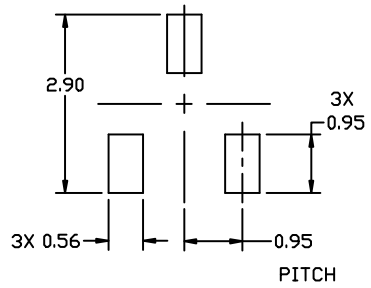
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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