

# 2.5 V / 3.3 V 1:2 Differential LVPECL Clock / Data Fanout Buffer

## Multi-Level Inputs with Internal Termination

### NB6L611

#### Description

The NB6L611 is a differential 1:2 clock or data fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VTD pins and will accept LVPECL, CML, LVDS, LVCMOS or LVTTTL logic levels.

The V<sub>REFAC</sub> reference output can be used to rebias capacitor-coupled differential or single-ended input signals. When used, decouple V<sub>REFAC</sub> with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When used, decouple V<sub>REFAC</sub> with a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V<sub>REFAC</sub> output should be left open.

The device is housed in a small 3x3 mm 16 pin QFN package.

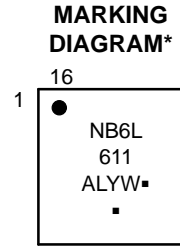
The NB6L611 is a member of the ECLinPS MAX™ family of high performance clock and data management products.

#### Features

- Input Clock Frequency > 4.0 GHz
- 280 ps Typical Propagation Delay
- 100 ps Typical Rise and Fall Times
- 0.5 ps maximum RMS Clock Jitter
- Differential LVPECL Outputs, 780 mV Amplitude, typical
- LVPECL Operating Range: V<sub>CC</sub> = 2.375 V to 3.63 V with V<sub>EE</sub> = 0 V
- NECL Operating Range: V<sub>CC</sub> = 0 V with V<sub>EE</sub> = -2.375 V to -3.63 V
- Internal Input Termination Resistors, 50 Ω
- V<sub>REFAC</sub> Reference Output Voltage
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



QFN-16  
MN SUFFIX  
CASE 485G



- A = Assembly Location
  - L = Wafer Lot
  - Y = Year
  - W = Work Week
  - = Pb-Free Package
- (Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

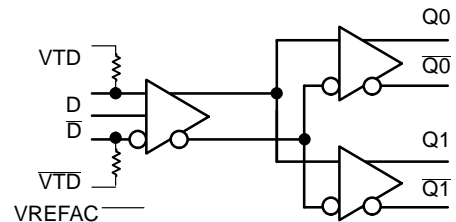


Figure 1. Simplified Logic Diagram

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

# NB6L611

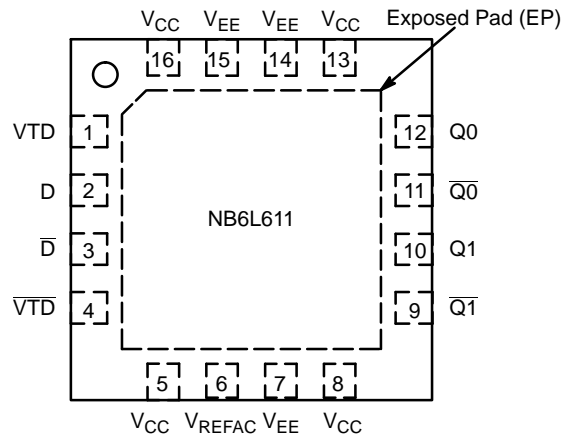


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTD	-	Internal 50 $\Omega$ Termination Pin for D input.
2	D	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input. Note1. Internal 50 $\Omega$ Resistor to Termination Pin, VTD.
3	$\bar{D}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input. Note 1. Internal 50 $\Omega$ Resistor to Termination Pin, $\bar{VTD}$ .
4	$\bar{VTD}$	-	Internal 50 $\Omega$ Termination Pin for $\bar{D}$ input.
5	VCC	-	Positive Supply Voltage
6	VREFAC		Output Reference Voltage for direct or capacitor coupled inputs
7	VEE	-	Negative Supply Voltage
8	VCC	-	Positive Supply Voltage
9	$\bar{Q1}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to VCC - 2.0 V.
10	Q1	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to VCC - 2.0 V.
11	$\bar{Q0}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to VCC - 2.0 V.
12	Q0	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to VCC - 2.0 V.
13	VCC	-	Positive Supply Voltage
14	VEE	-	Negative Supply Voltage
15	VEE	-	Negative Supply Voltage
16	VCC	-	Positive Supply Voltage
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to VEE on the PC board.

1. In the differential configuration when the input termination pins (VTD,  $\bar{VTD}$ ) are connected to a common termination voltage or left open, and if no signal is applied on D/ $\bar{D}$  input, then, the device will be susceptible to self-oscillation.
2. All VCC and VEE pins must be externally connected to a power supply for proper operation.

# NB6L611

**Table 2. ATTRIBUTES**

Characteristics	Value
ESD Protection Human Body Model Machine Model	> 2 kV > 200V
Moisture Sensitivity 16-QFN	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	V <sub>EE</sub> = 0 V		4.0	V
V <sub>EE</sub>	Negative Power Supply	V <sub>CC</sub> = 0 V		-4.0	V
V <sub>IO</sub>	Positive Input/Output Voltage Negative Input/Output Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	-0.5 ≤ V <sub>Io</sub> ≤ V <sub>CC</sub> + 0.5 +0.5 ≥ V <sub>Io</sub> ≥ V <sub>EE</sub> - 0.5	4.5 -4.5	V V
V <sub>INPP</sub>	Differential Input Voltage  D - $\bar{D}$			V <sub>CC</sub> -V <sub>EE</sub>	V
I <sub>IN</sub>	Input Current Through R <sub>T</sub> (50 Ω Resistor)	Static Surge		45 80	mA mA
I <sub>OUT</sub>	Output Current (LVPECL Output)	Continuous Surge		50 100	mA mA
I <sub>VREFAC</sub>	V <sub>REFAC</sub> Sink/Source Current			±2.0	mA
T <sub>A</sub>	Operating Temperature Range	16 QFN		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	42 35	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 3)	QFN-16	4	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

# NB6L611

**Table 4. DC CHARACTERISTICS, Multi-Level Inputs**  $V_{CC} = 2.375\text{ V to }3.63\text{ V}$ ,  $V_{EE} = 0\text{ V}$ , or  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.375\text{ V to }-3.63\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
--------	----------------	-----	-----	-----	------

## POWER SUPPLY CURRENT

$I_{CC}$	Power Supply Current (Inputs and Outputs Open)	30	45	60	mA
----------	--	----	----	----	----

## LVPECL OUTPUTS (Notes 4 and 5)

$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1075$ 2225 1425	$V_{CC} - 950$ 2350 1550	$V_{CC} - 825$ 2475 1675	mV
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1875$ 1475 675	$V_{CC} - 1725$ 1575 775	$V_{CC} - 1625$ 1675 875	mV

## DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 9 and 10) (Note 6)

$V_{th}$	Input Threshold Reference Voltage Range (Note 7)	$V_{EE} + 1050$		$V_{CC} - 150$	mV
$V_{IH}$	Single-ended Input HIGH Voltage	$V_{th} + 150$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage	$V_{EE}$		$V_{th} - 150$	mV
$V_{ISE}$	Single-ended Input Voltage Amplitude ( $V_{IH} - V_{IL}$ )	300		$V_{CC} - V_{EE}$	mV

## $V_{REFAC}$

$V_{REFAC}$	Output Reference Voltage ( $V_{CC} \geq 2.5\text{ V}$ )	$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	mV
-------------	---	------------------	------------------	------------------	----

## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 11, 12 and 13) (Note 8)

$V_{IHD}$	Differential Input HIGH Voltage	$V_{EE} + 1200$		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage	$V_{EE}$		$V_{CC} - 150$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	$V_{EE} + 150$		$V_{CC} - V_{EE}$	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration) (Note 9)	$V_{EE} + 950$		$V_{CC} - 75$	mV
$I_{IH}$	Input HIGH Current D/D, (VTD/VTD Open)	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current D/D, (VTD/VTD Open)	-150		150	$\mu\text{A}$

## TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor (Measured from D to VTD)	40	50	60	$\Omega$
-----------	--	----	----	----	----------

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- LVPECL outputs loaded with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$  for proper operation.
- Input and output parameters vary 1:1 with  $V_{CC}$ .
- $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.
- $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.
- $V_{CMR}$  minimum varies 1:1 with  $V_{EE}$ .  $V_{CMR}$  maximum varies 1:1 with  $V_{CC}$ . The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal.

# NB6L611

**Table 5. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }3.63\text{ V}$ ,  $V_{EE} = 0\text{ V}$ , or  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.375\text{ V to }-3.63\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ; (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit	
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPP}$ ) (Note 14) (See Figure 3)	$f_{in} \leq 1.5\text{ GHz}$ 725 $f_{in} = 2.0\text{ GHz}$ 520 $f_{in} = 3.0\text{ GHz}$ 320 $f_{in} = 4.0\text{ GHz}$ 170	780 680 500 400		mV	
$t_{PD}$	Propagation Delay D to Q	225	280	375	ps	
$t_{SKEW}$	Duty Cycle Skew (Note 11) Within Device Skew Device to Device Skew (Note 12)		3	15 15 80	ps	
$t_{DC}$	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq 4.0\text{ GHz}$	40	50	60	ps
$t_{JITTER}$	RMS Random Clock Jitter (Note 13)	$f_{in} \leq 4.0\text{ GHz}$		0.2	0.5	ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14)	150		$V_{CC} - V_{EE}$	mV	
$t_r, t_f$	Output Rise/Fall Times @ 0.5 GHz (20% – 80%) Q, $\bar{Q}$		100	170	ps	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

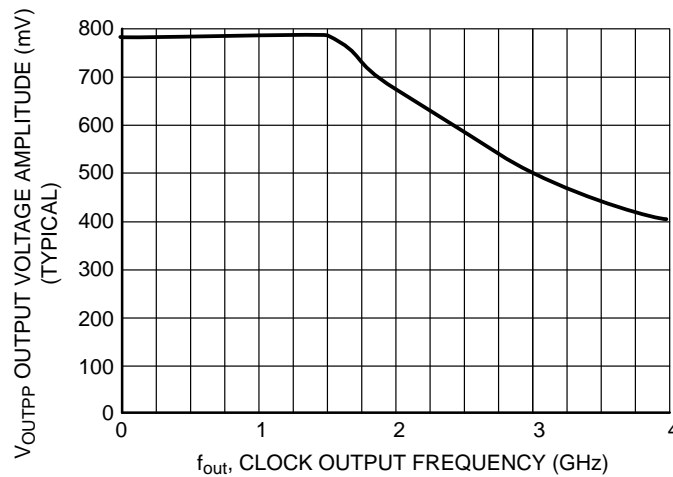
10. Measured by forcing  $V_{INPP}$  (MIN) from a 50% duty cycle clock source. All loading with an external  $R_L = 50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ . Input edge rates 40 ps (20% – 80%).

11. Duty cycle skew is measured between differential outputs using the deviations of the sum of  $T_{pw-}$  and  $T_{pw+}$  @ 0.5GHz.

12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.

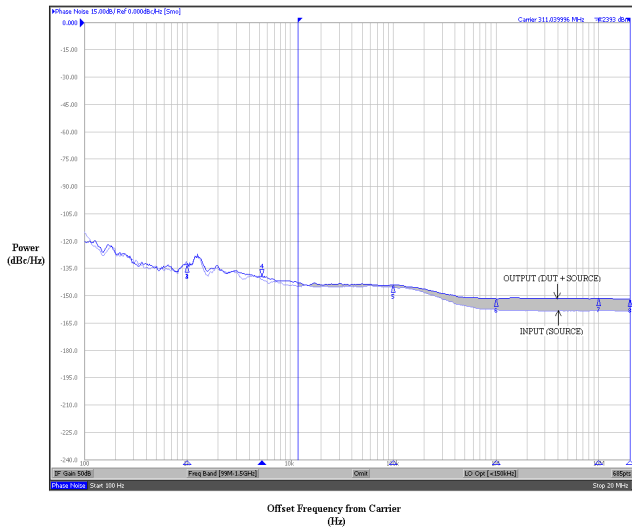
13. Additive RMS jitter with 50% duty cycle clock signal.

14. Input and output voltage swing is a single-ended measurement operating in differential mode.

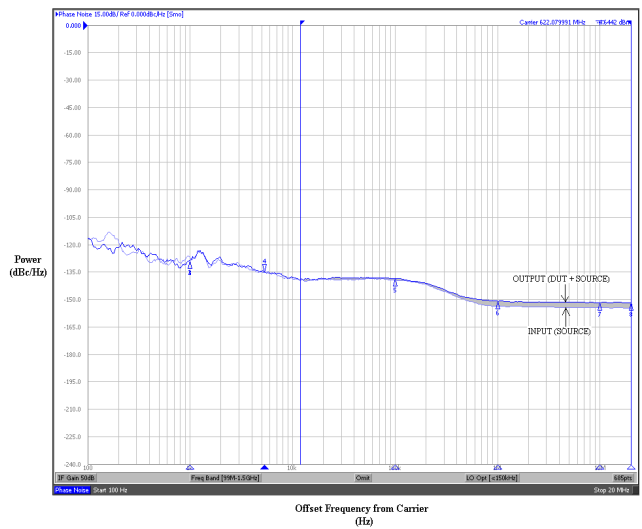


**Figure 3. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Output Frequency at Ambient Temperature (Typical)**

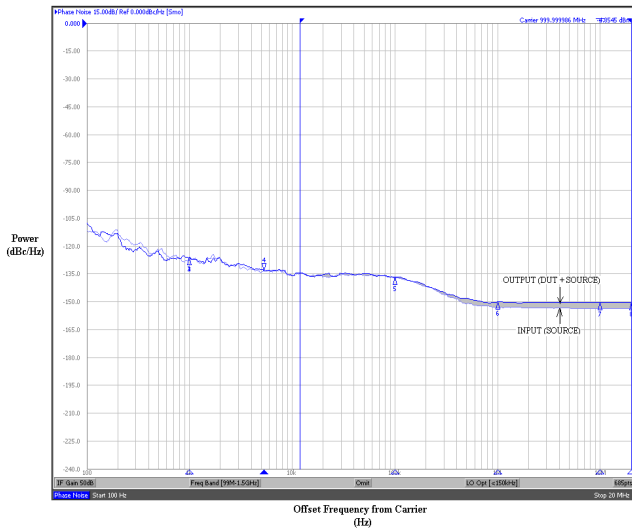
# NB6L611



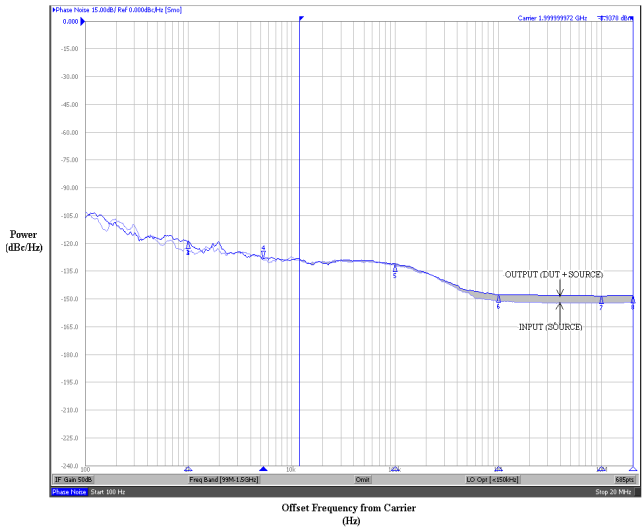
**Figure 4. Typical Phase Noise Plot at  $f_{\text{carrier}} = 311.04 \text{ MHz}$**



**Figure 5. Typical Phase Noise Plot at  $f_{\text{carrier}} = 622.08 \text{ MHz}$**



**Figure 6. Typical Phase Noise Plot at  $f_{\text{carrier}} = 1 \text{ GHz}$**



**Figure 7. Typical Phase Noise Plot at  $f_{\text{carrier}} = 2 \text{ GHz}$**

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L611 device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 44 fs, 11 fs, 8 fs and 6 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

# NB6L611

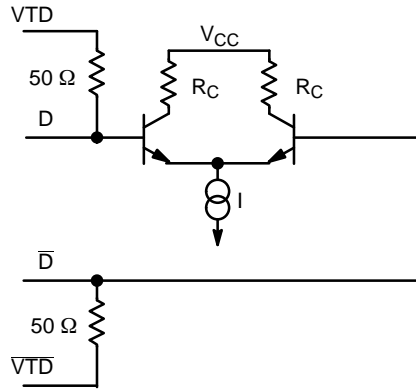


Figure 8. Input Structure

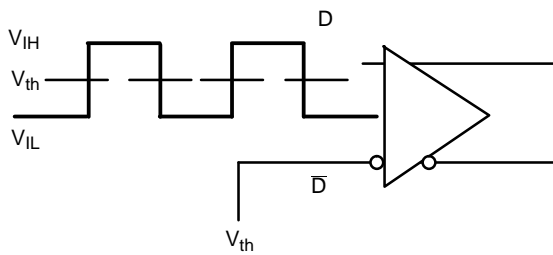


Figure 9. Differential Input Driven Single-Ended

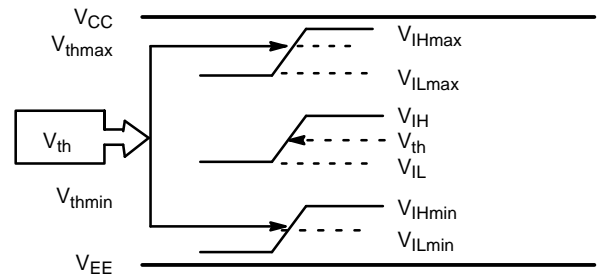


Figure 10.  $V_{th}$  Diagram

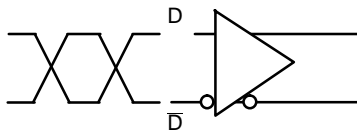


Figure 11. Differential Inputs Driven Differentially

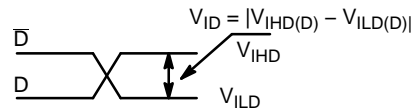


Figure 12. Differential Inputs Driven Differentially

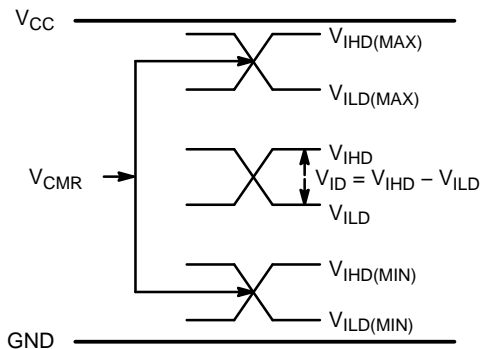


Figure 13.  $V_{CMR}$  Diagram

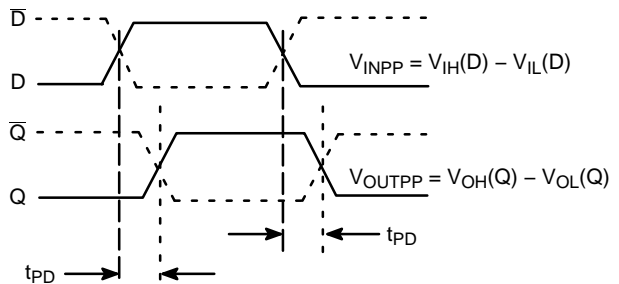


Figure 14. AC Reference Measurement

# NB6L611

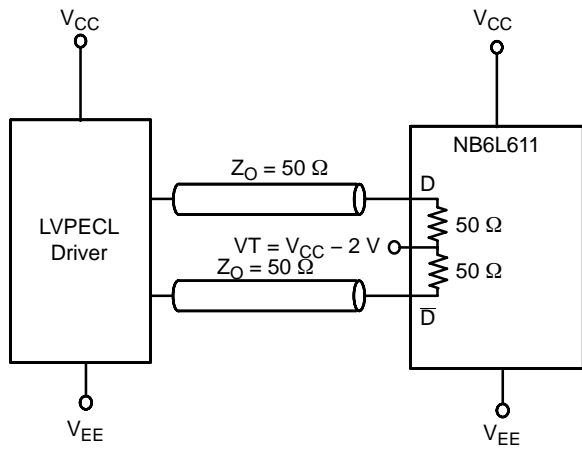


Figure 15. LVPECL Interface

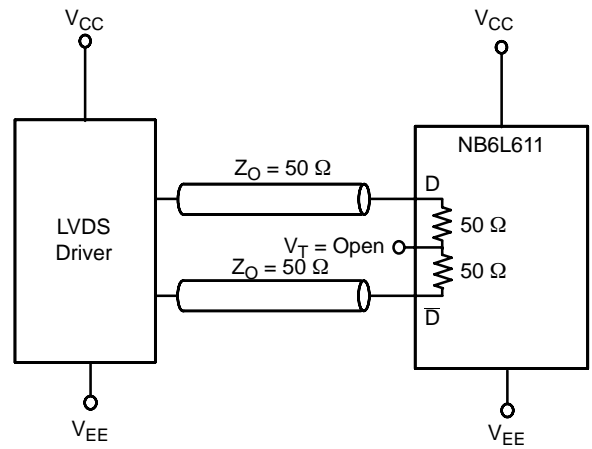


Figure 16. LVDS Interface

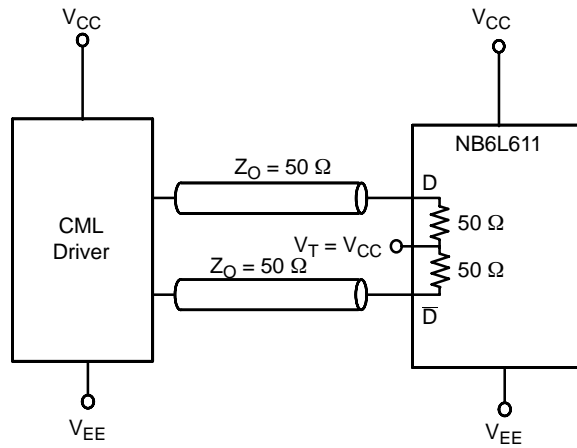


Figure 17. Standard 50 Ω Load CML Interface

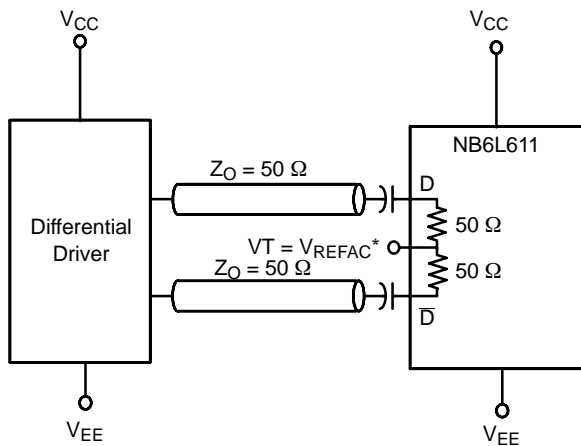


Figure 18. Capacitor-Coupled Differential Interface (VT Connected to  $V_{REFAC}$ )

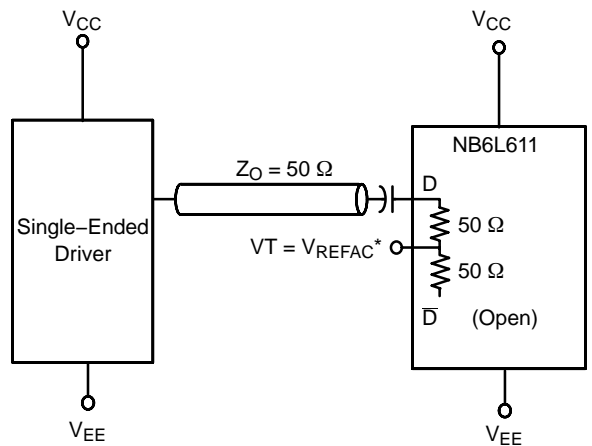
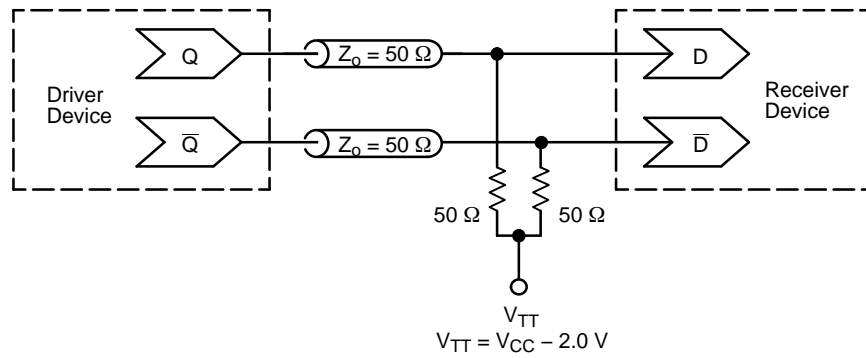


Figure 19. Capacitor-Coupled Single-Ended Interface (VT Connected to  $V_{REFAC}$ )

\* $V_{REFAC}$  bypassed to ground with a 0.01  $\mu$ F capacitor



## NB6L611



**Figure 20. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NB6L611MNG	QFN-16 (Pb-free)	123 Units / Rail
NB6L611MNR2G	QFN-16 (Pb-free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

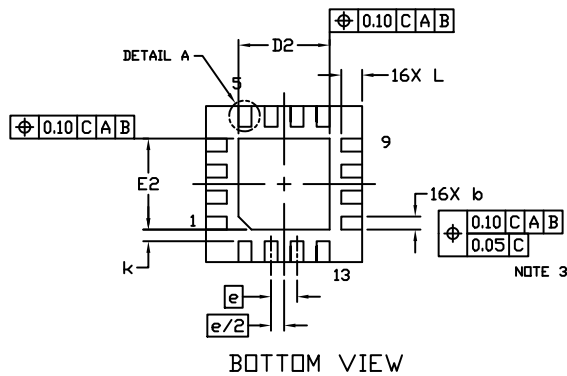
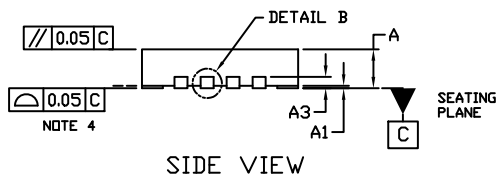
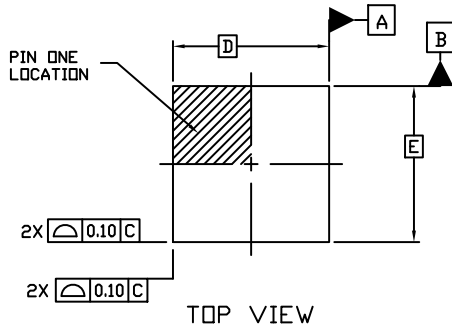
The products described herein (NB6L611), may be covered by U.S. patents including 6,362,644. There may be other patents pending. ECLinPS MAX is trademark of Semiconductor Components Industries, LLC (SCILLC).



1  
SCALE 2:1

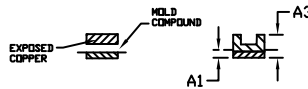
QFN16 3x3, 0.5P  
CASE 485G  
ISSUE G

DATE 08 OCT 2021

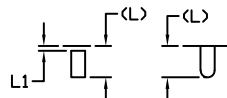


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



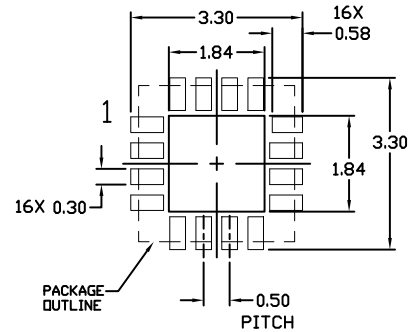
DETAIL B  
ALTERNATE CONSTRUCTIONS



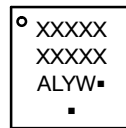
DETAIL A  
ALTERNATE TERMINAL CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON04795D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	QFN16 3X3, 0.5P	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)