# NCL30086BH

## Analog/Digital Dimmable Power Factor Corrected Quasi-Resonant Primary Side Current-Mode Controller for LED Lighting

The NCL30086BH is a controller targeting isolated and non–isolated "smart–dimmable" constant–current LED drivers. Designed to support flyback, buck–boost, and SEPIC topologies, its proprietary current–control algorithm provides near–unity power factor and tightly regulates a constant LED current from the primary side, thus eliminating the need for a secondary–side feedback circuitry or an optocoupler.

Housed in the SOIC10 which has the same body size as a standard SOIC8, the NCL30086BH is specifically intended for very compact space–efficient designs. The device is highly integrated with a minimum number of external components. A robust suite of safety protections is built in to simplify the design. To ensure reliable operation at elevated temperatures, a user configurable current foldback circuit is also provided. In addition, it supports analog and PWM dimming with a dedicated dimming input intended to control the average LED current.

Pin–to–pin compatible to the NCL30086, the NCL30086BH provides the same benefits with in addition, an increased resolution of the digital current–control algorithm for a 75% reduction in the LED current quantization ripple.

### Features

- Quasi–resonant Peak Current–mode Control Operation
- Valley Lockout Optimizes Efficiency over the Line/Load Range
- Constant Current Control with Primary Side Feedback
- Tight LED Constant Current Regulation of ±2% Typical
- Power Factor Correction
- Analog or PWM dimming
- Line Feedforward for Enhanced Regulation Accuracy
- Low Start–up Current (10 μA typ.)
- Wide $V_{cc}$ Range
- 300 mA / 500 mA Totem Pole Driver with 12 V Gate Clamp
- Robust Protection Features
  - Brown–Out Detection
  - OVP on $V_{CC}$
  - Programmable Over Voltage / LED Open Circuit Protection
  - Cycle–by–cycle Peak Current Limit
  - Winding Short Circuit Protection
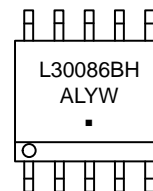  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Current Sense (CS) Short Detection
  - User programmable NTC Based Thermal Foldback
  - Thermal Shutdown
- −40 to 125°C Operating Junction Temperature
- Pb–Free, Halide–Free Product

### Typical Applications
- Integral LED Bulbs
- LED Light Engines
- LED Driver Power Supplies
- Smart LED Lighting Applications
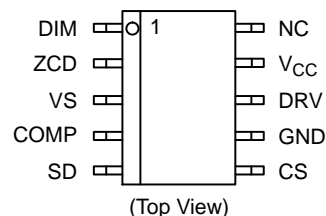
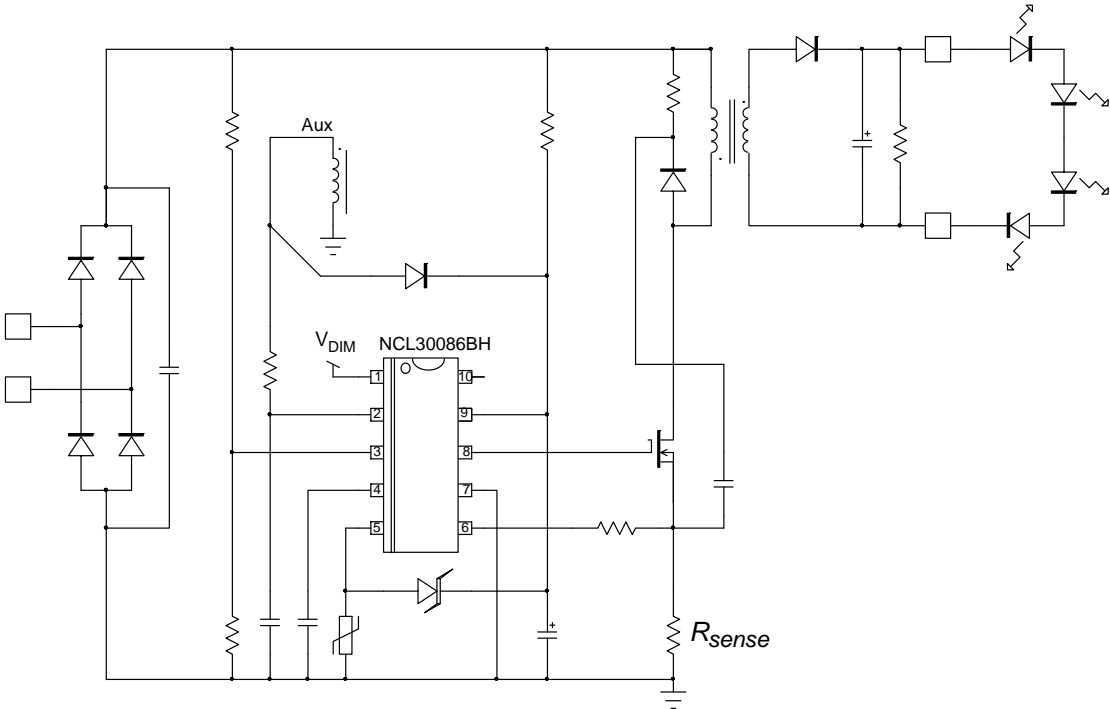## ON Semiconductor®

**SOIC−10**
**CASE 751BQ**

### MARKING DIAGRAM



L30086BH
ALYW
▪

L30086BH = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

### PIN CONNECTIONS

| | |
|---|---|
| DIM | NC |
| ZCD | $V_{CC}$ |
| VS | DRV |
| COMP | GND |
| SD | CS |

(Top View)

### ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

**February, 2016 − Rev. 0**

Publication Order Number:
**NCL30086BH/D**

**Figure 1. Typical Application Schematic in a Flyback Converter**
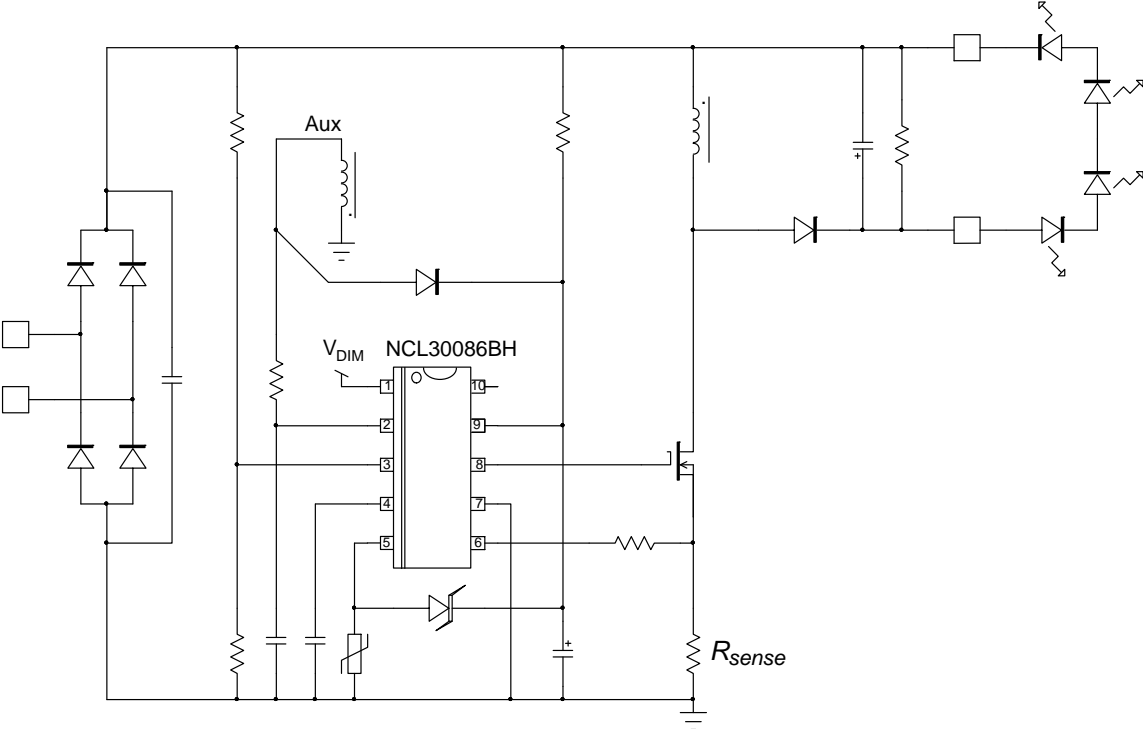


**Figure 2. Typical Application Schematic in a Buck−Boost Converter**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin No | Pin Name | Function | Pin Description |
|---|---|---|---|
| 1 | DIM | Analog / PWM Dimming | This pin is used for analog or PWM dimming control. An analog signal that can be varied between $V_{DIM0}$ and $V_{DIM100}$ or a PWM signal can be used to adjust the LED current. |
| 2 | ZCD | Zero Crossing Detection | Connected to the auxiliary winding, this pin detects the core reset event. |
| 3 | VS | Input Voltage Sensing | This pin monitors the input voltage rail for: Power Factor Correction Valley lockout Brownout Detection |
| 4 | COMP | Filtering Capacitor | This pin receives a filtering capacitor for power factor correction. Typical values ranges from $1 - 4.7$ $\mu$F. |
| 5 | SD | Thermal Foldback and Shutdown | Connecting an NTC to this pin allows the user to program thermal current fold-back threshold and slope. A Zener diode can also be used to pull–up the pin and stop the controller for adjustable OVP protection. |
| 6 | CS | Current Sense | This pin monitors the primary peak current. |
| 7 | GND | – | Controller ground pin. |
| 8 | DRV | Driver Output | The driver's output to an external MOSFET |
| 9 | $V_{CC}$ | IC Supply Pin | This pin is the positive supply of the IC. The circuit starts to operate when $V_{CC}$ exceeds 18 V and turns off when $V_{CC}$ goes below 8.8 V (typical values). After start–up, the operating range is 9.4 V up to 26 V ($V_{CC(OVP)}$ minimum level). |
| 10 | NC | – | – |

# NCL30086BH

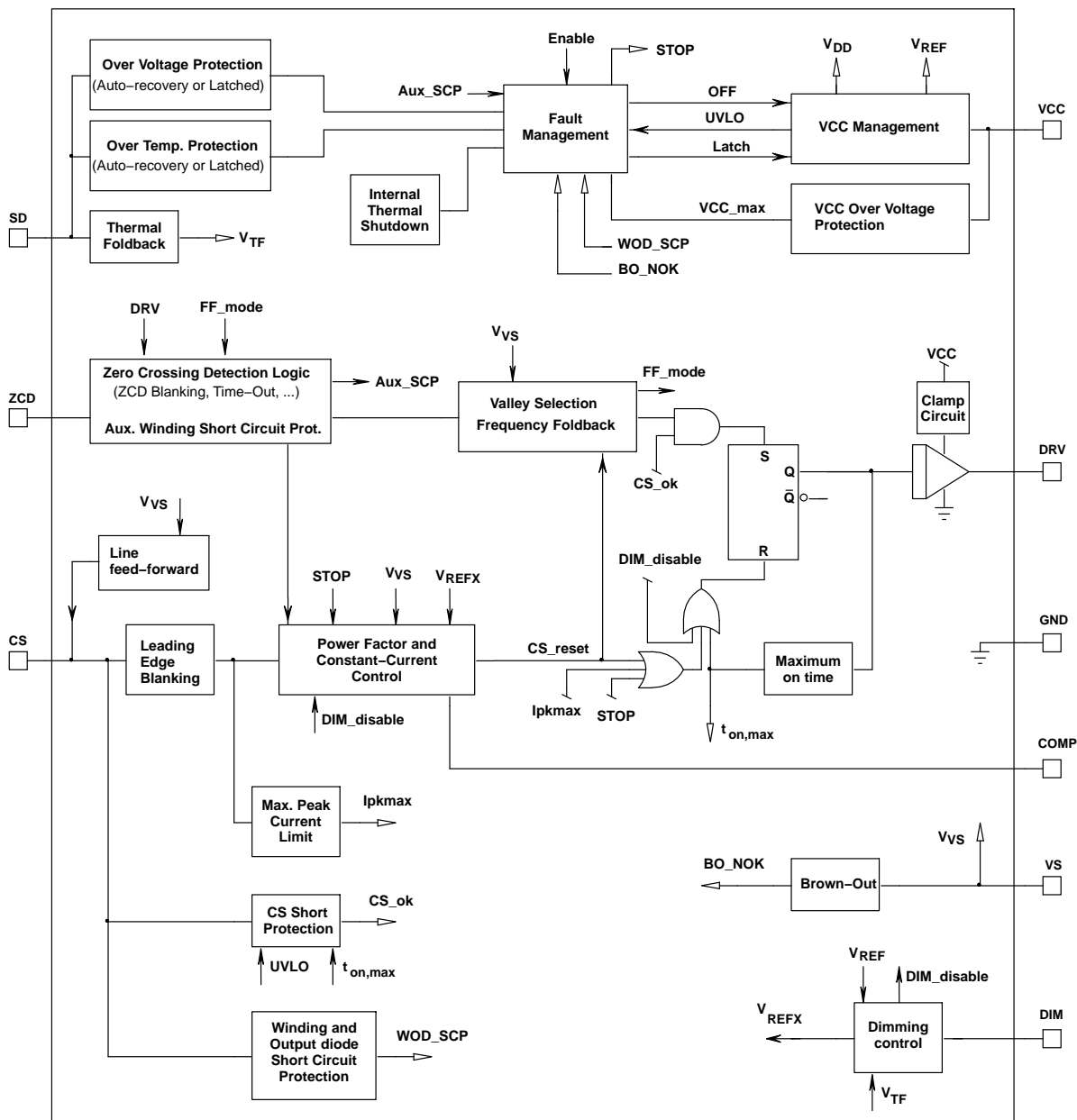## Internal Circuit Architecture



**Figure 3. Internal Circuit Architecture**

**Table 2. MAXIMUM RATINGS TABLE(S)**

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CC(MAX)}$<br>$I_{CC(MAX)}$ | Maximum Power Supply voltage, $V_{CC}$ pin, continuous voltage<br>Maximum current for $V_{CC}$ pin | –0.3 to 30<br>Internally limited | V<br>mA |
| $V_{DRV(MAX)}$<br>$I_{DRV(MAX)}$ | Maximum driver pin voltage, DRV pin, continuous voltage<br>Maximum current for DRV pin | –0.3, $V_{DRV}$ (Note 1)<br>–300, +500 | V<br>mA |
| $V_{MAX}$<br>$I_{MAX}$ | Maximum voltage on low power pins (except DRV and $V_{CC}$ pins)<br>Current range for low power pins (except DRV and $V_{CC}$ pins) | –0.3, 5.5 (Notes 2 and 5)<br>–2, +5 | V<br>mA |
| $R_{\theta J–A}$ | Thermal Resistance Junction–to–Air | 180 | °C/W |
| $T_{J(MAX)}$ | Maximum Junction Temperature | 150 | °C |
| | Operating Temperature Range | –40 to +125 | °C |
| | Storage Temperature Range | –60 to +150 | °C |
| | ESD Capability, HBM model (Note 3) | 3.5 | kV |
| | ESD Capability, MM model (Note 3) | 250 | V |
| | ESD Capability, CDM model (Note 3) | 2 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1.  $V_{DRV}$ is the DRV clamp voltage $V_{DRV(high)}$ when $V_{CC}$ is higher than $V_{DRV(high)}$. $V_{DRV}$ is $V_{CC}$ otherwise.
2.  These levels are low enough not to exceed the maximum ratings of the internal ESD 5.5–V Zener diode. More positive and negative voltages can be applied if the pin current stays within the –2 mA / 5 mA range.
3.  This device contains ESD protection and exceeds the following tests: Human Body Model 3500 V per JEDEC Standard JESD22–A114E, Machine Model Method 250 V per JEDEC Standard JESD22–A115B, Charged Device Model 2000 V per JEDEC Standard JESD22–C101E.
4.  This device contains latch–up protection and has been tested per JEDEC Standard JESD78D, Class I and exceeds ±100 mA.
5.  **Recommended maximum $V_S$ voltage for optimal operation is 4 V. –0.3 V to +4.0 V is hence, the $V_S$ pin recommended range.**

**Table 3. ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J = 25°C$, $V_{CC} = 12$ V, $V_{ZCD} = 0$ V, $V_{CS} = 0$ V, $V_{SD} = 1.5$ V) For min/max values $T_J = –40°C$ to +125°C, $V_{CC} = 12$ V)

| Description | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STARTUP AND SUPPLY CIRCUITS** | | | | | | |
| Supply Voltage<br>  Startup Threshold<br>  Minimum Operating Voltage<br>  Hysteresis $V_{CC(on)} – V_{CC(off)}$<br>  Internal logic reset | $V_{CC}$ rising<br>$V_{CC}$ rising<br>$V_{CC}$ falling | $V_{CC(on)}$<br>$V_{CC(off)}$<br>$V_{CC(HYS)}$<br>$V_{CC(reset)}$ | 16.0<br>8.2<br>8<br>4 | 18.0<br>8.8<br>–<br>5 | 20.0<br>9.4<br>–<br>6 | V |
| $V_{CC}$ Over Voltage Protection Threshold | | $V_{CC(OVP)}$ | 25.5 | 26.8 | 28.5 | V |
| $V_{CC(off)}$ noise filter<br>$V_{CC(reset)}$ noise filter | | $t_{VCC(off)}$<br>$t_{VCC(reset)}$ | –<br>– | 5<br>20 | –<br>– | µs |
| Startup current | | $I_{CC(start)}$ | – | 13 | 30 | µA |
| Startup current in fault mode | | $I_{CC(Fault)}$ | | 58 | 75 | µA |
| Supply Current<br>  Device Disabled/Fault<br>  Device Enabled/No output load on DRV pin<br>  Device Switching | $V_{CC} > V_{CC(off)}$<br>$F_{sw} = 65$ kHz<br>$C_{DRV} = 470$ pF, $F_{sw} = 65$ kHz | $I_{CC1}$<br>$I_{CC2}$<br>$I_{CC3}$ | 0.8<br>–<br>– | 1.0<br>2.6<br>3.0 | 1.2<br>4.0<br>4.5 | mA |
| **CURRENT SENSE** | | | | | | |
| Maximum Internal current limit | | $V_{ILIM}$ | 0.95 | 1.00 | 1.05 | V |
| Leading Edge Blanking Duration for $V_{ILIM}$ | | $t_{LEB}$ | 240 | 300 | 360 | ns |
| Propagation delay from current detection to gate off–state | | $t_{ILIM}$ | – | 100 | 150 | ns |

6.  Guaranteed by Design
7.  A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.
8.  At startup, when $V_{CC}$ reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 µs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

**Table 3. ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J = 25°C$, $V_{CC} = 12$ V, $V_{ZCD} = 0$ V, $V_{CS} = 0$ V, $V_{SD} = 1.5$ V) For min/max values $T_J = -40°C$ to $+125°C$, $V_{CC} = 12$ V)

| Description | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CURRENT SENSE** | | | | | | |
| Maximum on–time | | $t_{on(MAX)}$ | 26 | 36 | 46 | μs |
| Threshold for immediate fault protection activation | | $V_{CS(stop)}$ | 1.35 | 1.50 | 1.65 | V |
| Leading Edge Blanking Duration for $V_{CS(stop)}$ | | $t_{BCS}$ | – | 150 | – | ns |
| Current source for CS to GND short detection | | $I_{CS(short)}$ | 400 | 500 | 600 | μA |
| Current sense threshold for CS to GND short detection | $V_{CS}$ rising | $V_{CS(low)}$ | 30 | 65 | 100 | mV |
| **GATE DRIVE** | | | | | | |
| Drive Resistance<br> DRV Sink<br> DRV Source | | $R_{SNK}$<br>$R_{SRC}$ | –<br>– | 13<br>30 | –<br>– | Ω |
| Drive current capability<br> DRV Sink (Note 6)<br> DRV Source (Note 6) | | $I_{SNK}$<br>$I_{SRC}$ | –<br>– | 500<br>300 | –<br>– | mA |
| Rise Time (10% to 90%) | $C_{DRV} = 470$ pF | $t_r$ | – | 40 | – | ns |
| Fall Time (90% to 10%) | $C_{DRV} = 470$ pF | $t_f$ | – | 30 | – | ns |
| DRV Low Voltage | $V_{CC} = V_{CC(off)}+0.2$ V<br>$C_{DRV} = 470$ pF, $R_{DRV} = 33$ kΩ | $V_{DRV(low)}$ | 8 | – | – | V |
| DRV High Voltage | $V_{CC} = V_{CC(MAX)}$<br>$C_{DRV} = 470$ pF, $R_{DRV} = 33$ kΩ | $V_{DRV(high)}$ | 10 | 12 | 14 | V |
| **ZERO VOLTAGE DETECTION CIRCUIT** | | | | | | |
| Upper ZCD threshold voltage | $V_{ZCD}$ rising | $V_{ZCD(rising)}$ | – | 90 | 150 | mV |
| Lower ZCD threshold voltage | $V_{ZCD}$ falling | $V_{ZCD(falling)}$ | 35 | 55 | – | mV |
| ZCD hysteresis | | $V_{ZCD(HYS)}$ | 15 | – | – | mV |
| Propagation Delay from valley detection to DRV high | $V_{ZCD}$ falling | $T_{DEM}$ | – | 100 | 300 | ns |
| Blanking delay after on–time | $V_{REFX} > 30\%$ $V_{REF}$ | $T_{ZCD(blank1)}$ | 1.12 | 1.50 | 1.88 | μs |
| Blanking delay at light load | $V_{REFX} < 25\%$ $V_{REF}$ | $T_{ZCD(blank2)}$ | 0.56 | 0.75 | 0.94 | μs |
| Timeout after last DEMAG transition | | $T_{TIMO}$ | 5.0 | 6.5 | 8.0 | μs |
| Pulling–down resistor | $V_{ZCD} = V_{ZCD(falling)}$ | $R_{ZCD(PD)}$ | – | 200 | – | kΩ |
| **CONSTANT CURRENT AND POWER FACTOR CONTROL** | | | | | | |
| Reference Voltage at $T_J = 25°C$ | | $V_{REF}$ | 245 | 250 | 255 | mV |
| Reference Voltage $T_J = 25°C$ to $100°C$ | | $V_{REF}$ | 242.5 | 250.0 | 257.5 | mV |
| Reference Voltage $T_J = -40°C$ to $125°C$ | | $V_{REF}$ | 240 | 250 | 260 | mV |
| Current sense lower threshold | $V_{CS}$ falling | $V_{CS(low)}$ | 20 | 50 | 100 | mV |
| $V_{control}$ to current setpoint division ratio | | $V_{ratio}$ | – | 4 | – | – |
| Error amplifier gain | $V_{REFX} = V_{REF}$ | $G_{EA}$ | 40 | 50 | 60 | μS |
| Error amplifier current capability | $V_{REFX} = V_{REF}$ (no dimming)<br>$V_{REFX} = 25\%*$ $V_{REF}$ | $I_{EA}$ | | ±60<br>±240 | | μA |
| COMP Pin Start–up Current Source | COMP pin grounded | $I_{EA\_STUP}$ | | 140 | | μA |

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7. A NTC is generally placed between the SD and GND pins. Parameters $R_{TF(start)}$, $R_{TF(stop)}$, $R_{OTP(off)}$ and $R_{OTP(on)}$ give the resistance the NTC must exhibit to respectively, enter thermal foldback, stop thermal foldback, trigger the OTP limit and allow the circuit recovery after an OTP situation.
8. At startup, when $V_{CC}$ reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 μs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

**Table 3. ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J = 25°C$, $V_{CC} = 12$ V, $V_{ZCD} = 0$ V, $V_{CS} = 0$ V, $V_{SD} = 1.5$ V) For min/max values $T_J = -40°C$ to $+125°C$, $V_{CC} = 12$ V)

| Description | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LINE FEED FORWARD** | | | | | | |
| $V_{VS}$ to $I_{CS(offset)}$ conversion ratio | | $K_{LFF}$ | 18 | 20 | 22 | µS |
| Line feed–forward current on CS pin | DRV high, $V_{VS} = 2$ V | $I_{FF}$ | 35 | 40 | 45 | µA |
| Offset current maximum value | | $I_{offset(MAX)}$ | 80 | 100 | 120 | µA |
| **VALLEY LOCKOUT SECTION** | | | | | | |
| Threshold for high– line range (HL) detection | $V_{VS}$ rising | $V_{HL}$ | 2.28 | 2.40 | 2.52 | V |
| Threshold for low–line range (LL) detection | $V_{VS}$ falling | $V_{LL}$ | 2.18 | 2.30 | 2.42 | V |
| Blanking time for line range detection | | $t_{HL(blank)}$ | 15 | 25 | 35 | ms |
| **FREQUENCY FOLDBACK** | | | | | | |
| Minimum additional dead time in frequency fold-back mode | | $t_{FF1LL}$ | 1.4 | 2.0 | 2.6 | µs |
| Additional dead time | $V_{REFX} = 5\%$ $V_{REF}$ | $t_{FF2HL}$ | – | 40 | – | µs |
| Additional dead time | $V_{REFX} = 0\%$ $V_{REF}$ | $t_{FF3HL}$ | 90 | | – | µs |
| **FAULT PROTECTION** | | | | | | |
| Thermal Shutdown (Note 6) | $F_{SW} = 65$ kHz | $T_{SHDN}$ | 130 | 150 | 170 | °C |
| Thermal Shutdown Hysteresis | | $T_{SHDN(HYS)}$ | – | 50 | – | °C |
| Threshold voltage for output short circuit or aux. winding short circuit detection | | $V_{ZCD(short)}$ | 0.8 | 1.0 | 1.2 | V |
| Short circuit detection Timer | $V_{ZCD} < V_{ZCD(short)}$ | $t_{OVLD}$ | 70 | 90 | 110 | ms |
| Auto–recovery timer duration | | $t_{recovery}$ | 3 | 4 | 5 | s |
| SD pin Clamp series resistor | | $R_{SD(clamp)}$ | | 1.6 | | kΩ |
| Clamped voltage | SD pin open | $V_{SD(clamp)}$ | 1.13 | 1.35 | 1.57 | V |
| SD pin detection level for OVP | $V_{SD}$ rising | $V_{OVP}$ | 2.35 | 2.50 | 2.65 | V |
| Delay before OVP or OTP confirmation | | $T_{SD(delay)}$ | 22.5 | 30.0 | 37.5 | µs |
| Reference current for direct connection of an NTC (Note 8) | | $I_{OTP(REF)}$ | 80 | 85 | 90 | µA |
| Fault detection level for OTP (Note 7) | $V_{SD}$ falling | $V_{OTP(off)}$ | 0.47 | 0.50 | 0.53 | V |
| SD pin level for operation recovery after an OTP detection | $V_{SD}$ rising | $V_{OTP(on)}$ | 0.66 | 0.70 | 0.74 | V |
| OTP blanking time when circuit starts operating (Note 8) | | $t_{OTP(start)}$ | 250 | | 370 | µs |
| SD pin voltage where thermal fold–back starts ($V_{REF}$ is decreased) | | $V_{TF(start)}$ | 0.94 | 1.00 | 1.06 | V |
| SD pin voltage at which thermal fold–back stops ($V_{REF}$ is clamped to $V_{REF50}$) | | $V_{TF(stop)}$ | 0.64 | 0.69 | 0.74 | V |
| $V_{TF(start)}$ over $I_{OTP(REF)}$ ratio (Note 7) | $T_J = +25°C$ to $+125°C$ | $R_{TF(start)}$ | 10.8 | 11.7 | 12.6 | kΩ |
| $V_{TF(stop)}$ over $I_{OTP(REF)}$ ratio (Note 7) | $T_J = +25°C$ to $+125°C$ | $R_{TF(stop)}$ | 7.4 | 8.1 | 8.8 | kΩ |
| $V_{OTP(off)}$ over $I_{OTP(REF)}$ ratio (Note 7) | $T_J = +25°C$ to $+125°C$ | $R_{OTP(off)}$ | 5.4 | 5.9 | 6.4 | kΩ |
| $V_{OTP(on)}$ over $I_{OTP(REF)}$ ratio (Note 7) | $T_J = +25°C$ to $+125°C$ | $R_{OTP(on)}$ | 7.5 | 8.1 | 8.7 | kΩ |

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8. At startup, when $V_{CC}$ reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 µs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

**Table 3. ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: For typical values $T_J = 25°C$, $V_{CC} = 12$ V, $V_{ZCD} = 0$ V, $V_{CS} = 0$ V, $V_{SD} = 1.5$ V) For min/max values $T_J = -40°C$ to $+125°C$, $V_{CC} = 12$ V)

| Description | Test Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FAULT PROTECTION** | | | | | | |
| $V_{REFX}$ @ $V_{SD} = 600$ mV (as percentage of $V_{REF}$) | SD pin falling (no OTP detection) | $V_{REF(50)}$ | 40 | 50 | 60 | % |
| **BROWN–OUT** | | | | | | |
| Brown–Out ON level (IC start pulsing) | $V_S$ rising | $V_{BO(on)}$ | 0.95 | 1.00 | 1.05 | V |
| Brown–Out OFF level (IC shuts down) | $V_S$ falling | $V_{BO(off)}$ | 0.85 | 0.90 | 0.95 | V |
| BO comparators delay | | $t_{BO(delay)}$ | | 30 | | μs |
| Brown–Out blanking time | | $t_{BO(blank)}$ | 15 | 25 | 35 | ms |
| $V_S$ pin Pulling–down Current | $V_S = V_{BO(on)}$ | $I_{BO(bias)}$ | 50 | 250 | 450 | nA |
| **DIMMING SECTION** | | | | | | |
| DIM pin voltage for zero output current (OFF voltage) | $V_{DIM}$ falling | $V_{DIM0}$ | 0.66 | 0.70 | 0.74 | V |
| DIM pin voltage for maximum output current ($V_{REFX} = V_{REF}$) | $V_{DIM}$ rising | $V_{DIM100}$ | – | 2.45 | 2.60 | V |
| DIM pin voltage for 50% output current ($V_{REFX} = 125$ mV) | $V_{DIM}$ rising or falling | $V_{DIM50}$ | 1.35 | 1.57 | 1.75 | V |
| Dimming range | | $V_{DIM(range)}$ | | 1.75 | | V |
| Dimming pin pull–up current source | | $I_{DIM(pullup)}$ | 7.5 | 9.6 | 12 | μA |

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8. At startup, when $V_{CC}$ reaches $V_{CC(on)}$, the controller blanks OTP for more than 250 μs to avoid detecting an OTP fault by allowing the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin.

**TYPICAL CHARACTERISTICS**
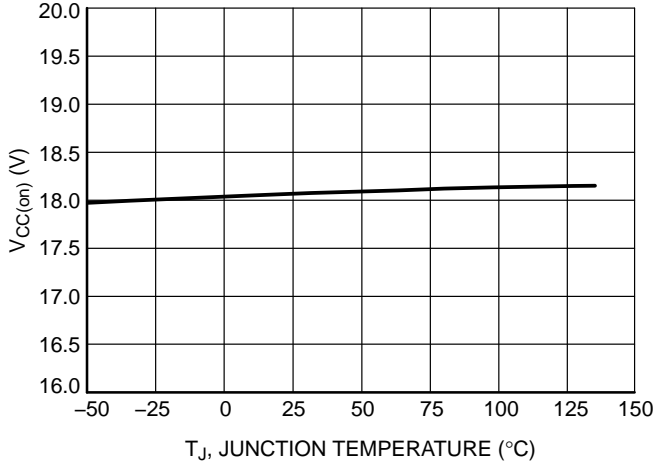


**Figure 4. V$_{CC}$ Start–up Threshold vs. Temperature**
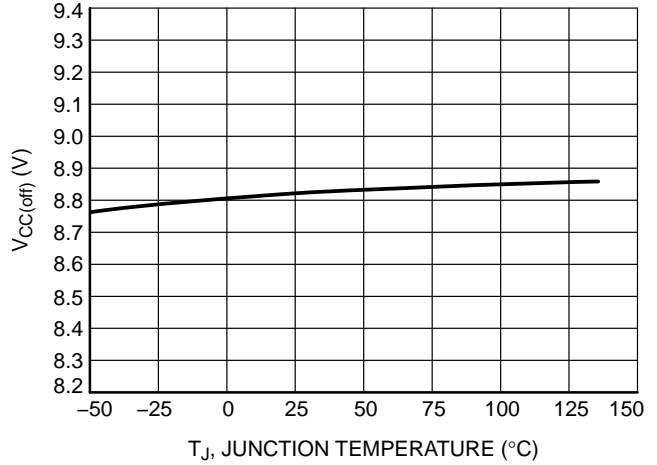


**Figure 5. V$_{CC}$ Minimum Operating Voltage vs. Temperature**
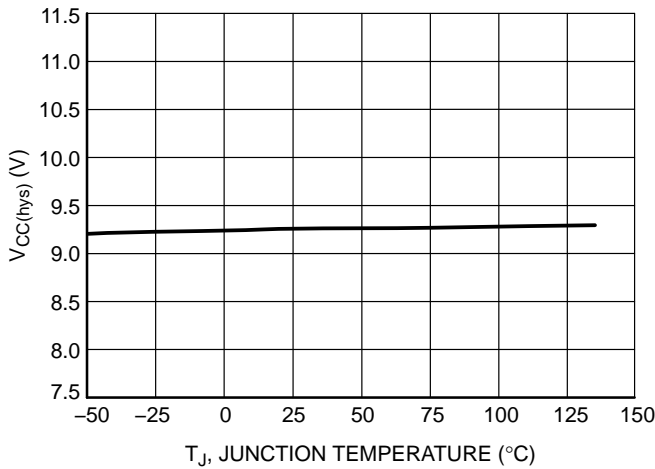


**Figure 6. Hysteresis (V$_{CC(on)}$ − V$_{CC(off)}$) vs. Temperature**
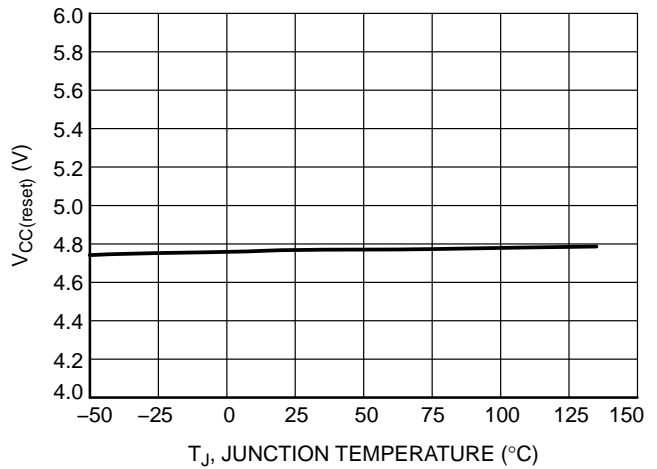


**Figure 7. V$_{CC(reset)}$ vs. Temperature**

# NCL30086BH

## TYPICAL CHARACTERISTICS
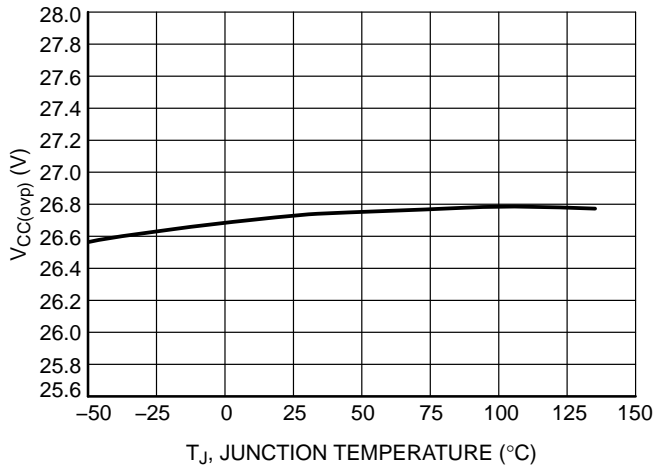
Figure 8. V$_{CC}$ Over Voltage Protection
Threshold vs. Temperature
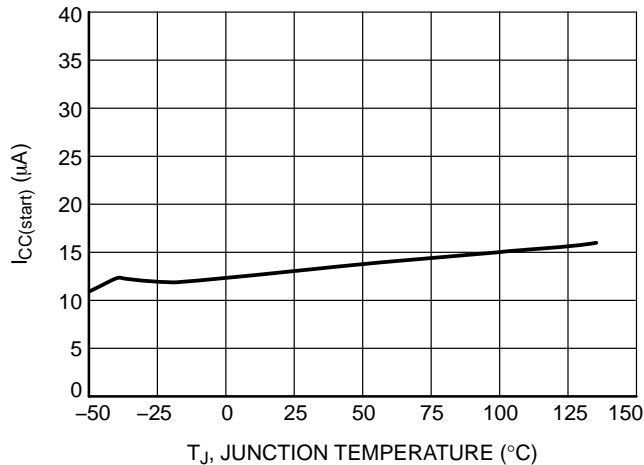
Figure 9. Start−up Current vs. Temperature
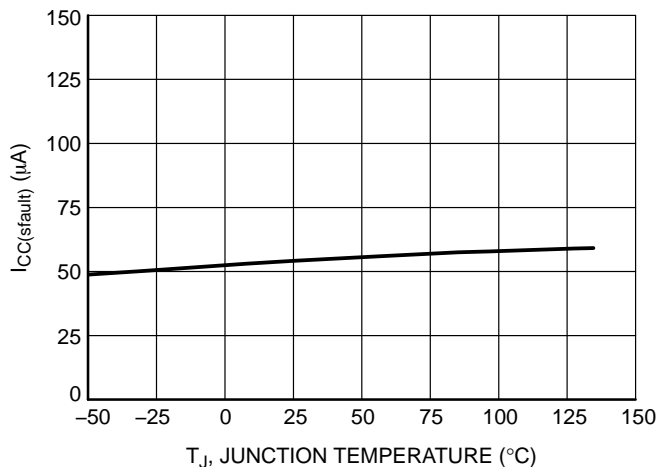
Figure 10. Start−up Current in Fault Mode vs.
Temperature
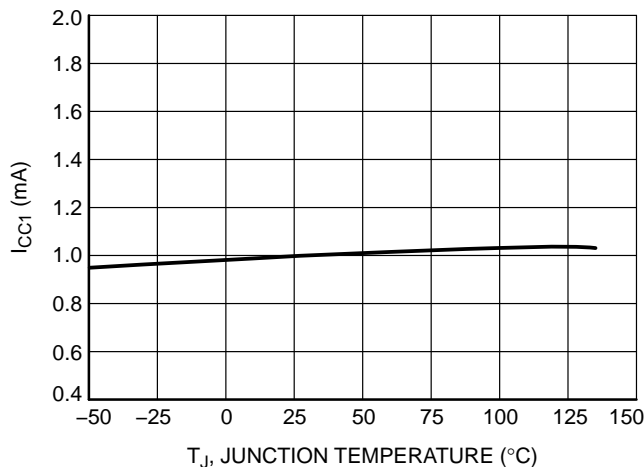
Figure 11. I$_{CC1}$ vs. Temperature
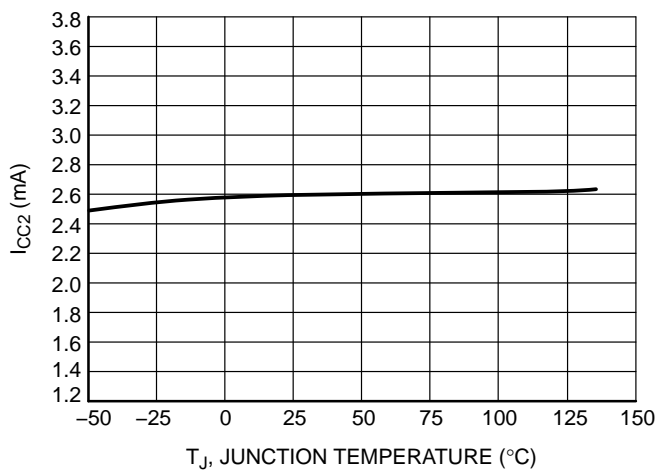
Figure 12. I$_{CC2}$ vs. Temperature
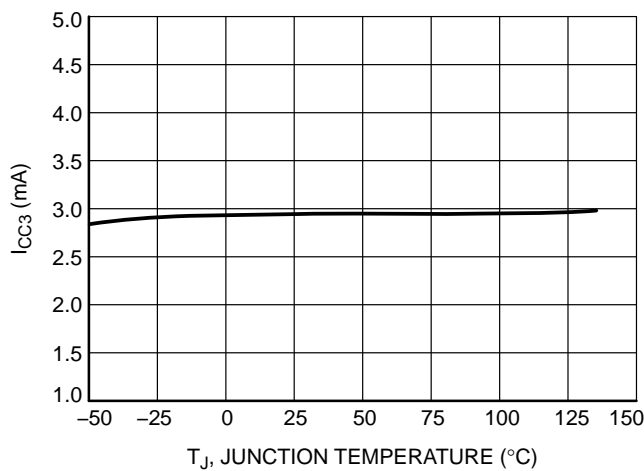
Figure 13. I$_{CC3}$ vs. Temperature

## TYPICAL CHARACTERISTICS
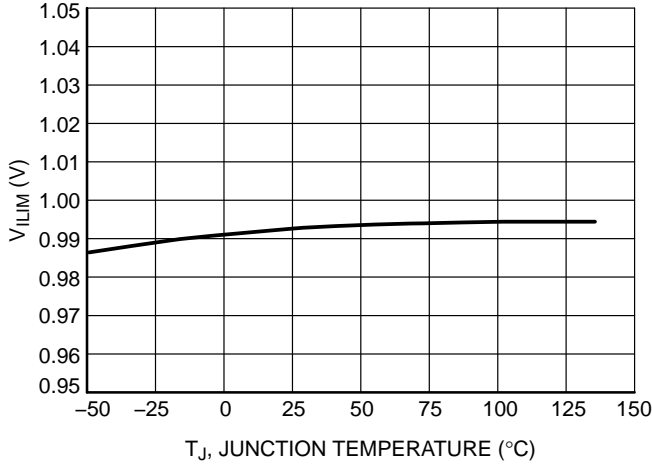


**Figure 14. Maximum Internal Current Limit vs. Temperature**
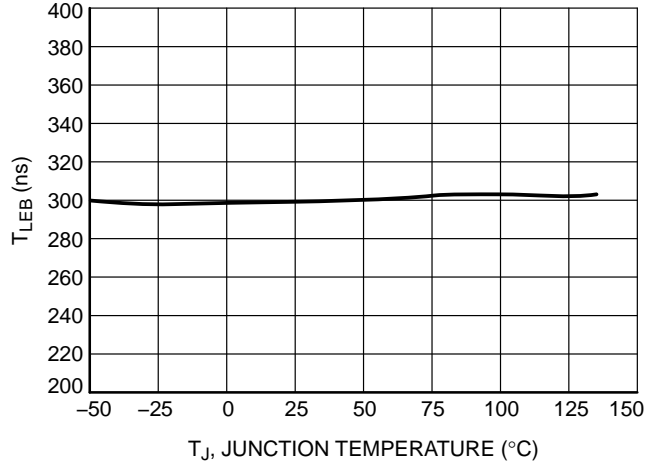


**Figure 15. Leading Edge Blanking vs. Temperature**
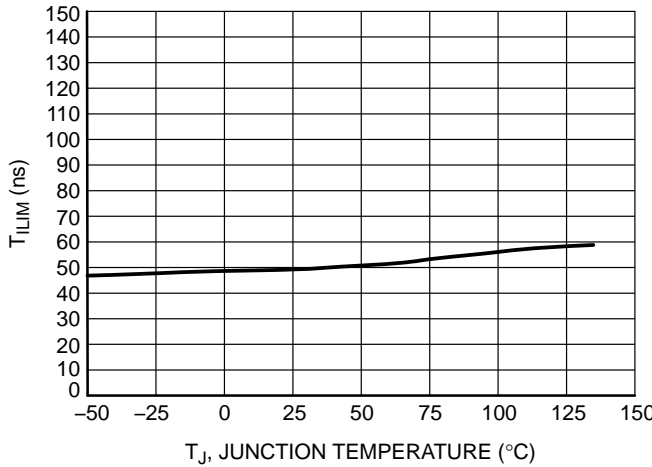


**Figure 16. Current Limit Propagation Delay vs. Temperature**
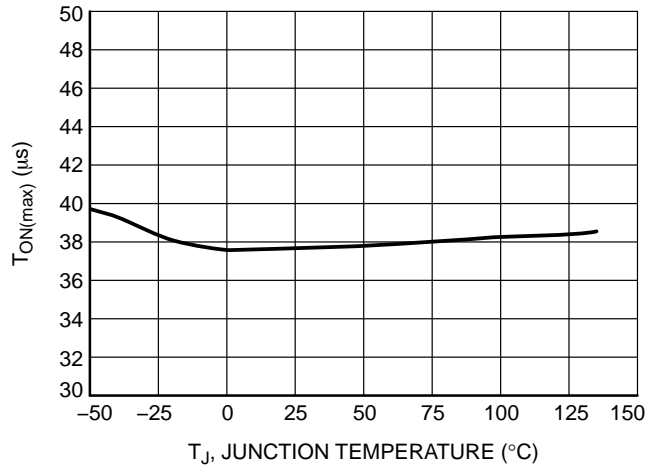


**Figure 17. Maximum On–time vs. Temperature**
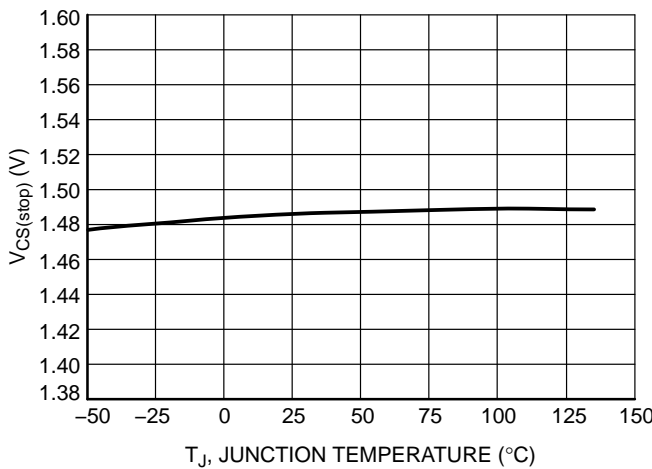


**Figure 18. V$_{CS(stop)}$ vs. Temperature**
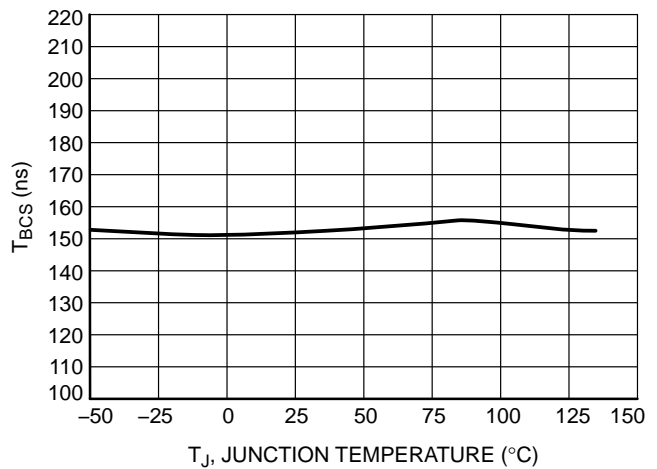


**Figure 19. Leading Edge Blanking Duration for V$_{CS(stop)}$ vs. Temperature**

## TYPICAL CHARACTERISTICS
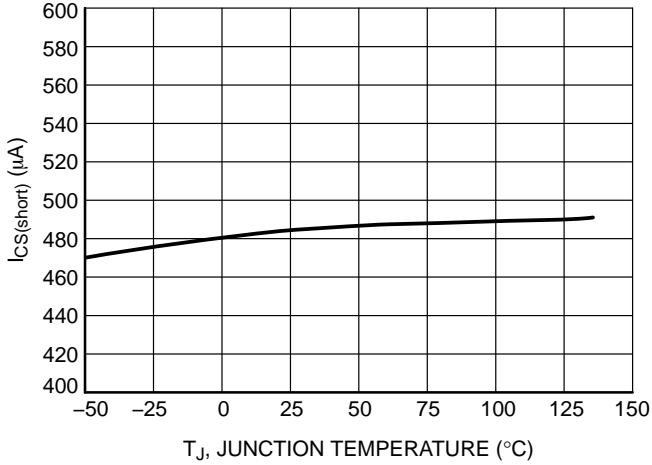


**Figure 20. $I_{CS(short)}$ vs. Temperature**
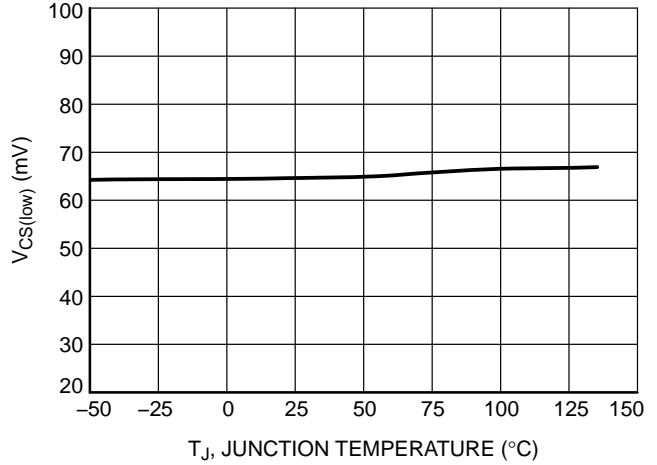


**Figure 21. $V_{CS(low)}$, $V_{CS}$ Rising vs. Temperature**
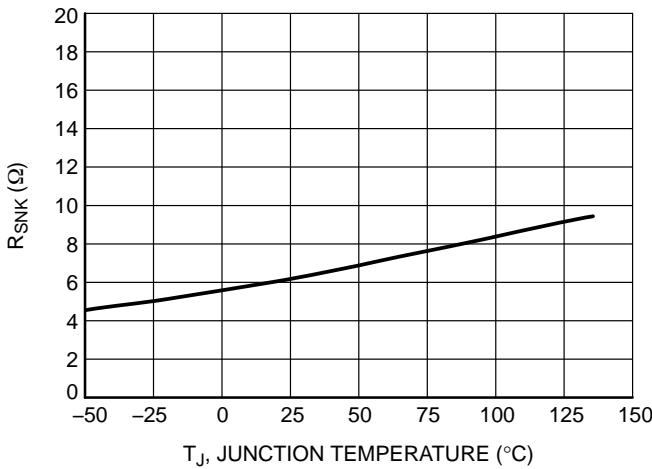


**Figure 22. Sink Gate Drive Resistance vs. Temperature**
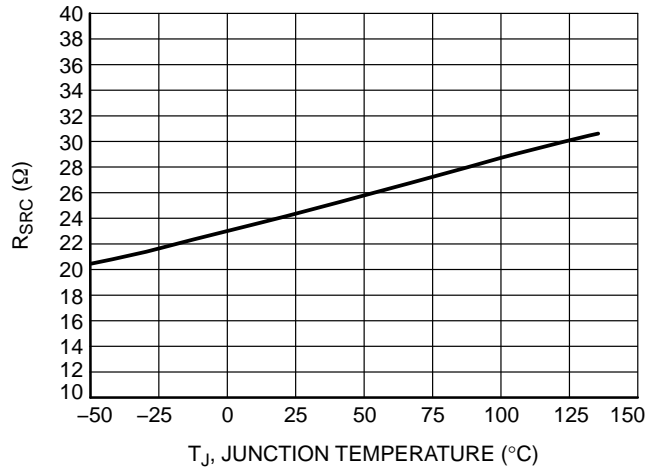


**Figure 23. Source Gate Drive Resistance vs. Temperature**
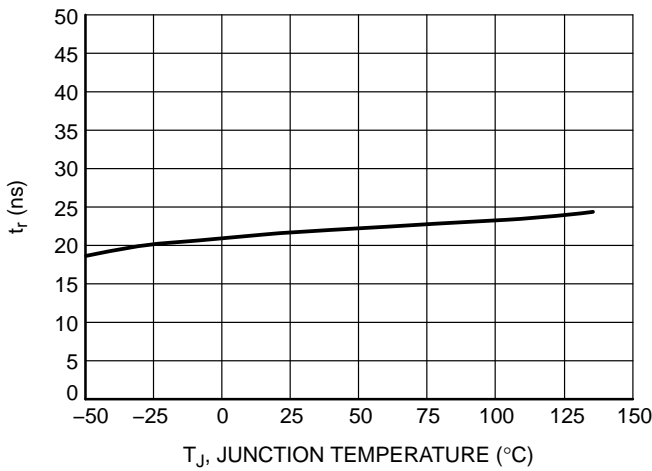


**Figure 24. Gate Drive Rise Time vs. Temperature**
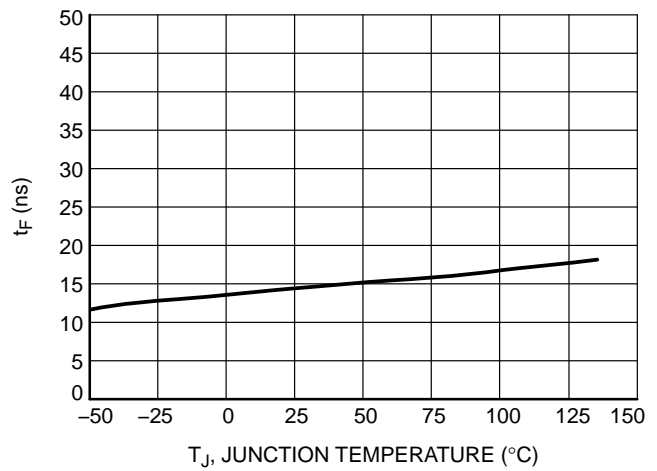


**Figure 25. Gate Drive Fall Time ($C_{DRV}$ = 470 pF) vs. Temperature**

## TYPICAL CHARACTERISTICS
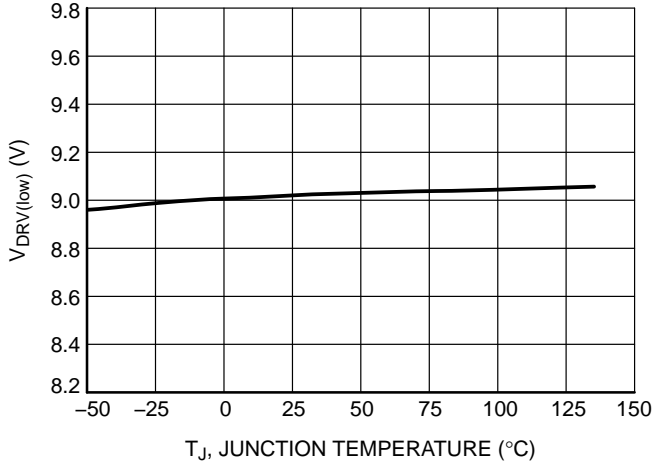


**Figure 26. DRV Low Voltage vs. Temperature**
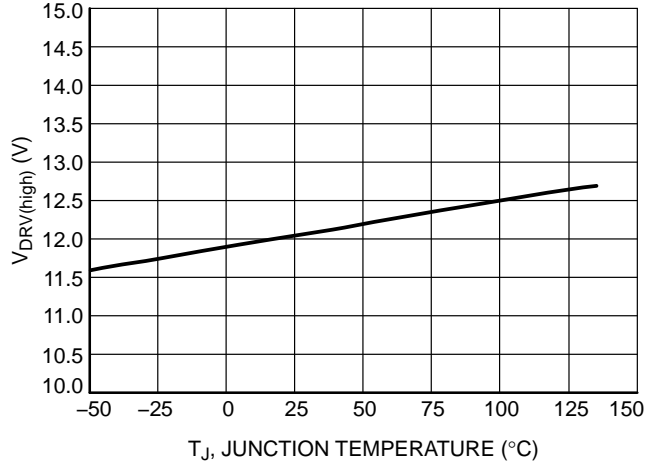


**Figure 27. DRV High Voltage vs. Temperature**
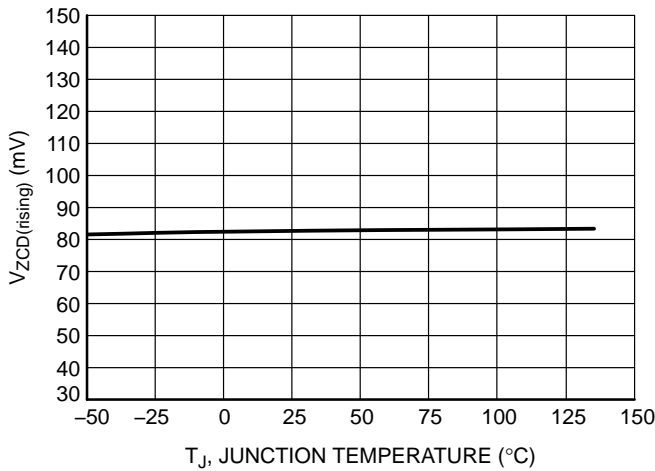


**Figure 28. Upper ZCD Threshold Voltage vs. Temperature**
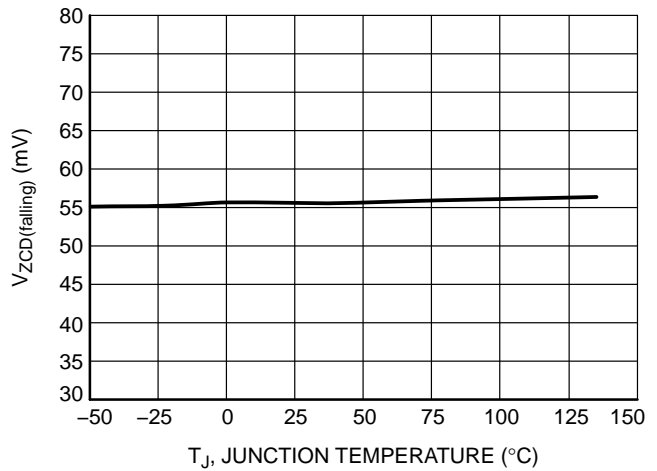


**Figure 29. Lower ZCD Threshold vs. Temperature**
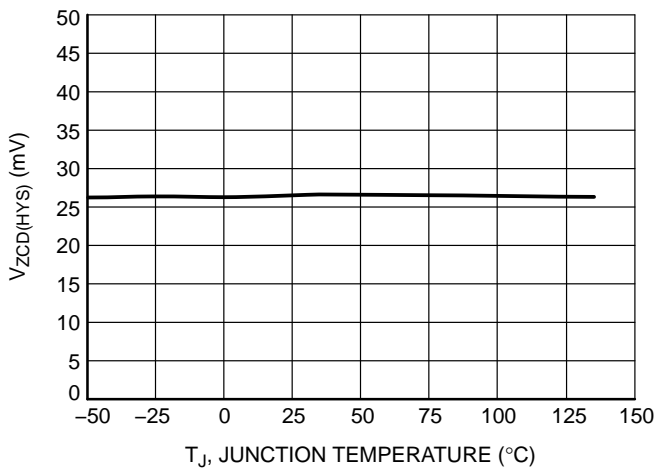


**Figure 30. ZCD Hysteresis vs. Temperature**
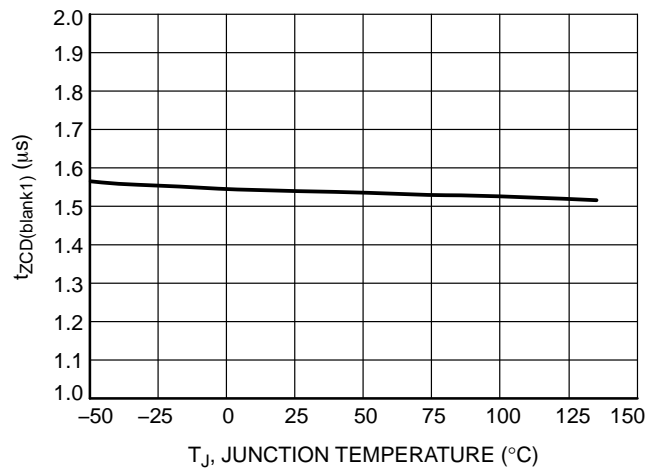


**Figure 31. ZCD Blanking Delay vs. Temperature**

## TYPICAL CHARACTERISTICS
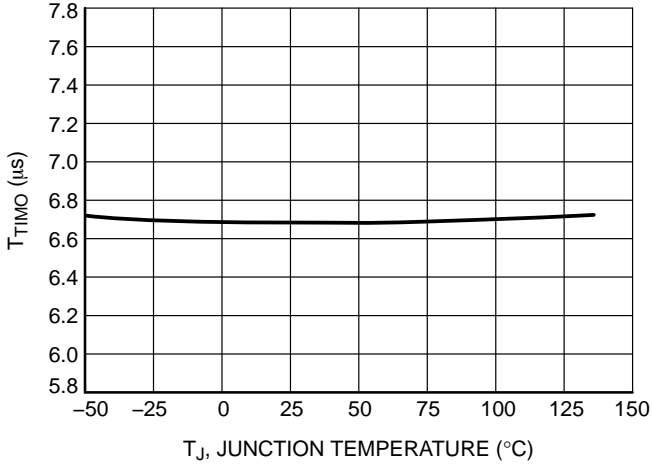


Figure 32. ZCD Time–out vs. Temperature
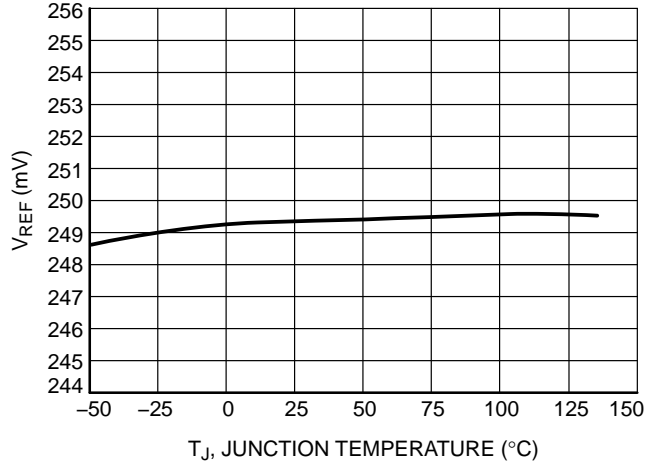


Figure 33. Reference Voltage vs. Temperature
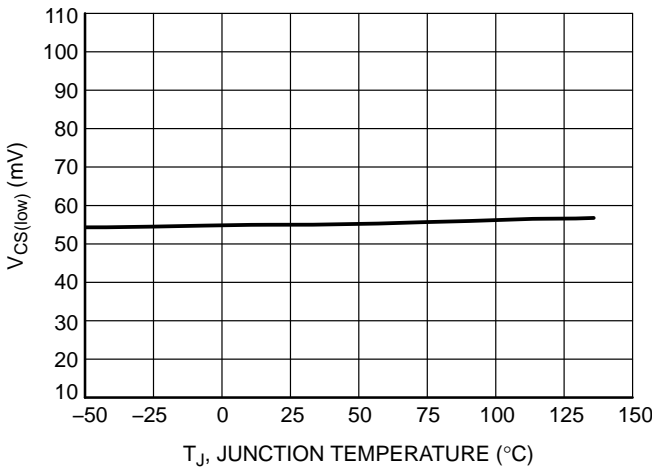


Figure 34. Current Sense Lower Threshold
($V_{CS}$ Falling) vs. Temperature
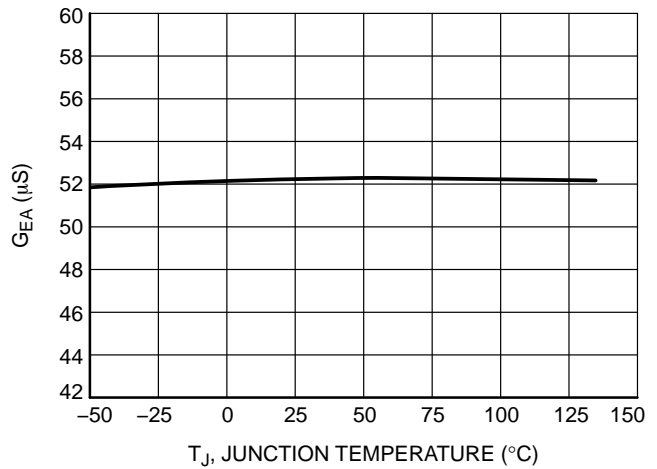


Figure 35. Error Amplifier Trans–conductance
Gain vs. Temperature
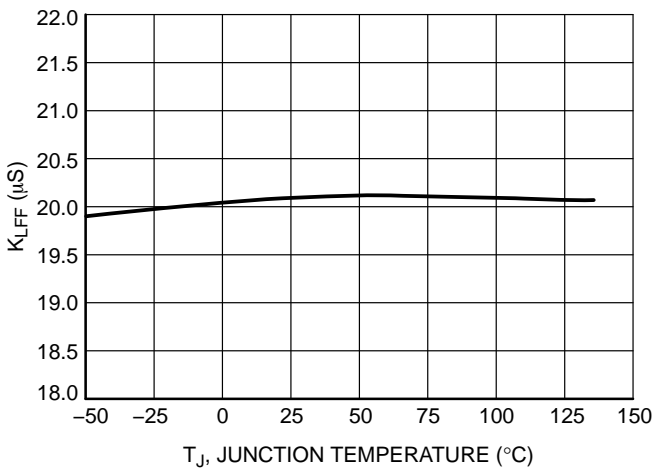


Figure 36. Feedforward $V_{VS}$ to $I_{CS(offset)}$
Conversion Ratio vs. Temperature
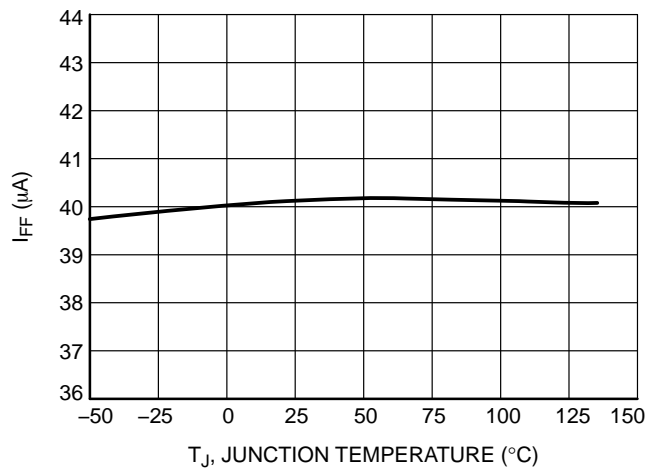


Figure 37. Line Feedforward Current on CS
Pin (@ $V_{VS}$ = 2 V) vs. Temperature

## TYPICAL CHARACTERISTICS
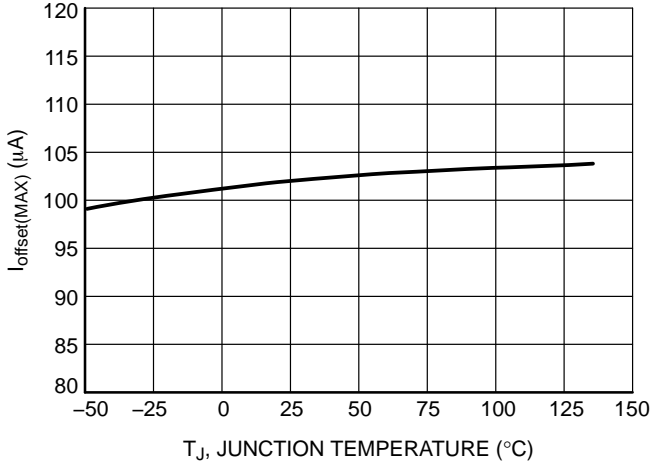


**Figure 38. I_offset(MAX) vs. Temperature**
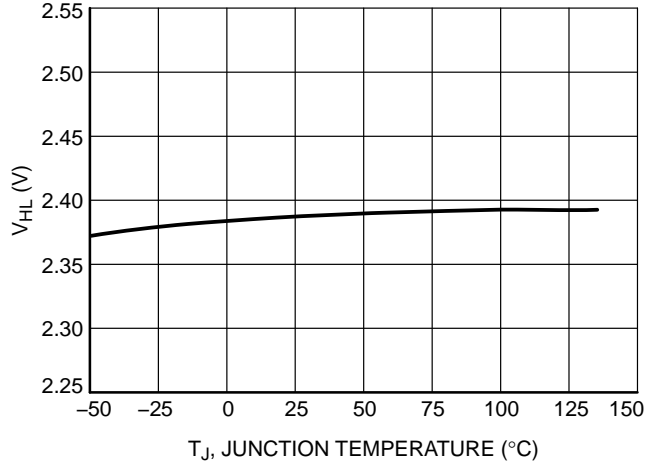


**Figure 39. Threshold for High−line Range Detection vs. Temperature**
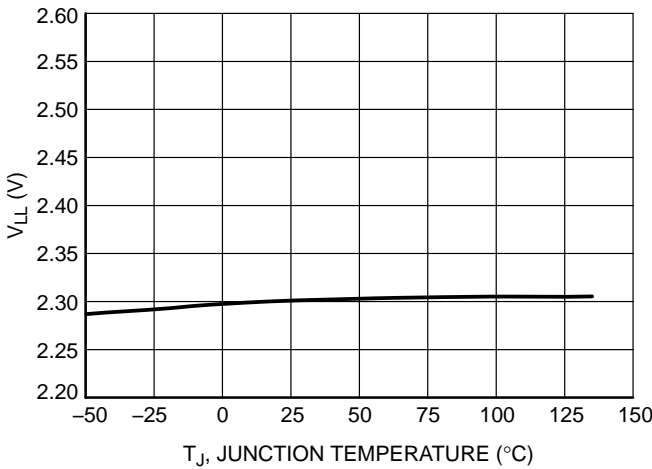


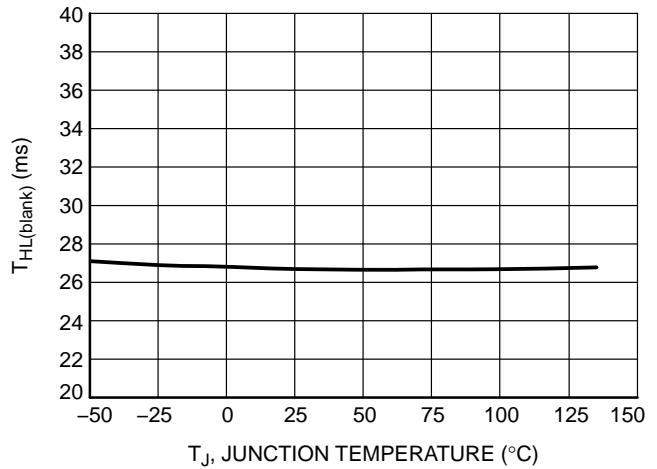**Figure 40. Threshold for Low−line Range Detection vs. Temperature**



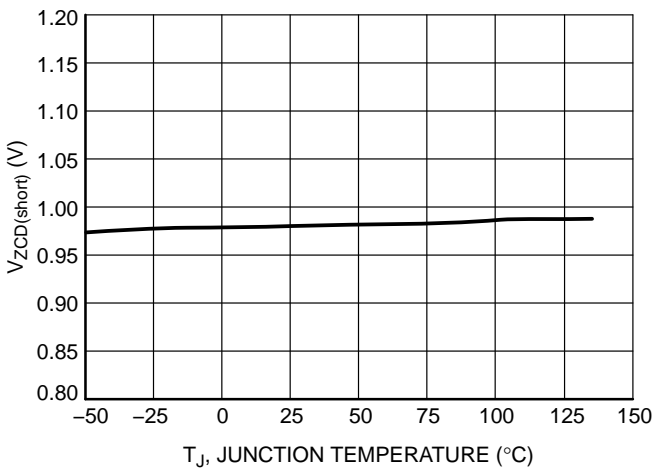**Figure 41. Blanking Time for Low−line Range Detection vs. Temperature**



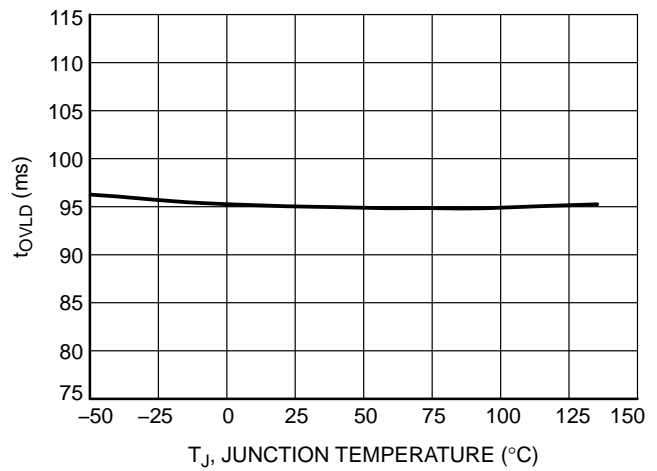**Figure 42. Threshold Voltage for Output Short Circuit Detection vs. Temperature**



**Figure 43. Short Circuit Detection Timer vs. Temperature**
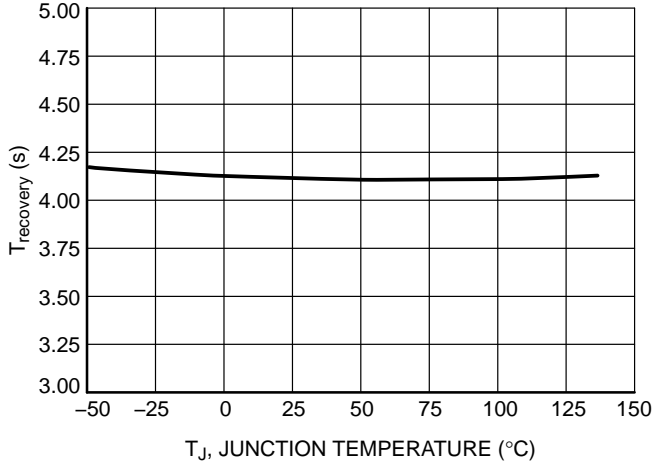
## TYPICAL CHARACTERISTICS



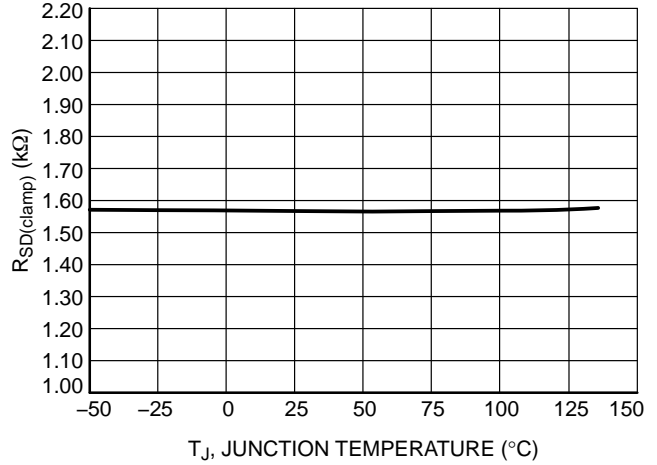**Figure 44. Auto−recovery Timer Duration vs. Temperature**



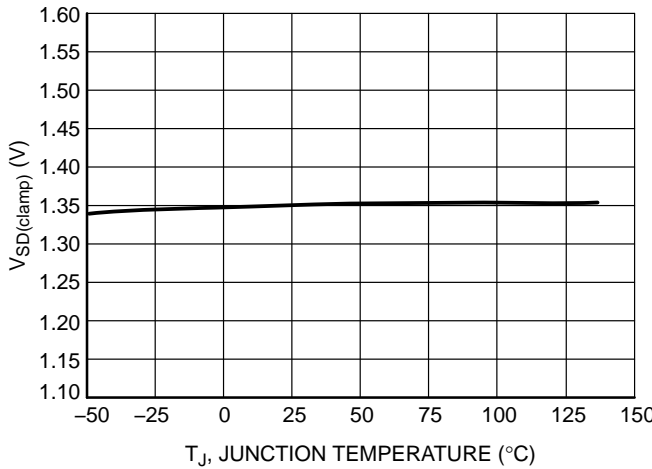**Figure 45. SD Pin Clamp Series Resistor vs. Temperature**



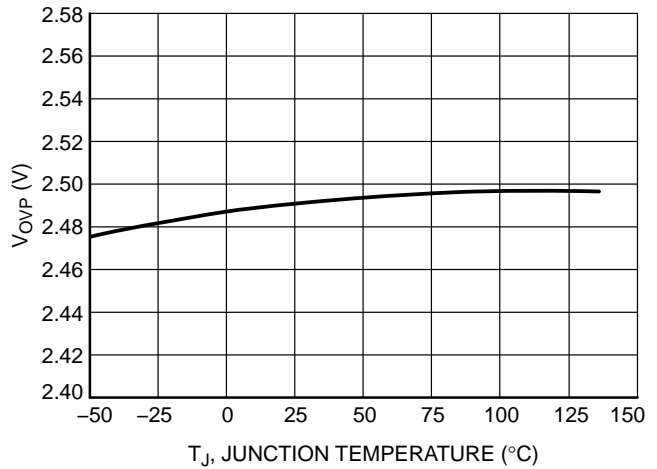**Figure 46. SD Pin Clamp Voltage vs. Temperature**



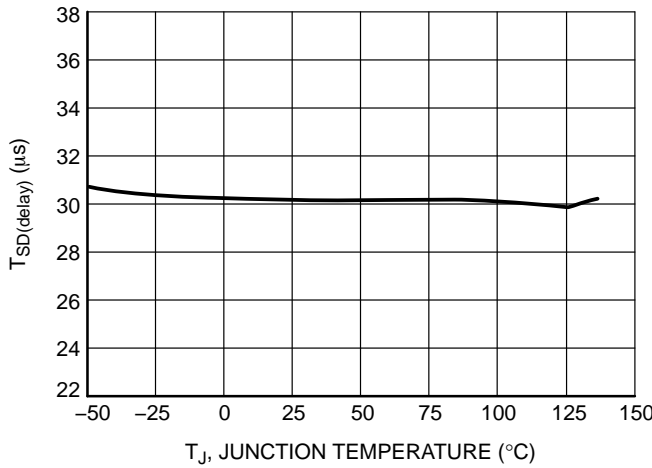**Figure 47. SD Pin OVP Threshold Voltage vs. Temperature**

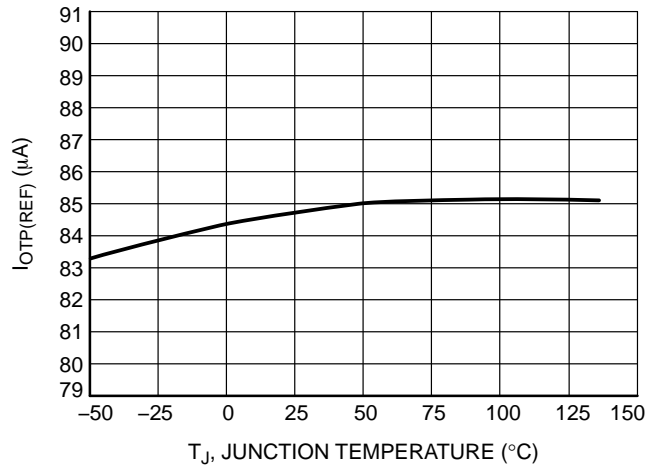

**Figure 48. $T_{SD(delay)}$ vs. Temperature**



**Figure 49. $I_{OTP(REF)}$ vs. Temperature**

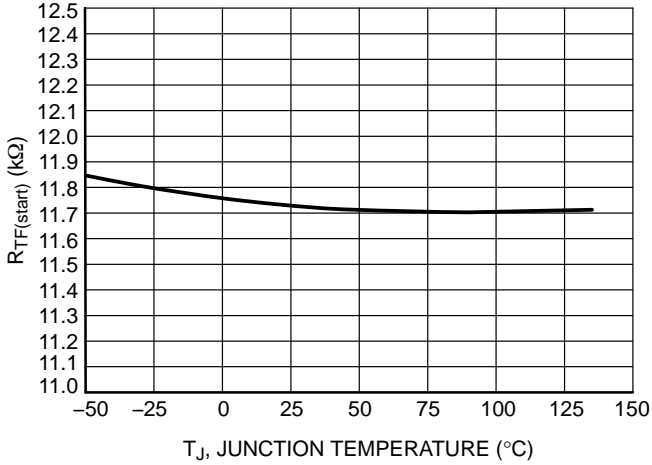## TYPICAL CHARACTERISTICS



**Figure 50. R$_{TF(start)}$ vs. Temperature**
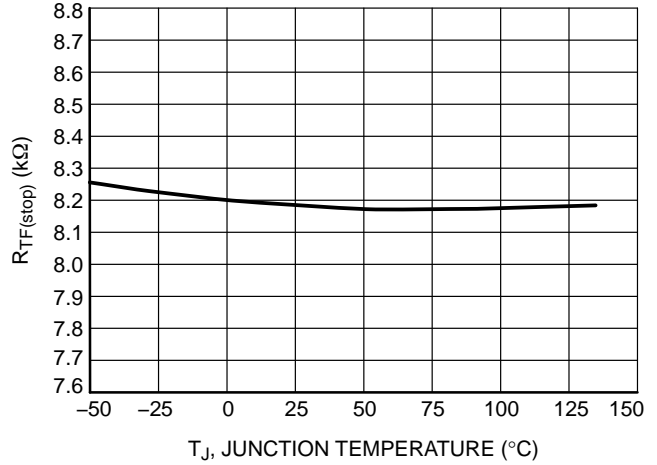


**Figure 51. R$_{TF(stop)}$ vs. Temperature**



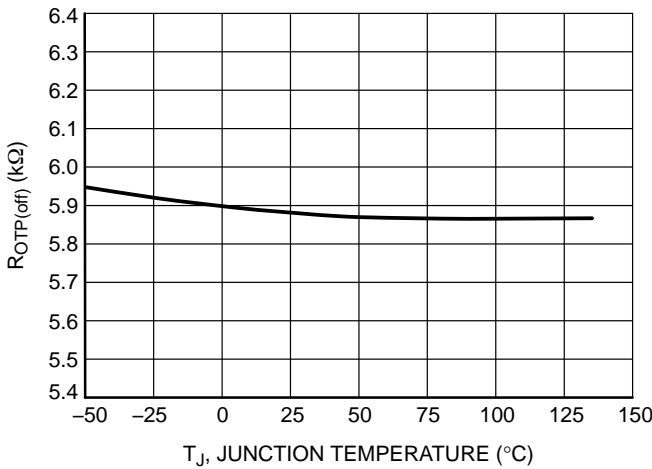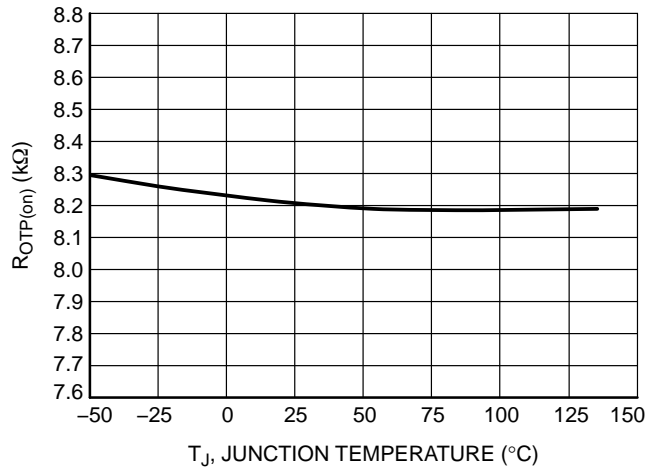**Figure 52. R$_{OTP(off)}$ vs. Temperature**



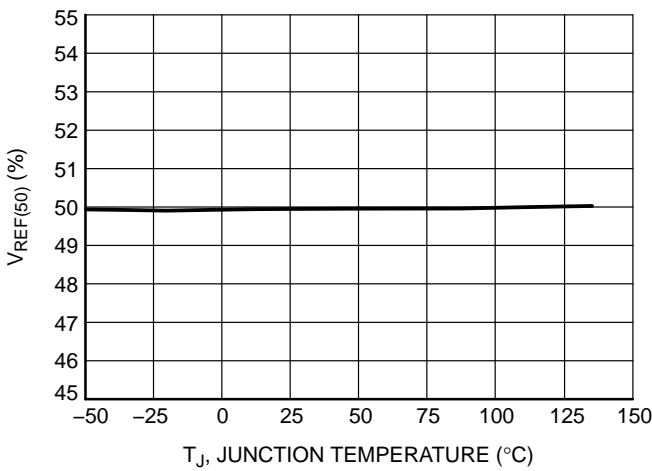**Figure 53. R$_{OTP(on)}$ vs. Temperature**



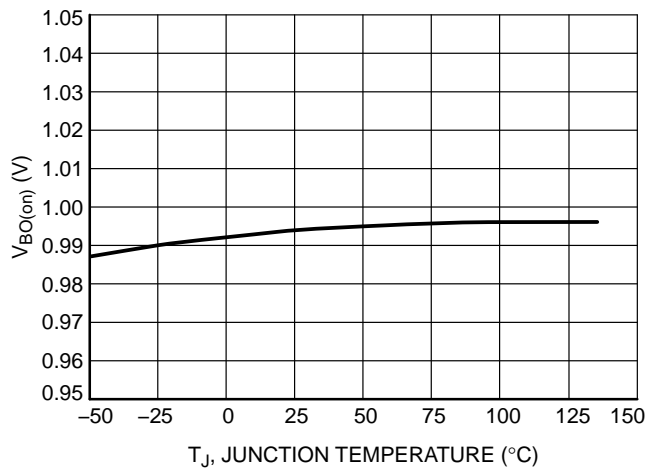**Figure 54. Ratio V$_{REF(50)}$ over V$_{REF}$ vs. Temperature**



**Figure 55. Brown−out ON Level vs. Temperature**
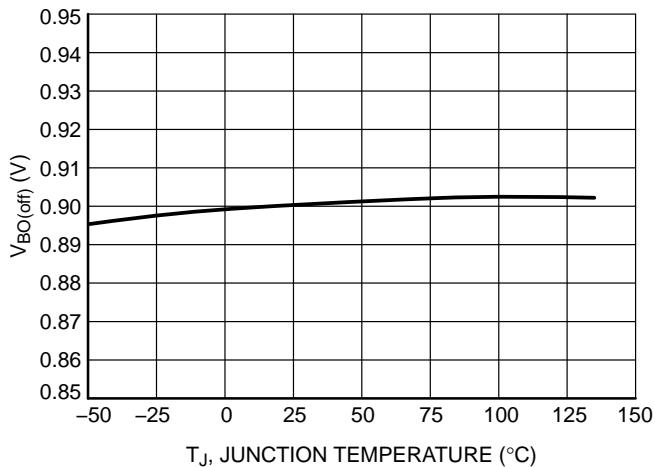
## TYPICAL CHARACTERISTICS

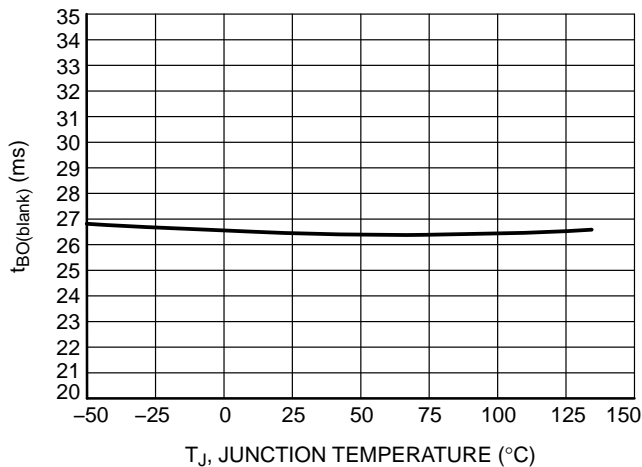Figure 56. Brown–out OFF Level vs. Temperature

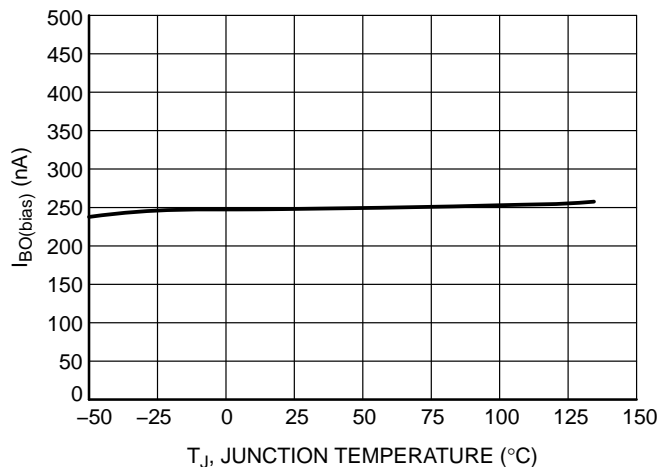Figure 57. Brown–out Blanking Time vs. Temperature

Figure 58. $V_S$ Pin Pulling–down Current vs. Temperature

# NCL30086BH

## Application Information

The NCL30086BH is a driver for power−factor corrected flyback and non−isolated buck−boost/ SEPIC converters. It implements a current−mode, quasi−resonant architecture including valley lockout and frequency fold−back capabilities for maintaining high−efficiency performance over a wide load range. A proprietary circuitry ensures both accurate regulation of the output current (without the need for a secondary−side feedback) and near−unity power factor correction. The circuit contains a suite of powerful protections to ensure a robust LED driver design without the need of extra external components or overdesign

- **Quasi−Resonance Current−Mode Operation:** implementing quasi−resonance operation in peak current−mode control, the NCL30086BH optimizes the efficiency by turning on the MOSFET when its drain−source voltage is minimal (valley). In light−load conditions, the circuit changes valleys to reduce the switching losses. For a stable operation, the valley at which the MOSFET switches on remains locked until the input voltage or the output current set−point significantly changes.
- **Primary−Side Constant−Current Control with Power Factor Correction:** a proprietary circuitry allows the LED driver to achieve both near−unity power factor correction and accurate regulation of the output current without requiring any secondary−side feedback (no optocoupler needed). A power factor as high as 0.99 and an output current deviation below ±2% are typically obtained.
- **Linear or PWM dimming:** the DIM pin allows implementing both analog and PWM dimming.
- **Main protection features:**
  - **Over Temperature Thermal Fold−back/ Shutdown/Over Voltage Protection:** the NCL30086BH features a gradual current foldback to protect the driver from excessive temperature down to 50% of the programmed current. If the temperature continues to rise after this point to a second level, the controller stops operating. This mode would only be expected to be reached under normal conditions if there is a severe fault. The first

and second temperature thresholds depend on the NTC connected to the circuit SD pin. The SD pin can also be used to shutdown the device by pulling this pin below the $V_{OTP(off)}$ min level. A Zener diode can also be used to pull−up the pin and stop the controller for adjustable OVP protection. When triggered, both protections lead the controller to stop operating for the 4−s auto−recovery time.
  - **Cycle−by−cycle peak current limit:** when the current sense voltage exceeds the internal threshold $V_{ILIM}$, the MOSFET is immediately turned off.
  - **Winding or Output Diode Short−Circuit Protection:** an additional comparator senses the CS signal and stops the controller for the 4−s auto−recovery time if it exceeds 150% x VILIM for 4 consecutive cycles. This feature can protect the converter if a winding is shorted or if the output diode is shorted or simply if the transformer saturates.
  - **Output Short−circuit protection:** if the ZCD pin voltage remains low for a 90−ms time interval, the controller detects that the output or the ZCD pin is grounded and hence, stops operation for the 4−s auto−recovery time.
  - **Open LED protection:** if the $V_{CC}$ pin voltage exceeds the OVP threshold, the controller shuts down and waits 4 seconds before restarting switching operation.
  - **Floating or Short Pin Detection:** NCL30086BH protections aid in pass safety tests. For instance, the circuit stops operating when the CS pin is grounded or open.

### Power Factor and Constant Current Control

The NCL30086BH embeds an analog/digital block to control the power factor and regulate the output current by monitoring the ZCD, $V_S$ and CS pin voltages (signals ZCD, $V_S$ and $V_{CS}$ of Figure 59). This circuitry generates the current setpoint ($V_{CONTROL}/4$) and compares it to the current sense signal ($V_{CS}$) to dictate the MOSFET turning off event when $V_{CS}$ exceeds $V_{CONTROL}/4$.
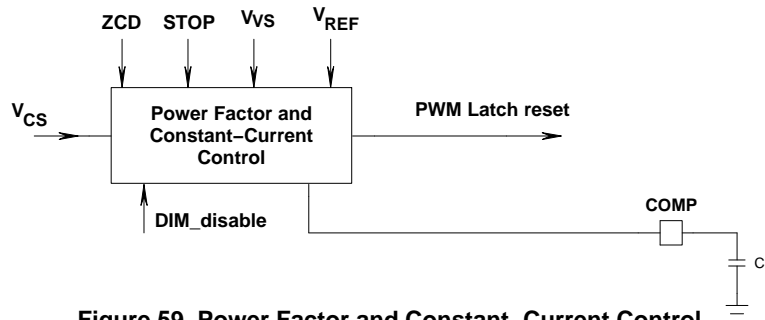


**Figure 59. Power Factor and Constant−Current Control**

The $V_S$ pin provides the sinusoidal reference necessary for shaping the input current. The obtained current reference is further modulated so that when averaged over a half–line period, it is equal to the output current reference ($V_{REFX}$). This averaging process is made by an internal Operational Trans–conductance Amplifier (OTA) and the capacitor connected to the COMP pin (C1 in Figure 59). Typical COMP capacitance is 2.2 μF and should not be less than 1 μF to ensure stability. The COMP ripple does not affect the power factor performance as the circuit digitally eliminates it when generating the current setpoint.

If the $V_S$ pin properly conveys the sinusoidal shape, power factor will be close to 1. Also, the Total Harmonic Distortion (THD) will be low, especially if the output voltage ripple is small. In any case, the output current will be well regulated following the equation below:

$$I_{out} = \frac{V_{REFX}}{2N_{PS}R_{sense}} \qquad \text{(eq. 1)}$$

Where:

- $N_{PS}$ is the secondary to primary transformer turns $N_{PS} = N_S / N_P$
- $R_{sense}$ is the current sense resistor (see Figure 1).
- $V_{REFX}$ is the output current internal reference. $V_{REFX} = V_{REF}$ (250 mV, typically) at full load.

The output current reference ($V_{REFX}$) is $V_{REF}$ unless thermal fold–back is activated by the SD pin voltage being reduced below 1 V typical (see "protections" section) or unless the DIM pin voltage is below $V_{DIM100}$ (see analog dimming section).

If a major fault is detected, the circuit enters the latched–off or auto–recovery mode and the COMP pin is grounded (except in an UVLO condition). This ensures a clean start–up when the circuit resumes operation.

**Start–up Sequence**

Generally an LED lamp is expected to emit light in < 1 sec and typically within 300 ms. The start–up phase consists of the time to charge the $V_{CC}$ capacitor, initiate startup and begin switching and the time to charge the output capacitor until sufficient current flows into the LED string. To speed–up this phase, the following defines the start–up sequence:

- The COMP pin is grounded when the circuit is off. The average COMP voltage needs to exceed the $V_S$ pin peak value to have the LED current properly regulated (whatever the current target is). To speed–up the COMP capacitance charge and shorten the start–up phase, an internal 80–μA current source adds to the OTA sourced current (60 μA max typically) to charge up the COMP capacitance. The 80–μA current source remains on until the OTA starts to sink current as a result of the COMP pin voltage sufficient rise. At that moment, the COMP pin being near its steady–state value, it is only driven by the OTA.
- If $V_{CC}$ drops below the $V_{CC(off)}$ threshold because the circuit fails to start–up properly on the first attempt, a new attempt takes place as soon as $V_{CC}$ is recharged to $V_{CC(on)}$. The COMP voltage is not reset at that moment. Instead, the new attempt starts with the COMP level obtained at the end of the previous operating phase.
- If the load is shorted, the circuit will operate in hiccup mode with $V_{CC}$ oscillating between $V_{CC(off)}$ and $V_{CC(on)}$ until the AUX_SCP protection trips (AUX_SCP is triggered if the ZCD pin voltage does not exceed 1 V within a 90–ms operation period of time thus indicating a short to ground of the ZCD pin or an excessive load preventing the output voltage from rising). The AUX_SCP protection forces the 4–s auto–recovery delay to reduce the operation duty–ratio. Figure 60 illustrates a start–up sequence with the output shorted to ground.
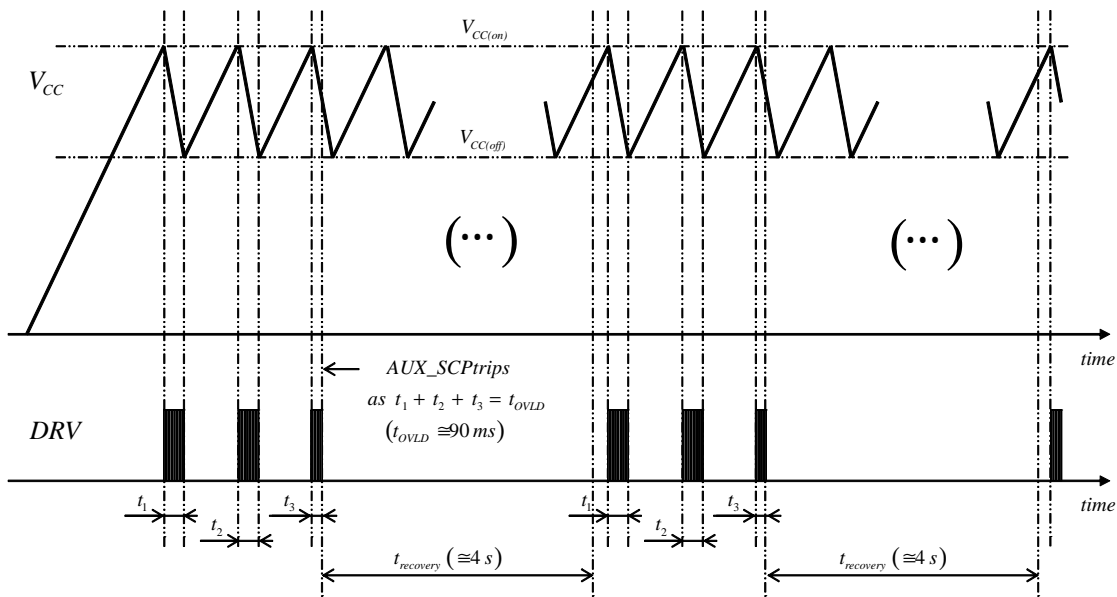
**Figure 60. Start−up Sequence in a Load Short−circuit Situation**

## Zero Crossing Detection Block

The ZCD pin detects when the drain−source voltage of the power MOSFET reaches a valley by crossing below the 55−mV internal threshold ($V_{ZCD(TH)}$). At startup or in case of extremely damped free oscillations, the ZCD comparator may not be able to detect the valleys. To avoid such a situation, the NCL30086BH features a time−out circuit that generates pulses if the voltage on ZCD pin stays below the 55−mV threshold for 6.5 μs nominal. The time−out also acts as a substitute clock for the valley detection and simulates a missing valley in case the free oscillations are too damped.
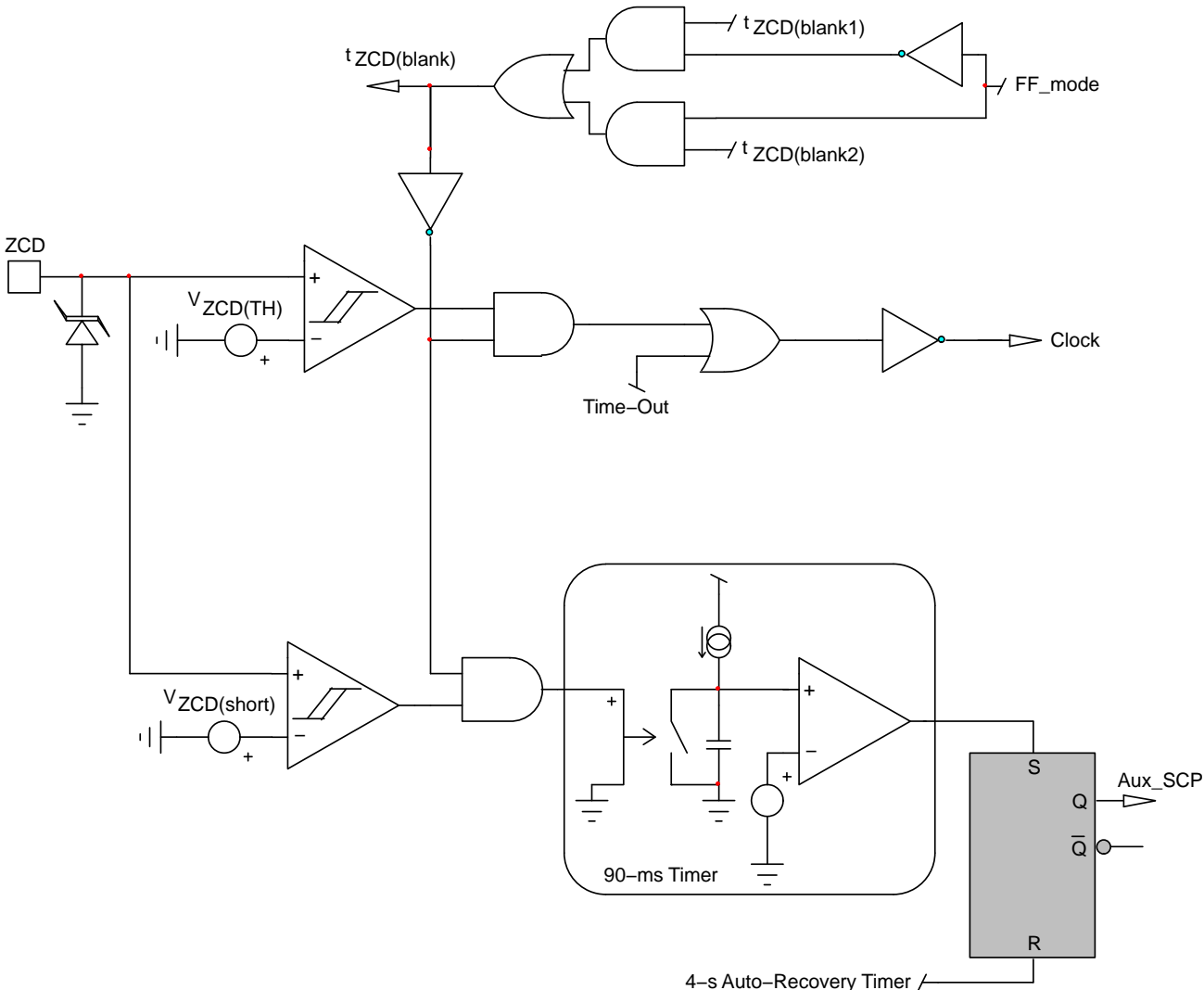
**Figure 61. Zero Current Detection Block**

If the ZCD pin or the auxiliary winding happen to be shorted, the time−out function would normally make the controller keep switching and hence lead to improper LED current value. The "AUX_SCP" protection prevents such a stressful operation: a secondary timer starts counting that is only reset when the ZCD voltage exceeds the $V_{ZCD(short)}$ threshold (1 V typically). If this timer reaches 90 ms (no ZCD voltage pulse having exceeded $V_{ZCD(short)}$ for this time period), the controller detects a fault and stops operation for 4 seconds.

The "clock" shown in Figure 61 is used by the "valley selection frequency foldback" circuitry of the block diagram (Figure 3), to generate the next DRV pulse (if no fault prevents it):

- Immediately when the clock occurs in QR mode at low line or valley 2 at high line (full load)

- After the appropriate number of "clock" pulses in thermal foldback or dimming mode

**For an optimal operation, the maximum ZCD level should be maintained below 5 V to stay safely below the built in clamping voltage of the pin.**

### Line Range Detection

As sketched in Figure 62, this circuit detects the low−line range if the $V_S$ pin remains below the $V_{LL}$ threshold (2.3 V typical) for more than the 25−ms blanking time. High−line is detected as soon as the $V_S$ pin voltage exceeds $V_{HL}$ (2.4 V typical). These levels roughly correspond to 184−V rms and 192−V rms line voltages if the external resistors divider applied to the $V_S$ pin is designed to provide a 1−V peak value at 80 V rms.
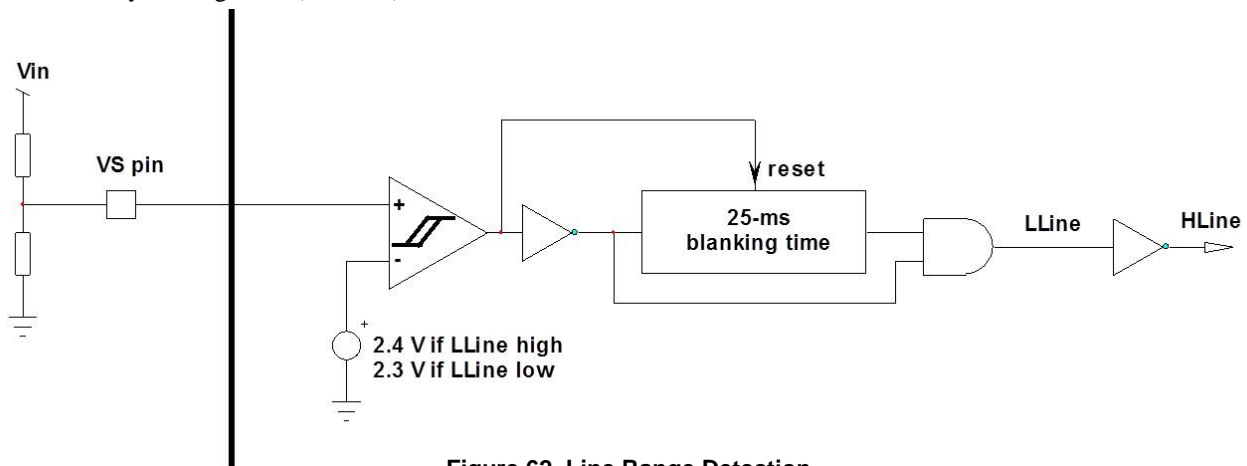


**Figure 62. Line Range Detection**

In the low−line range, conduction losses are generally dominant. Adding a dead−time would further increase these losses. Hence, only a short dead−time is necessary to reach the MOSFET valley. In high−line conditions, switching losses generally are the most critical. It is thus efficient to skip one valley to lower the switching frequency. Hence, under normal operation, the NCL30086BH optimizes the efficiency over the line range by turning on the MOSFET at the first valley in low−line conditions and at the second valley in the high−line case. This is illustrated by Figure 63 that sketches the MOSFET Drain−Source voltage in both cases. In the event that thermal foldback is activated, additional valleys can be skipped as the power is reduced.



**Figure 63. Full−load Operation – Quasi−resonant Mode in low line (left), turn on at valley 2 when in high line (right)**

### Line Feedforward

To compensate for current regulation errors due to AC line variation, the NCL30086BH includes a method to add line feedforward adjustment. As illustrated by Figure 64, the input voltage is sensed by the $V_S$ pin and converted into a current. By adding an external resistor in series between the sense resistor and the CS pin, a voltage offset proportional to the input voltage is added to the CS signal for the MOSFET on−time.
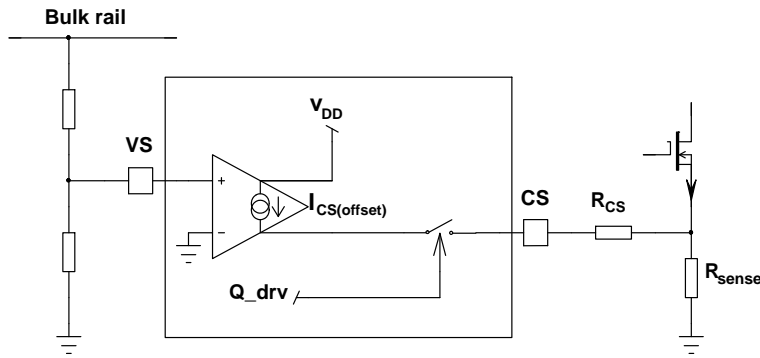
**Figure 64. Line Feed−Forward Schematic**

In Figure 64, Q_drv designates the output of the PWM latch which is high for the on−time and low otherwise.

## PWM or Linear Dimming Detection

The DIM pin of the NCL30086BH is provided to implement linear and/or PWM dimming of the LED current.

Applying a voltage on the DIM pin voltage ($V_{DIM}$) forces the output current internal reference to operate in one of three regions:

$$V_{REFX} = 0 \qquad \text{if } V_{DIM} \leq V_{DIM0} \qquad \text{(eq. 2)}$$

$$V_{REFX} = V_{REF} \qquad \text{if } V_{DIM} \geq V_{DIM100}$$

$$V_{REFX} = \frac{V_{DIM} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} V_{REF} \qquad \text{otherwise}$$

$V_{DIM0}$ and $V_{DIM100}$ respectively, are 0.7 V and 2.45 V typically.

The output current can then be controlled by the DIM pin as follows:

$$I_{out} = 0 \qquad \text{if } V_{DIM} \leq V_{DIM0} \quad \text{(eq. 3)}$$

$$I_{out} = I_{out,nom} = \frac{V_{REF}}{2 N_{PS} R_{sense}} \quad \text{if } V_{DIM} \geq V_{DIM100}$$

$$I_{out} = \frac{V_{DIM} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} I_{out,nom} \qquad \text{otherwise}$$

Where:
- $N_{PS}$ is the secondary to primary transformer turns
  $$N_{PS} = N_S/N_P$$
- $R_{sense}$ is the current sense resistor (see Figure 1).
- $V_{REF}$ is the output current internal reference (250 mV typically)
- $I_{out,nom}$ is the full−load output current.

The DRV output is disabled whenever the DIM pin voltage is lower than $V_{DIM0}$ and the output current setpoint is maximal when $V_{DIM}$ exceeds $V_{DIM100}$. Thus, for PWM dimming, a PWM signal with a low−state value below $V_{DIM0}$ and a high−state value above $V_{DIM100}$ should be applied.

In this case, the output current will be:

$$I_{out} \cong I_{out,nom} \cdot d \qquad \text{(eq. 4)}$$
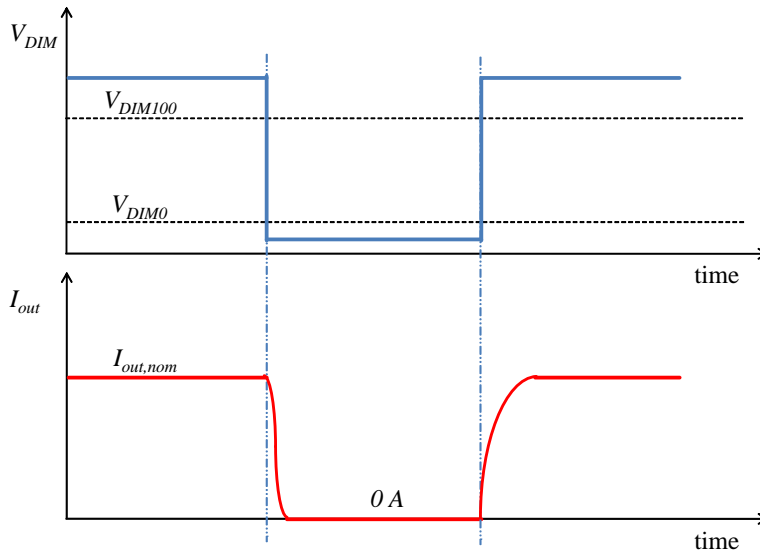
Where d is the duty ratio of the DIM pin signal.



**Figure 65. Pin DIM Chronograms**

*Notes*:

- The current does not immediately reach its new target value when the PWM dimming signal state changes due to system time constants like the time necessary to charge or discharge the output capacitor to the required level. The output current settling time can hence affect the obtained output current, particularly if the PWM signal frequency is high.

- If either the high−state ($V_{DIM(high)}$) or low−state level ($V_{DIM(low)}$) of the input or both are between $V_{DIM0}$ and $V_{DIM100}$, the output current will be proportionally reduced as both analog and PWM dimming are simultaneous active, thus the output current will be:

$$I_{out} \cong \left( \frac{V_{DIM(high)} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} d + \frac{V_{DIM(low)} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} (1 - d) \right) I_{out,nom} \text{ if } V_{DIM0} \leq V_{DIM(low)} \leq V_{DIM(high)} \leq V_{DIM100}$$

$$I_{out} \cong \frac{V_{DIM(high)} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} d \cdot I_{out,nom} \qquad \text{if } V_{DIM0} \leq V_{DIM(high)} \leq V_{DIM100} \text{ and } V_{DIM(low)} \leq V_{DIM0}$$

$$I_{out} \cong \left( d + \frac{V_{DIM(low)} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} (1 - d) \right) I_{out,nom} \qquad \text{if } V_{DIM(high)} \geq V_{DIM100} \text{ and } V_{DIM0} \leq V_{DIM(low)} \leq V_{DIM100}$$

- If thermal foldback is activated as well, the current reduction is cumulative. For instance, if the DIM pin voltage and the thermal foldback respectively, reduces the output current setpoint by 50% and 20% respectively, the output current will be 80%*50% that is 40% of its nominal level.

The DIM pin is pulled up internally by a 10−μA current source. Thus, if the pin is let open, the controller is able to start.

For any power factor corrected single stage architecture there will be a component of line ripple (100 / 120 Hz) on the output. If PWM dimming is used, it is recommended to select the dimming frequency to be sufficiently high not to generating beat frequencies that could create optical artifacts.

**>> As a general rule, the minimum PWM frequency should be at least 2.5x the line ripple frequency and not be set near multiples of the line frequency.**

## Protections

The circuit incorporates a full suite of protection features listed below to make the LED driver very rugged.

### Output Short Circuit Situation

An overload fault is detected if the ZCD pin voltage remains below $V_{ZCD(short)}$ for 90 ms. In such a situation, the circuit stops generating pulses until the 4−s delay auto−recovery time has elapsed.

### Winding or Output Diode Short Circuit Protection

If a transformer winding happens to be shorted, the primary inductance will collapse leading the current to ramp up in a very abrupt manner. The $V_{ILIM}$ comparator (current limitation threshold) will trip to open the MOSFET and eventually stop the current rise. However, because of the abnormally steep slope of the current, internal propagation delays and the MOSFET turn−off time, a current rise > 50% of the nominal maximum value set by $V_{ILIM}$ is possible. As illustrated in Figure 66, an additional circuit monitors for this current overshoot to detect a winding short circuit. The leading edge blanking (LEB) time for short circuit protection (LEB2) is significantly faster than the LEB time for cycle−by−cycle protection (LEB1). Practically, if four consecutive switching periods lead the CS pin voltage to exceed ($V_{CS(stop)} = 150\% * V_{ILIM}$), the controller enters the auto−recovery mode (4−s operation interruption between active bursts.)
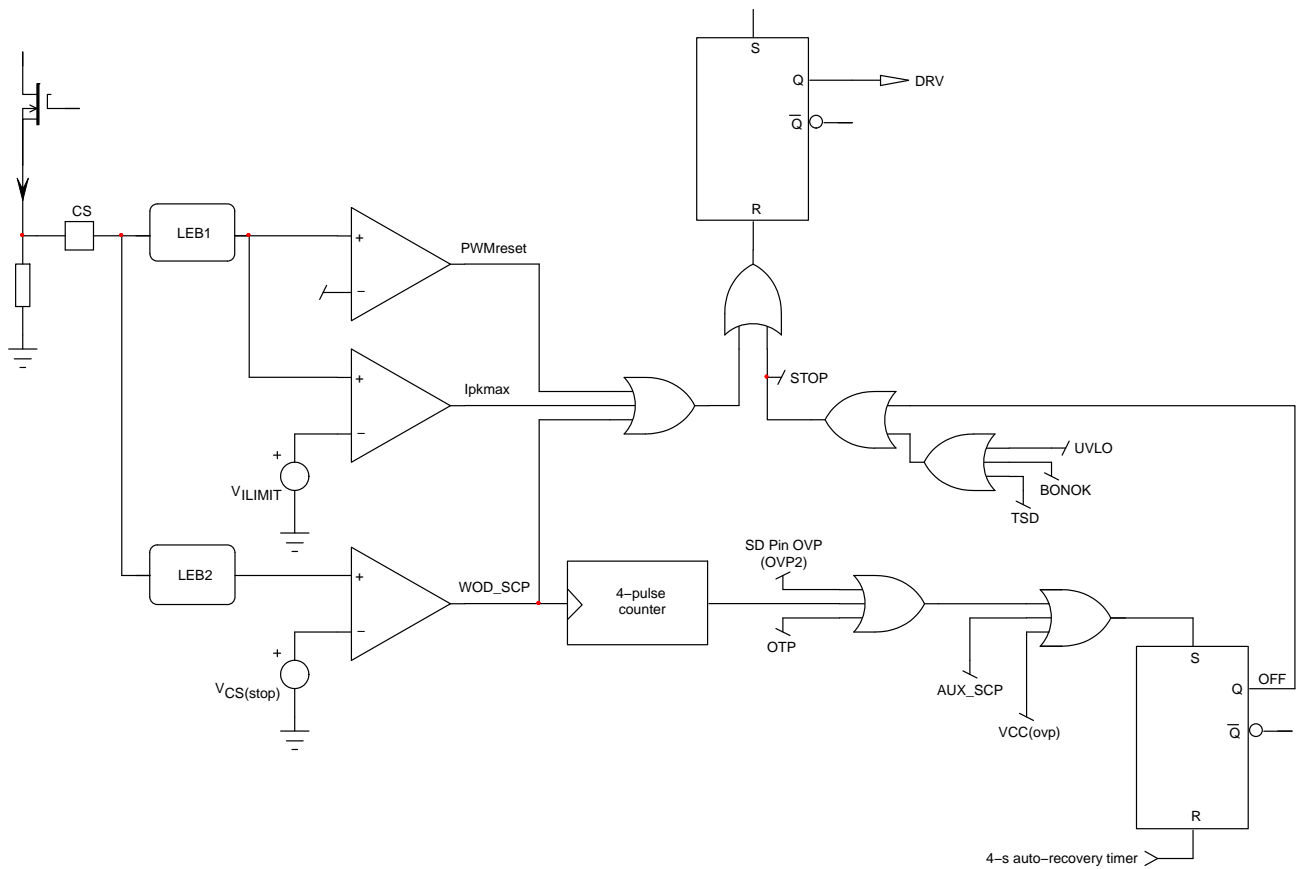
**Figure 66. Winding Short Circuit Protection, Max. Peak Current Limit Circuits**

**$V_{CC}$ Over Voltage Protection**

The circuit stops generating pulses if $V_{CC}$ exceeds $V_{CC(OVP)}$ and enters auto–recovery mode. This feature protects the circuit in the event that the output LED string is disconnected or an individual LED in the string happens to fail open.

**Programmable Over Voltage Protection (OVP2)**

In addition to the $V_{CC}$ OVP protection, it is possible to connect a Zener diode between $V_{CC}$ and the SD pin to implement programmable $V_{CC}$ OVP monitoring ($D_Z$ of Figure 67). The triggering level is ($V_Z + V_{OVP}$) where $V_{OVP}$ is the 2.5–V internal threshold. If this protection trips, the circuit enters the auto–recovery mode.
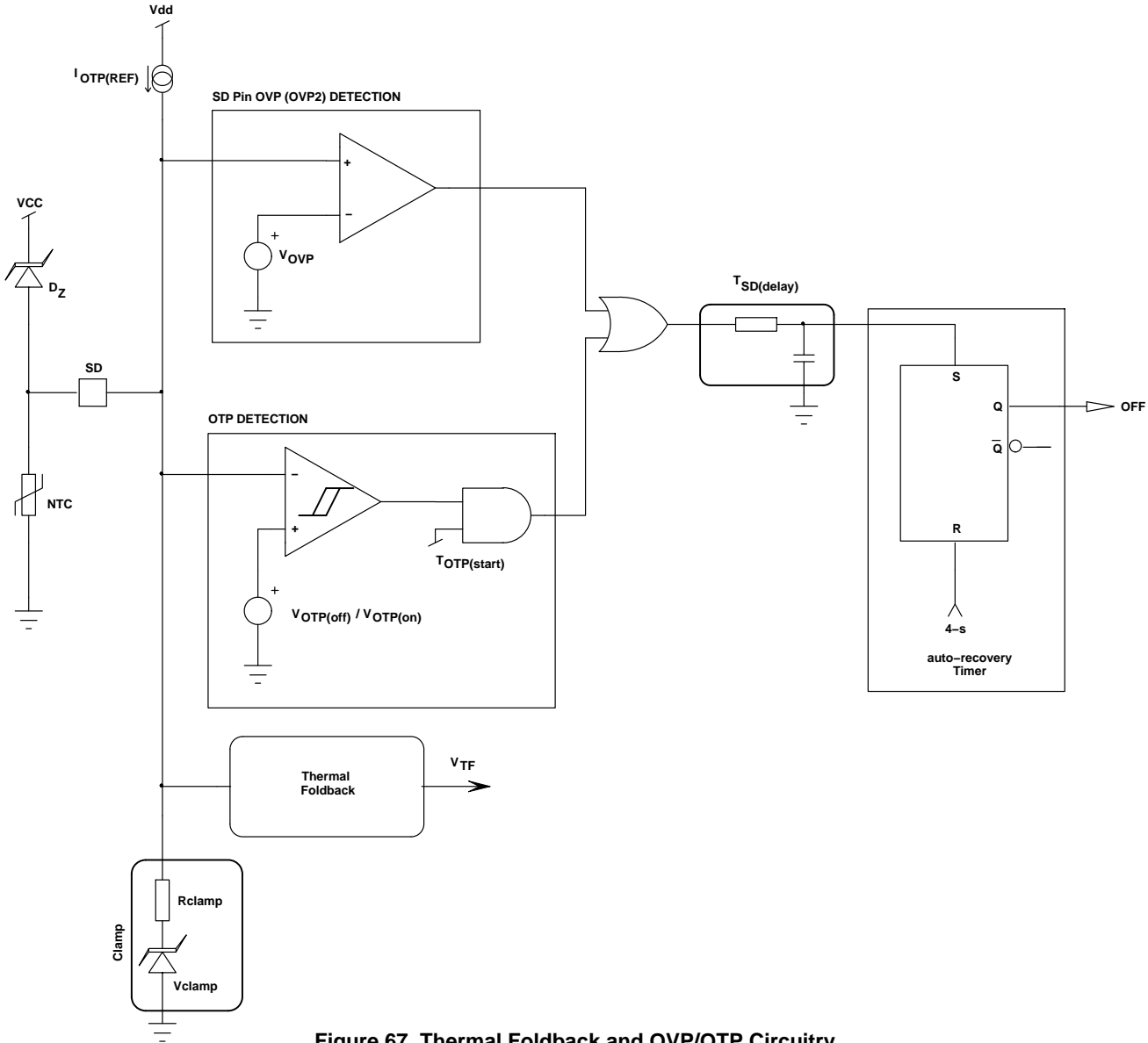
**Figure 67. Thermal Foldback and OVP/OTP Circuitry**

The SD pin is clamped to about 1.35 V ($V_{clamp}$) through a 1.6–kΩ resistor ($R_{clamp}$). It is then necessary to inject about

$$\left( \frac{V_{OVP} - V_{clamp}}{R_{clamp}} \right)$$

that is

$$\left( \frac{2.50 - 1.35}{1.6 \ k} \cong 700 \ \mu A \right)$$

typically, to trigger the OVP protection. This current helps ensure an accurate detection by using the Zener diode far from its knee region.

### Programmable Over Temperature Foldback Protection (OTP)

Connect an NTC between the SD pin and ground to detect an over–temperature condition. In response to a high temperature (detected if $V_{SD}$ drops below $V_{TF(start)}$), the circuit gradually reduces the LED current down to 50% (> 50% reduction in output power) of its initial value when $V_{SD}$ reaches $V_{TF(stop)}$, in accordance with the characteristic of Figure 68 (Note 9).

At this point, if the temperature continues to rise and the secondary OTP level is reached, ($V_{SD}$ drop below $V_{OTP}$), the circuit enters auto–recovery mode and cannot resume operation until $V_{SD}$ exceeds $V_{OTP(on)}$ to provide some temperature hysteresis (around 10°C typically). The OTP thresholds nearly correspond to the following resistances of the NTC:

- Thermal foldback starts when $R_{NTC} \le R_{TF(start)}$ (11.7 kΩ, typically)
- Thermal foldback stops when $R_{NTC} \le R_{TF(stop)}$ (8.0 kΩ, typically)
- OTP triggers when $R_{NTC} \le R_{OTP(off)}$ (5.9 kΩ, typically)
- OTP is removed when $R_{NTC} \le R_{OTP(on)}$ (8.0 kΩ, typically)
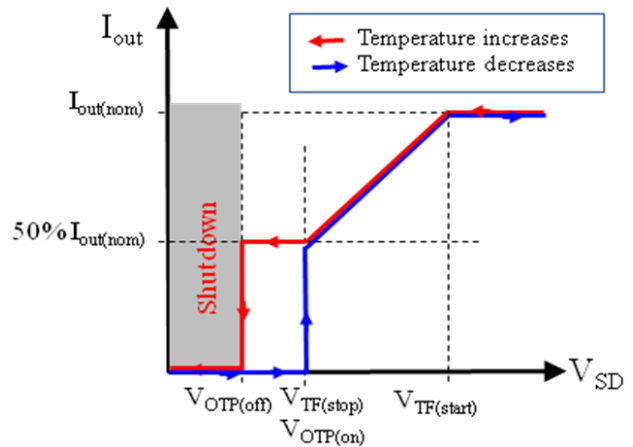


**Figure 68. Output Current Reduction versus SD Pin Voltage**

At startup, when $V_{CC}$ reaches $V_{CC(on)}$, the OTP comparator is blanked for at least 180 μs which allows the SD pin voltage to reach its nominal value if a filtering capacitor is connected to the SD pin. This avoids flickering of the LED light during turn on.

### Brown–Out Protection

The NCL30086BH prevents operation when the line voltage is too low for proper operation. As sketched in Figure 69, the circuit detects a brown–out situation if the $V_S$ pin remains below the $V_{BO(off)}$ threshold (0.9 V typical) for more than the 25–ms blanking time. In this case, the controller stops operating. Operation resumes as soon as the $V_S$ pin voltage exceeds $V_{BO(on)}$ (1.0 V typical) and $V_{CC}$ is higher than $V_{CC(on)}$. To ease recovery, the circuit overrides the $V_{CC}$ normal sequence (no need for $V_{CC}$ cycling down below $V_{CC(off)}$). Instead, its consumption immediately reduces to $I_{CC(start)}$ so that $V_{CC}$ rapidly charges up to $V_{CC(on)}$ and the circuit re–starts operation.
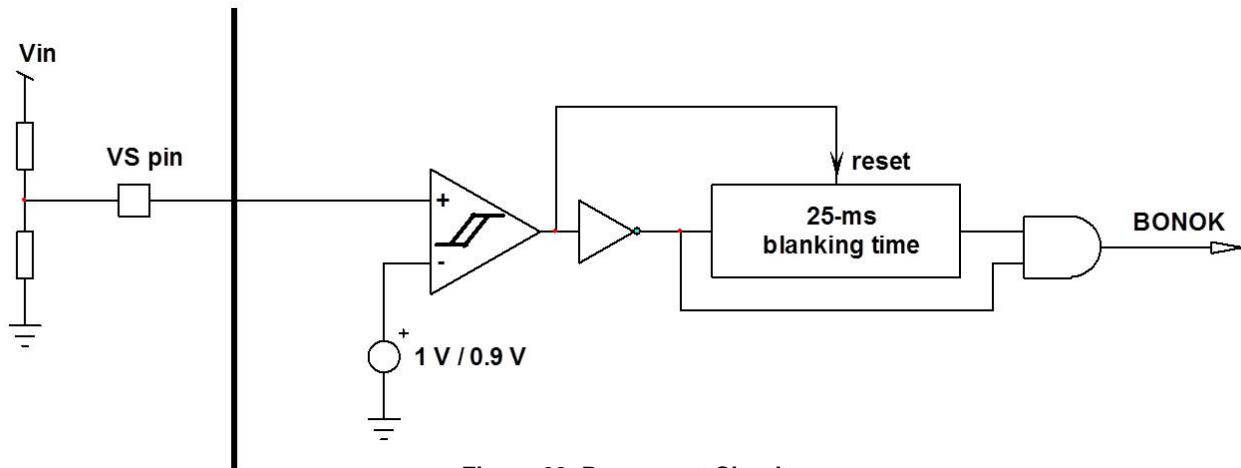


**Figure 69. Brown–out Circuit**

9. The above mentioned initial value is the output current before the system enters the thermal foldback, that is, its maximum level if PWM or analog dimming is not engaged or a lower one based on the dimming value.

**Die Over Temperature (TSD)**

The circuit stops operating if the junction temperature ($T_J$) exceeds 150°C typically. The controller remains off until $T_J$ goes below nearly 100°C.

**Pin Connection Faults**

The circuit addresses most pin connection fault cases:

- **CS Pin Short to Ground**

  The circuit senses the CS pin impedance every time it starts−up and after DRV pulses terminated by the 36−μs maximum on−time. If the measured impedance does not exceed 120 Ω typically, the circuit stops operating. In practice, it is recommended to place a minimum of 250 Ω in series between the CS pin and the current sense resistor to take into account parasitics.

- **Fault of the GND Connection**

  If the GND pin is properly connected, the supply current drawn from the positive terminal of the $V_{CC}$ capacitor, flows out of the GND pin to return to the negative terminal of the $V_{CC}$ capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non−connection of the GND pin is monitored by detecting that one of the ESD diode is conducting. Practically, the ESD diode of CS pin is monitored. If such a fault is detected for 200 μs, the circuit stops generating DRV pulses.

**More generally, incorrect pin connection situations (open, grounded, shorted to adjacent pin) are covered by ANDxxxx.**

**Fault Management**

*OFF Mode*

The circuit turns off in the case of an incorrect feeding of the circuit: "UVLO high". The UVLO signal becomes high when VCC drops below VCC(off) and remains high until VCC exceeds VCC(on).

The circuit also turns off whenever a major faulty condition prevents it from operating:

- Severe OTP ($V_{SD}$ level below $V_{OTP(off)}$)
- $V_{CC}$ OVP
- OVP2 (additional OVP provided by SD pin)
- Output diode short circuit protection: "WOD_SCP high"
- Output / Auxiliary winding Short circuit protection: "Aux_SCP high"
- Die over temperature (TSD)

In this mode, the DRV pulses generation is interrupted.

In the case of a latching−off fault, the circuit stops pulsing until the LED driver is unplugged and $V_{CC}$ drops below $V_{CC(reset)}$. At that moment, the circuit resumes operation.

In the auto−recovery case, the circuit cannot generate DRV pulses for the auto−recovery 4−s delay. When this time has elapsed, the circuit recovers operation as soon as the $V_{CC}$ voltage has exceeded $V_{CC(on)}$. All these protections are auto−recovery.

## ORDERING INFORMATION

| Device | Package Type | Shipping |
|---|---|---|
| NCL30086BHDR2G | SOIC−8 (Pb−Free/Halide Free) | 2500 / Tape & Reel |

**SOIC−10 NB**
CASE 751BQ
ISSUE B

DATE 26 NOV 2013

10

1

**SCALE 1:1**

2X
△ | 0.10 | C | A−B

D

D | A

2X
△ | 0.10 | C | A−B

F

10    6

H

E

1    5

△ | 0.20 | C

**2X 5 TIPS**

B

10X b

⊕ | 0.25 Ⓜ | C | A−B | D
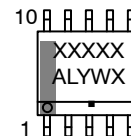
**TOP VIEW**

L2

A3

L

SEATING
PLANE

C

**DETAIL A**
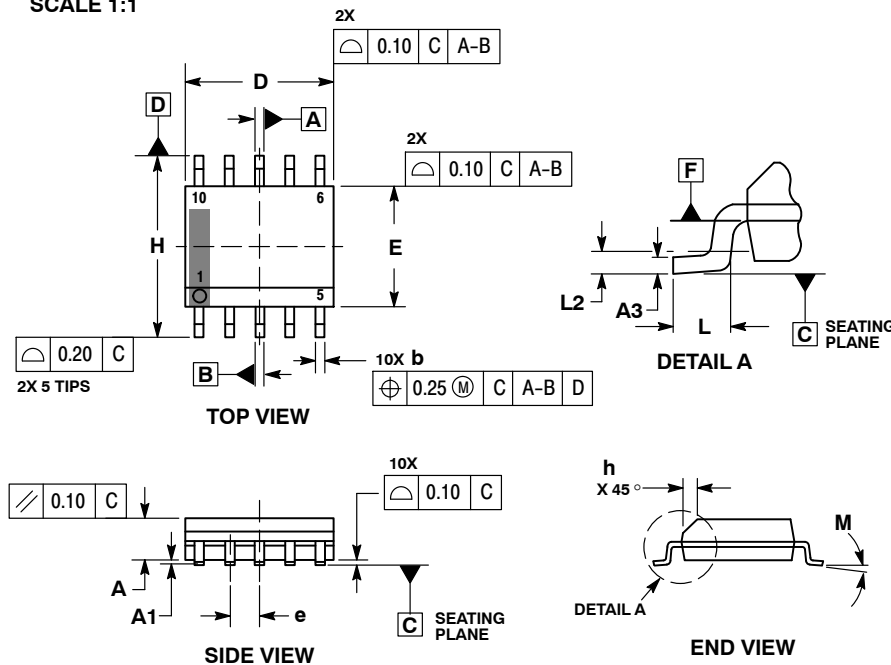
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DE-TERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERM-INED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | |
| --- | --- | --- |
| | **MIN** | **MAX** |
| A | 1.25 | 1.75 |
| A1 | 0.10 | 0.25 |
| A3 | 0.17 | 0.25 |
| b | 0.31 | 0.51 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.00 BSC | |
| H | 5.80 | 6.20 |
| h | 0.37 REF | |
| L | 0.40 | 0.80 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |

10X
⫽ | 0.10 | C

△ | 0.10 | C

A

A1

e

SEATING
PLANE

C

**SIDE VIEW**

h

X 45°

M

DETAIL A

**END VIEW**

**RECOMMENDED
SOLDERING FOOTPRINT\***

10X 0.58

1.00
PITCH

6.50

10X 1.18

1

DIMENSION: MILLIMETERS
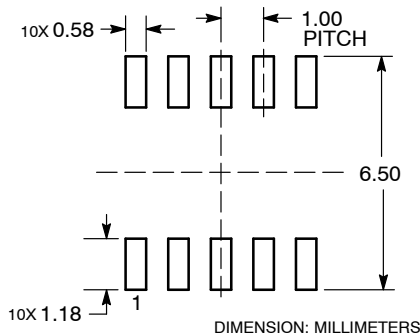
\*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM\***

10

XXXXX
ALYWX

1

XXXXX = Specific Device Code
A     = Assembly Location
L     = Wafer Lot
Y     = Year
W     = Work Week
▪      = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

## ADDITIONAL INFORMATION

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