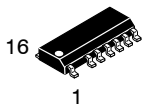
# LLC Converter Controller with HB Driver

# NCL30159AA




**SOIC−16 NB MISSING PINS 2 AND 13**
**CASE 751DU**

NCL 30159 is a primary side current mode LLC controller. The controller is eligible for lighting application with minimum external components. The control technique optimizes switching frequency depending on energy of resonant tank. This controller allows to implement many features (high efficiency in standby, open string protection, dedicated startup…). Also can provide wide dimming range operation in wide output condition. Housed in a SOIC−16 package it integrates half−bridge output drivers together with the primary current sensing.

High−Voltage section featuring the High−Voltage startup and Brown−out detection greatly simplifies the design of the power supply or LED string driver. Analog Dimming feature together with the PWM dimming allows to control the total light flux from the LED string this feature allows to design the window LED driver as well.

This controller allows to ensure the maximum power limit feature. This advantage is useful for designing the wide input voltage range converters or the LED drivers with their output matched to different LED strings.

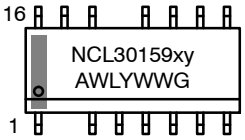
### Features

- Integrated High−Voltage Startup Circuit with Brownout Detection
- High−Frequency Operation from 20 kHz up to 750 kHz
- Current Mode Control Scheme
- Automatic Dead−time with Maximum Dead−time Clamp
- Over Current and Open String Protection
- Shorted LED String Protection
- Proprietary Skip Cycle in No−load Operation
- Dedicated Soft Start Sequence to Avoid Hard Switching
- This is a Pb−Free Device

### Applications

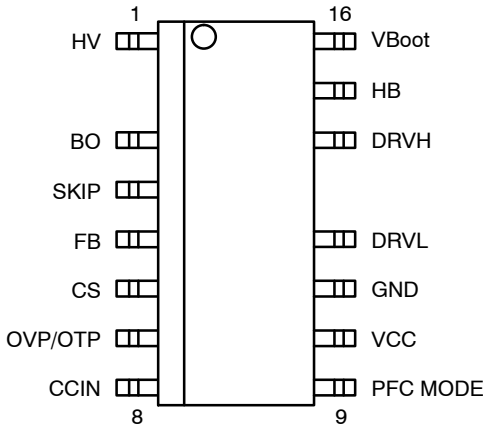
- Low Cost High Efficiency LED Lighting 50 ~ 300 W
- EV Battery Charger
- TV Set Power Supply

### MARKING DIAGRAM




| | |
|---|---|
| NCL30159xy | = Specific Device Code |
| xy | = Specific Device Option |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

### PIN CONNECTIONS




### ORDERING INFORMATION

See detailed ordering and shipping information on page 44 of this data sheet.

## TYPICAL APPLICATION EXAMPLE

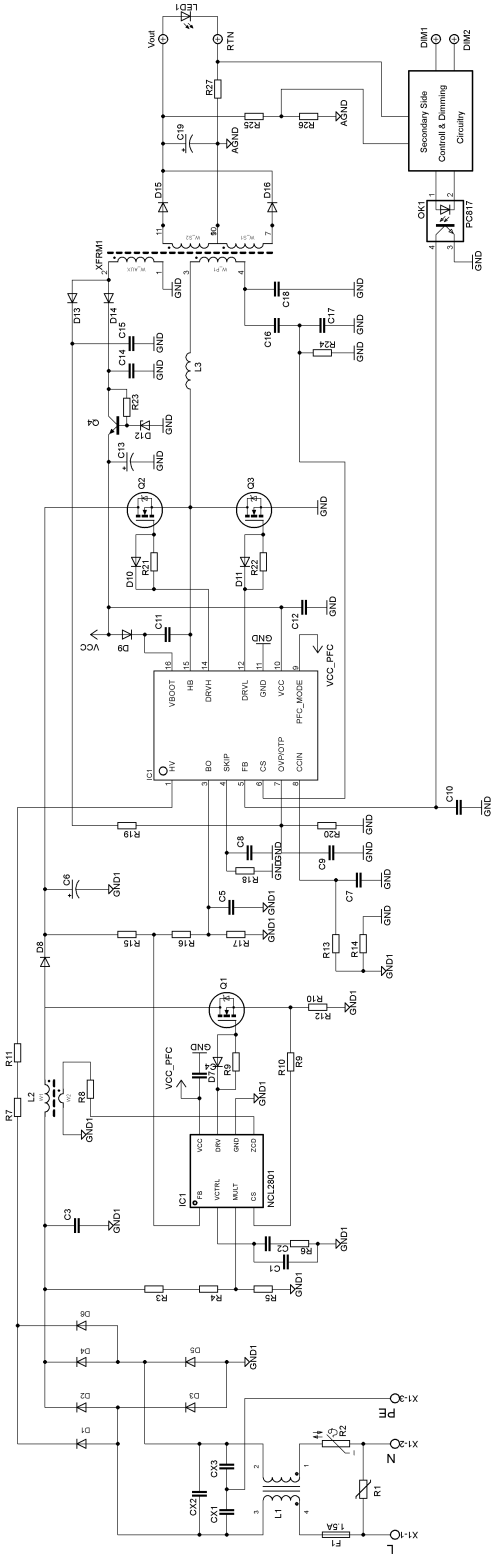



**Figure 1. LLC Converter Application Using the NCL30159**

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Function | Pin Description |
|---|---|---|---|
| 1 | HV | High−voltage start−up current source input | Connects to the rectified ac line or to bulk capacitor to perform the functions of start−up current source, Dynamic Self−Supply, AC brown−out detection. |
| − | − | Creepage distance | − |
| 3 | BO | Bulk voltage monitoring input | Receives divided bulk voltage to perform Brown−out protection. |
| 4 | SKIP | Skip threshold adjust | Sets the skip in threshold via a resistor connected to ground. |
| 5 | FB | Feedback input | Defines operating frequency based on given load conditions. Activate skipmode operation under light load conditions. |
| 6 | CS | Current sensing input | Senses divided resonant capacitor voltage to perform on−time modulation, out of resonant switching protection, over−over current protection and secondary side short circuit protection. |
| 7 | OVP/OTP | Over−temperature and over−voltage protection input | Implements over−temperature and over−voltage protection on single pin. |
| 8 | CCIN | Average current sensing input | Senses the voltage drop across the shunt resistor to provide the average input current input for maximum power limit. |
| 9 | PFC MODE | PFC and external HV switch output | Provides supply voltage for PFC front stage controller and/or enables Vbulk sensing network switch. |
| 10 | VCC | Supplies the controller | This supply pin accepts up to 40 Vdc, with overvoltage detection. The pin is connected to an external auxiliary voltage. |
| 11 | GND | The controller ground | Common ground connection for adjust components, sensing networks and DRV outputs. |
| 12 | DRVL | Low side driver output | The driver's output to an external low side MOSFET gate. It is clamped to a safe 12−V gate−source level. |
| − | − | Creepage distance | − |
| 14 | DRVH | High side driver output | The driver's output to an external high side MOSFET gate. It is clamped to a safe 12−V gate−source level. |
| 15 | HB | Half−bridge connection | Connects to the half−bridge output. |
| 16 | VBOOT | Bootstrap supply | The floating supply voltage for the upper stage. |

## SIMPLIFIED INTERNAL BLOCK SCHEMATIC

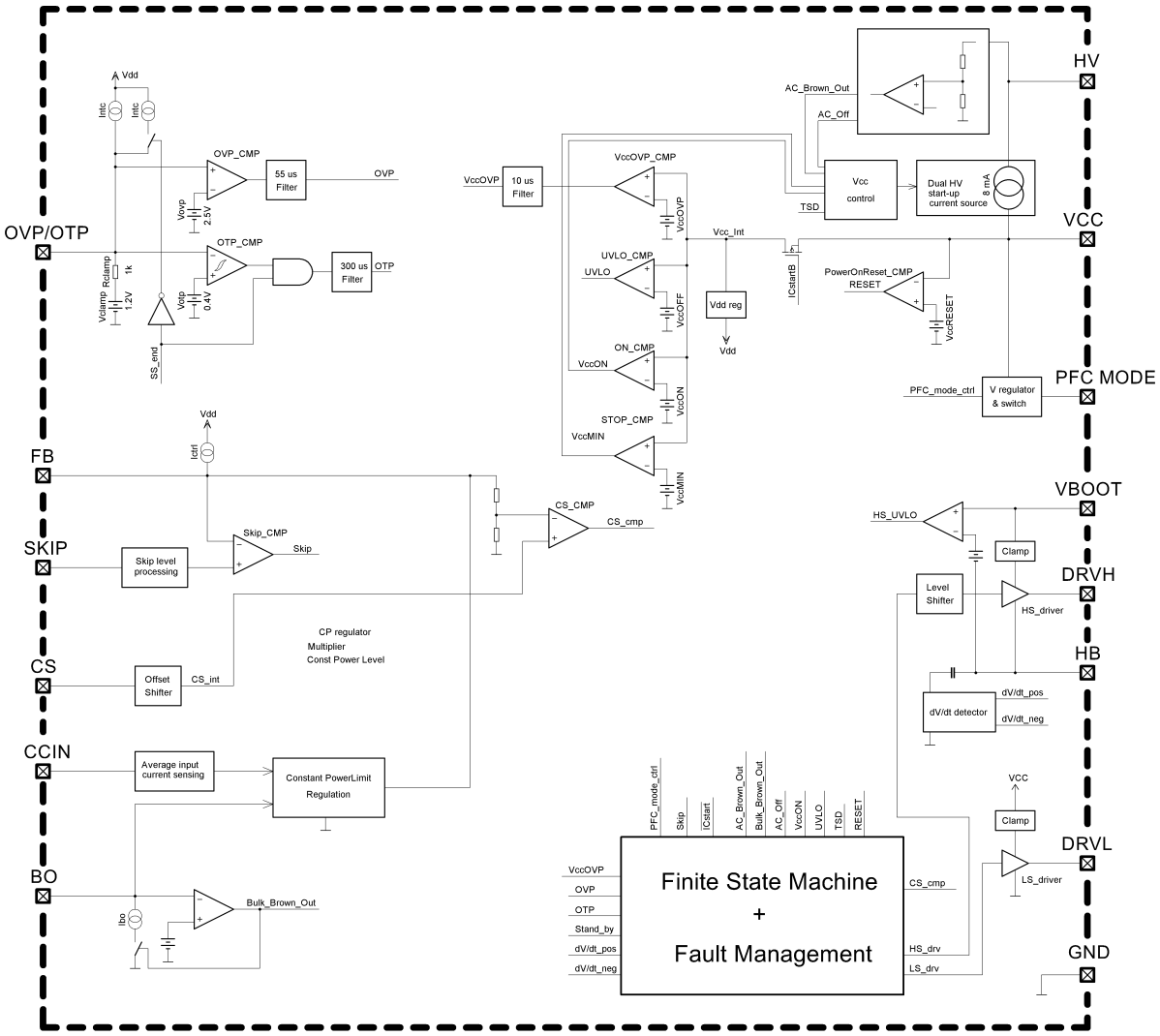



**Figure 2. Simplified Internal Block Schematic**

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{HV}$ | Maximum Voltage on HV/BO Pin (Pin 1)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 700<br>+20/−5 | V<br>mA |
| $V_{BO}$ | Maximum Voltage on BO Pin (Pin3)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 5.3<br>±10 (peak) | V<br>mA |
| $V_{SKIP}$ | Maximum Voltage on SKIP Pin (Pin 4)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 5.3<br>±10 (peak) | V<br>mA |
| $V_{FB}$ | Maximum Voltage on FB Pin (Pin 5)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 5.3<br>±10 (peak) | V<br>mA |
| $V_{CS}$ | Maximum Voltage on CS Pin (Pin 6)<br>(Dc−Current self−limited if operated within the allowed range) | −5.3 to 5.3<br>±10 (peak) | V<br>mA |
| $V_{CCIN}$ | Maximum Voltage on CCIN Pin (Pin 7)<br>(Dc−Current self−limited if operated within the allowed range) | −5.3 to 5.3<br>±10 (peak) | V<br>mA |
| $V_{OVP/OTP}$ | Maximum Voltage on OVP/OTP Pin (Pin 8)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 5.3<br>±10 (peak) | V<br>mA |
| $V_{PFC\ MODE}$ | Maximum Voltage on PFC MODE Pin (Pin 9)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to $V_{CC}$ + 0.3<br>+10/−30 (peak) | V<br>mA |
| $V_{CC}$ | $V_{CC}$ Power Supply Voltage, $V_{CC}$ pin, Continuous Voltage<br>Power Supply Voltage, $V_{CC}$ Pin, Continuous Voltage (Pin 10) | −0.3 to 40<br>+1000/−30 (peak) | V<br>mA |
| $V_{DRVL}$ | Maximum Low Side Driver Voltage on DRVL pin (Pin 12)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 20<br>±1000 (peak) | V<br>mA |
| $V_{DRVH}$ | Maximum High Side Driver Voltage on DRVH Pin (Pin 14)<br>(Dc−Current self−limited if operated within the allowed range) | $V_{HB}$ − 0.3 to $V_{HB}$ + 20 V<br>±1000 (peak) | V<br>mA |
| $V_{HB}$ | Allowable Negative Voltage on HB Pin @ $V_{CC}$ = 12 V; $V_{BOOT}$ = 12 V<br>(Dc−Current self−limited if operated within the allowed range) (Pin 15) | −10<br>−30 (peak) | V<br>mA |
| $dV_{HB}/dt$ | Allowable Slew Rate on HB pin (Pin 15) | 100 | V/ns |
| $V_{BOOT}$ | Maximum High Side Boot Voltage on VBoot Pin (Pin 16)<br>(Dc−Current self−limited if operated within the allowed range) | −0.3 to 740<br>±30 (peak) | V<br>mA |
| $V_{BOOT} - V_{HB}$ | High Side Floating Supply Voltage (Pin 16, 15) | −0.3 to 38.5<br>+1000/−30 (peak) | V<br>mA |
| $R_{\theta J-A}$ | Thermal Resistance Junction−to−Air | 130 | °C/W |
| $T_{JMAX}$ | Operating Junction Temperature | −40 to +150 | °C |
| $T_{STRGMAX}$ | Storage Temperature Range | −60 to +150 | °C |
| − | ESD Capability, HBM Model (Note 1) | >2000 | V |
| − | ESD Capability, Charge Discharge Model (Note 1) | >500 | V |
| $I_{LU}$ | Latch−up Current, per JEDEC Standard JESD78 | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC standard JESD22, Method A114E
   Charge Discharge Model Method 500 V per JEDEC standard JESD22, Method C101E

**ELECTRICAL CHARACTERISTICS** (For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, $V_{HV}$ = 125 V, Vcc = 12 V, $C_{DRVH}$ = $C_{DRVL}$ = 1 nF unless otherwise noted)

| Characteristics | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HIGH VOLTAGE CURRENT SOURCE** | | | | | | |
| Minimum Voltage for Current Source Operation | $V_{CC}$ = $V_{CC(on)}$ − 0.5 V | $V_{HV\_MIN}$ | − | 30 | 40 | V |
| Current Flowing Out of $V_{CC}$ Pin | $V_{CC}$ = 0 V<br>$V_{CC}$ = $V_{CC(on)}$ − 0.5 V | $I_{START1}$<br>$I_{START2}$ | 0.2<br>6 | 0.5<br>9 | 0.8<br>15 | mA |
| Off−state Leakage Current | $V_{HV}$ = 700 V | $I_{START\_OFF}$ | − | 8 | 15 | μA |
| **SUPPLY** | | | | | | |
| Turn−on Threshold Level, $V_{CC}$ Going Up<br>HV Current Source Stop Threshold − Optional | | $V_{CC\_ON}$ | 15.0 | 16.0 | 17.0 | V |
| Turn−off Threshold | | $V_{CC\_OFF}$ | 9.5 | 10 | 10.5 | V |
| Overvoltage Threshold | | $V_{CC\_OVP}$ | 36.4 | 38.3 | 39.8 | V |
| Blanking Duration on $V_{CC\_OFF}$ and $V_{CC\_OVP}$ Detection (Note 2) | | $t_{VCC\_BLANK}$ | − | 10 | − | μs |
| $V_{CC}$ Decreasing Level at Which the Internal Logic Resets | | $V_{CC\_RESET}$ | 6.4 | 7.0 | 7.6 | V |
| $V_{CC}$ Level for $I_{START1}$ to $I_{START2}$ Transition | | $V_{CC\_INHIBIT}$ | 1.0 | 2.0 | 3.0 | V |
| Internal Current Consumption (all IPT options setup) | Normal operation, $C_{DRVH}$ = $C_{DRVL}$ = 1 nF, $f_{SW}$ = 100 kHz, $V_{CC}$ = 15 V | $I_{CC\_OPERATION}$ | 1.7 | 3.2 | 4.2 | mA |
| | Light load operation, $C_{DRVH}$ = $C_{DRVL}$ = 1 nF, $f_{SW}$ = 100 kHz, $V_{CC}$ = 15 V | $I_{CC\_LIGHTLOAD}$ | 1.2 | 2.9 | 3.5 | mA |
| | Skip mode operation, $V_{CC}$ = 15 V | $I_{CC\_SKIP-MODE}$ | 0.4 | 1.8 | 2.2 | mA |
| | Fault mode (latch), $V_{CC}$ = $V_{CC\_ON}$ − 0.2 V | $I_{CC\_LATCH}$ | 40 | 95 | 200 | μA |
| | Fault mode (autorecovery), $V_{CC}$ = $V_{CC\_ON}$ − 0.2 V | $I_{CC\_AUTOREC}$ | 40 | 95 | 200 | μA |
| | Off mode, $V_{CC}$ = $V_{CC\_ON}$ − 0.2 V | $I_{CC\_OFF-MODE}$ | 20 | 105 | 150 | μA |

2. Guaranteed by design.

| | | | | | | |
|---|---|---|---|---|---|---|
| **BOOTSTRAP SECTION** | | | | | | |
| Start−up Voltage on the Floating Section | $V_{BOOT}$ − $V_{HB}$ | $V_{BOOT\_ON}$ | 9.1 | 9.7 | 10.2 | V |
| Cut−off Voltage on the Floating Section | $V_{BOOT}$ − $V_{HB}$ | $V_{BOOT\_OFF}$ | 8.2 | 8.7 | 9.2 | V |
| Upper Driver Consumption, No DRV Pulses | | $I_{BOOT1}$ | 60 | 90 | 120 | μA |
| Upper Driver Consumption, $C_{DRVH}$ = 1 nF between Pins 14 & 15 | | $I_{BOOT2}$ | 1.20 | 1.55 | 1.80 | mA |
| **HB DISCHARGER** | | | | | | |
| HB Sink Current Capability | $V_{HB}$ = 30 V | $I_{DISCHARGE1}$ | 5 | 7 | 9 | mA |
| HB Sink Current Capability $V_{HB}$ = $V_{HB\_MIN}$ | | $I_{DISCHARGE2}$ | 5 | 6.5 | 8 | mA |
| HB Voltage @ $I_{DISCHARGE}$ Changes from 6 to 0 mA | | $V_{HB\_MIN}$ | − | − | 23 | V |
| **DRIVER OUTPUTS** | | | | | | |
| Rise−time, 10 to 90% of Output Signal, DRVH | $C_{DRVH}$ = 1 nF | $t_{DRVH\_RISE}$ | − | 25 | 50 | ns |
| Fall−time 90 to 10% of Output Signal, DRVH | $C_{DRVH}$ = 1 nF | $t_{DRVH\_FALL}$ | − | 25 | 50 | ns |
| High side driver clamping voltage | | $V_{DRVH\_CLAMP}$ | 12 | 14 | 16 | V |
| High side driver voltage drop | | $V_{DRVH\_DROP}$ | − | − | 50 | mV |
| Rise time, 10 to 90 % of output signal, DRVL | $C_{DRVL}$ = 1 nF | $t_{DRVL\_RISE}$ | − | 25 | 50 | ns |
| Fall time, 90 to 10 % of output signal, DRVL | $C_{DRVL}$ = 1 nF | $t_{DRVL\_FALL}$ | − | 25 | 50 | ns |
| Low side driver clamping voltage | | $V_{DRVL\_CLAMP}$ | 12 | 14 | 16 | V |

**ELECTRICAL CHARACTERISTICS** (For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, $V_{HV}$ = 125 V, Vcc = 12 V, $C_{DRVH}$ = $C_{DRVL}$ = 1 nF unless otherwise noted) (continued)

| Characteristics | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRIVER OUTPUTS** | | | | | | |
| Low side driver voltage drop | | $V_{DRVL\_DROP}$ | – | – | 50 | mV |
| Output source short circuit current | $V_{DRVx}$ = 0 V, PW = 300 ns | $I_{DRVx\_SOURCE}$ | – | 0.8 | – | A |
| Output sink short circuit current | $V_{DRVx}$ = 0 V, PW = 300 ns | $I_{DRVx\_SINK}$ | – | 1.5 | – | A |
| Leakage current on high side voltage pins to GND | $V_{HB}$ = $V_{BOOT}$ = $V_{DRVH}$ = 700 V | $I_{HB\_LEAK}$ | – | 5 | 10 | μA |
| **DEAD−TIME GENERATION** | | | | | | |
| Maximum Dead−time Value if no dV/dt Failing/ Rising Edge is Received | | $t_{DEAD\_MAX}$ | 2.54 | 2.68 | 2.86 | μs |
| Number of DT_MAX Events to Enter the Fault Mode | | $N_{DT\_MAX}$ | – | 16 | – | – |
| **START−UP SEQUENCE PARAMETERS** | | | | | | |
| Initial DRVL On−time Duration | | $t_{1st\_DRVL\_MAX}$ | 3.04 | 3.20 | 3.42 | μs |
| Initial DRVH On−time Duration | | $t_{1st\_DRVH\_MAX}$ | 1.52 | 1.60 | 1.71 | μs |
| On−time Period Increment During Soft−start | | $t_{TON\_SS\_INC}$ | – | 8 | – | ns |
| Internal FB Ramp Increment During Soft Start | | $N_{SS\_INC}$ | – | 9.0 | – | – |
| Soft−Start Increment Division Ratio | | $K_{SS\_INC}$ | – | 2 | – | – |
| Time Duration to Restart IC if Start−up Phase is not Finished | | $t_{WATCHDOG}$ | 0.48 | 0.50 | 0.54 | ms |
| First DRVH On−time Increment after Watchdog Elapses | | $K_{1stDRVH\_INC}$ | – | 0.125 | – | – |
| **FEEDBACK SECTION** | | | | | | |
| Internal Pull−up Resistor on FB Pin | | $R_{FB}$ | 14 | 17 | 20 | kΩ |
| $V_{FB}$ to Internal Current Set Point Division Ratio | | $K_{FB}$ | 1.92 | 2.00 | 2.08 | – |
| Internal Voltage Reference | | $V_{FB}$ | 4.50 | 4.90 | 5.30 | V |
| Internal Clamp on FB Input of On−time Comparator Referred to External FB Pin Voltage | KFB = 2 | $V_{FB\_CLAMP}$ | 4.3 | 4.6 | 4.8 | V |
| Internal FB Offset Voltage to Compensate Opto−coupler Saturation Level | KFB = 2 (IPT options) | $V_{FB\_OFFSET}$ | 360 | 400 | 440 | mV |
| Internal FB Offset Compensation During Normal Operation | | $V_{FB\_OFFSET\_COMP}$ | −20 | 0 | 20 | mV |
| **CURRENT SENSE INPUT CS** | | | | | | |
| On−time Comparator Delay to High Side Driver DRVH Turn Off | $V_{FB}$ = 2.5 V<br>$V_{CS}$ rises from −2.0 V to 3.0 V with Rising Edge of 100 ns | $t_{CS\_DELAY}$ | – | 125 | 200 | ns |
| Current Sense Input Current for $V_{CS}$ = ±3 V | | $I_{CS}$ | – | – | ±200 | μA |
| Leading Edge Blanking Time of the On−time Comparator Output | | $t_{LEB}$ | 380 | 400 | 428 | ns |
| **BULK VOLTAGE SENSING INPUT BO** | | | | | | |
| Brown−out Turn−off Threshold | | $V_{BO\_TH}$ | 0.85 | 0.90 | 0.95 | V |
| Brown−out Hysteresis Current Sink | $V_{BO}$ < $V_{BO\_TH}$ | $I_{BO\_SINK}$ | 4.3 | 5.0 | 5.5 | μA |
| Brown−Out Comparator Hysteresis | | $V_{BO\_HYST}$ | 5 | 10 | 15 | mV |
| Brown−Out Bias Current | | $I_{BO\_BIAS}$ | – | – | 50 | nA |
| Brown−Out Filter Duration | | $t_{BO\_FILTER}$ | 47.5 | 50 | 53.5 | μs |
| Brown−Out Pin Current Source During Standby | | $t_{BO\_SOURCE}$ | – | 15 | – | μA |
| **SKIP** | | | | | | |
| Current Sourced by Skip Pin to Define the Skip in Level | | $I_{SKIP\_IN}$ | 17.3 | 19.6 | 21.3 | μA |

**ELECTRICAL CHARACTERISTICS** (For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, $V_{HV}$ = 125 V, Vcc = 12 V, $C_{DRVH}$ = $C_{DRVL}$ = 1 nF unless otherwise noted) (continued)

| Characteristics | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SKIP** | | | | | | |
| Minimum of FB Pin Voltage Below which Skip Mode is Entered Defined by External Resistor on Skip Pin | | $V_{FB\_SKIP\_IN\_EXT\_MIN}$ | – | 0.1 | 0.15 | V |
| Maximum of FB Pin Voltage Below which Skip Mode is Entered Defined by External Resistor on Skip Pin | | $V_{FB\_SKIP\_IN\_EXT\_MAX}$ | 2.50 | 2.55 | 2.60 | V |
| Value of FB Pin Voltage above which IC Leaves Skip Mode | (ITP options) | $V_{FB\_SKIP\_OUT}$ | 630 | 700 | 770 | mV |
| On−time Duration of 1st DRVL Pulse when FB Cross $V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ Threshold | | $t_{1st\_DRVL\_SKIP}$ | 1.52 | 1.6 | 1.71 | μs |
| Internal FB Level Reduction During 1st DRVH Pulse when FB Cross $V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ Threshold | | $V_{1ST\_DRVH\_SKIP}$ | – | 150 | – | mV |
| **QUIET−SKIP** | | | | | | |
| Feedback Voltage Thresholds to Enter Light Load Mode | (ITP options) | $V_{FB\_LL\_IN}$ | 1.07 | 1.16 | 1.25 | V |
| Feedback Voltage Thresholds to Exit Light Load Mode | (ITP options) | $V_{FB\_LL\_OUT}$ | 1.40 | 1.50 | 1.60 | V |
| The Portion of Previous MU On−time that is Place for Last ML Pulse in Pattern | | $t_{LAST\_ML\_PATTERN}$ | – | 150 | – | % |
| The Portion of Previous MU On−time that is Place for Last ML Pulse before the LL or Skip Mode is Activated | | $t_{LAST\_ML\_SKIP}$ | – | 150 | – | % |
| Skip Burst Off−time Duration that is Needed to Increase Number of Skipped Valleys/Peaks between Following Patterns | | $t_{GEAR\_UP}$ | – | 1 | – | ms |
| Skip Burst On−time Duration that is Needed to Decrease Number of Skipped Valleys/Peaks between Following Patterns | | $t_{GEAR\_DOWN}$ | – | 1 | – | ms |
| Time Duration to Force Valley/Peak Count Logic if Valley or Peak is not Detected | | $t_{VALPK\_WD}$ | 12.2 | 12.8 | 13.7 | μs |
| Quiet Timer Duration | | $t_{QS\_timer}$ | – | 1 | – | ms |
| Number of Patterns Adjustment when Bust Period is Shorter than 1/4 of QS_timer Duration | | $N_{QS\_1Q4}$ | – | 2 | – | – |
| Number of Patterns Adjustment when Bust Period is Longer than 1/4 and Shorter than 2/4 of QS_timer Duration | | $N_{QS\_2Q4}$ | – | 1 | – | – |
| Number of Patterns Adjustment when Bust Period is Longer than 2/4 and Shorter than 3/4 of QS_timer Duration | | $N_{QS\_3Q4}$ | – | 0 | – | – |
| Number of Patterns Adjustment when Bust Period is Longer than 3/4 and Shorter than 4/4 of QS_timer Duration | | $N_{QS\_4Q4}$ | – | 0 | – | – |
| Number of Patterns Adjustment when Bust Period is Longer than QS_timer Duration | | $N_{QS\_INF}$ | – | −1 | – | – |
| Initial Number of Patterns Placed when LL or Skip Mode is Activated | | $N_{PATTERN\_INIT}$ | – | 1 | – | – |
| Number of MU Pulses During which FB_LL_IN cmp is Blanked Once VFB > $V_{FB\_LL\_OUT}$ | | $N_{LL\_BLANK}$ | – | 60 | – | – |
| **FAULTS AND AUTO−RECOVERY TIMER** | | | | | | |
| Maximum On−time Clamp | | $t_{TON\_MAX}$ | 8.3 | 8.8 | 9.4 | μs |
| Number of TON_MAX Events to Confirm Fault | | $N_{TON\_MAX\_COUNTER}$ | – | 1 | – | – |

**ELECTRICAL CHARACTERISTICS** (For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, $V_{HV}$ = 125 V, Vcc = 12 V, $C_{DRVH}$ = $C_{DRVL}$ = 1 nF unless otherwise noted) (continued)

| Characteristics | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FAULTS AND AUTO−RECOVERY TIMER** | | | | | | |
| Internal FB Input Voltage for FB Fault Activation | KFB = 2 | $V_{FB\_FAULT}$ | 3.9 | 4.05 | 4.2 | – |
| FB Fault Timer Duration | | $t_{FAULT}$ | 760 | 800 | 860 | ms |
| Fault Timer Reset Time | | $t_{FAULT, RES}$ | 95 | 100 | 107 | μs |
| CS Voltage when CS Fault is Detected (NCL30159xA) | | $V_{CS\_FAULT}$ | 2.278 | 2.4 | 2.523 | V |
| Number of CS_fault cmp Pulses to Confirm CS Fault | | $N_{CS\_FAULT}$ | – | 5 | – | – |
| Number of Drive Pulses to Start Decrement of CS Fault Counter | | $N_{CS\_FAULT\_DEC}$ | – | 50 | – | – |
| Auto−recovery Duration (Common Timer for All Fault Condition) | | $t_{A-REC\_TIMER}$ | 0.95 | 1 | 1.07 | s |
| **dV/dt DETECTOR** | | | | | | |
| Positive Slew Rate on $V_{HB}$ Pin above which Automatic Dead−time end is Generated | | $P_{dV/dt\_th}$ | – | 300 | – | V/μs |
| Negative Slew Rate on $V_{HB}$ Pin above which Automatic Dead−time end is Generated | | $N_{dV/dt\_th}$ | – | 300 | – | V/μs |
| Positive Slew Rate on $V_{HB}$ Pin above which Automatic Dead−time end is Generated in QS Mode | | $P_{dV/dt\_th\_QSM}$ | – | 90 | – | V/μs |
| Negative Slew Rate on $V_{HB}$ Pin above which Automatic Dead−time end is Generated in QS Mode | | $N_{dV/dt\_th\_QSM}$ | – | 90 | – | V/μs |
| **RAMP COMPENSATION** | | | | | | |
| Ramp Compensation Gain | | $RC_{GAIN}$ | 56 | 72 | 85 | mV/μs |
| Ramp Compensation Time Shift | | $t_{RC\_SHIFT}$ | – | 0.6 | – | μs |
| **PFC MODE OUTPUT** | | | | | | |
| PFC MODE Output Voltage when Internal Pull−down Switch is Activated | $I_{PFCM\_SINK}$ = 1 mA | $V_{PFCM\_PD}$ | – | 50 | 200 | mV |
| PFC MODE Regulation Voltage 1 | $I_{PFCM\_SRC}$ = 100 μA | $V_{PFCM\_REG1\_1}$ | 12.81 | 14.12 | 15.56 | V |
| PFC MODE Regulation Voltage 1 | $I_{PFCM\_SRC}$ = 10 mA | $V_{PFCM\_REG1\_2}$ | 12.81 | 14.10 | 15.56 | V |
| PFC MODE Regulation Voltage 2 | $I_{PFCM\_SRC}$ = 100 μA | $V_{PFCM\_REG2\_1}$ | 11.33 | 12.54 | 13.86 | V |
| PFC MODE Regulation Voltage 2 | $I_{PFCM\_SRC}$ = 10 mA | $V_{PFCM\_REG2\_2}$ | 11.33 | 12.52 | 13.86 | V |
| PFC Mode Pin Leakage in High−Z State | $V_{PFCM}$ = 15 V, $V_{CC}$ = 20 V | $I_{PFCM\_LEAK\_HZ}$ | – | – | ±1 | μA |
| One−shot Time Duration − Minimum Time at Regulation Voltage after Skip/LL Mode | | $t_{PFCM\_OS}$ | – | 200 | – | μs |
| **TEMPERATURE SHUTDOWN** | | | | | | |
| Temperature Shutdown | $T_J$ going up | $T_{TSD}$ | – | 150 | – | °C |
| Temperature Shutdown Hysteresis | $T_J$ going down | $T_{TSD(HYS)}$ | – | 40 | – | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

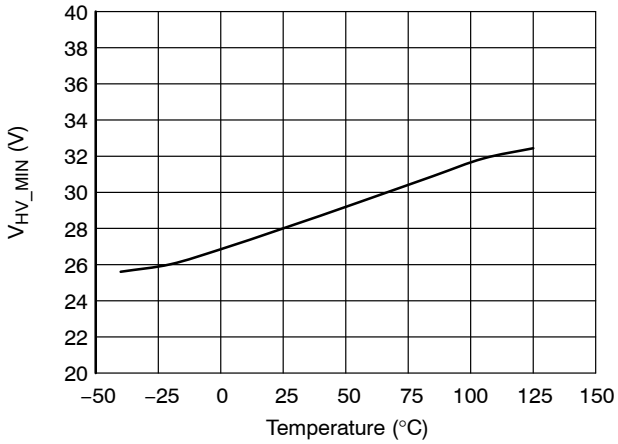



**Figure 3. Minimum Voltage for HV Current Source Operation VHV_MIN**

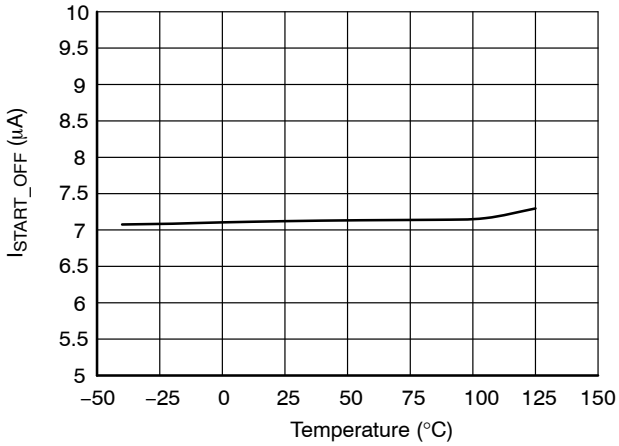



**Figure 4. Off−state Leakage Current to HV Pin $I_{START\_OFF}$**

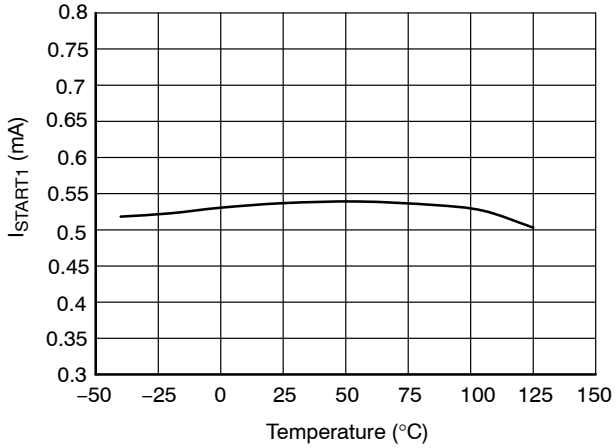



**Figure 5. High Voltage Startup Current Flowing Out of VCC Pin $I_{START1}$ in Case of VCC Pin Fault/Short**

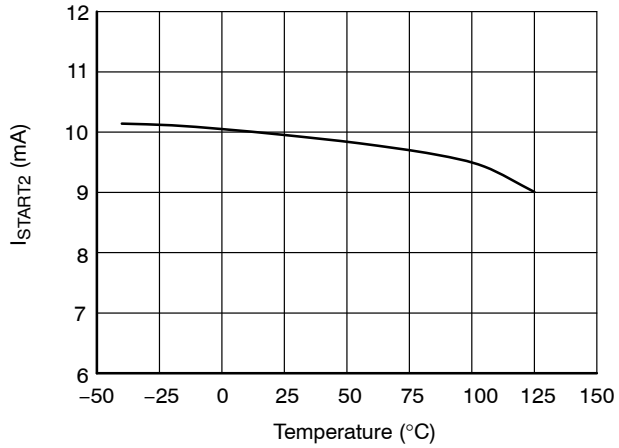



**Figure 6. High Voltage Startup Current Flowing Out of VCC Pin $I_{START2}$**

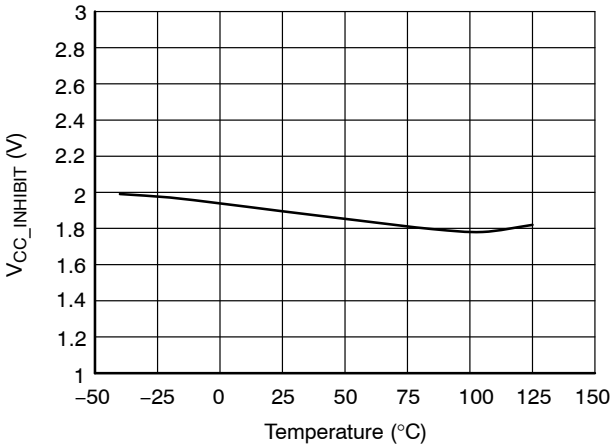



**Figure 7. VCC Level for $I_{START1}$ to $I_{START2}$ Transition**

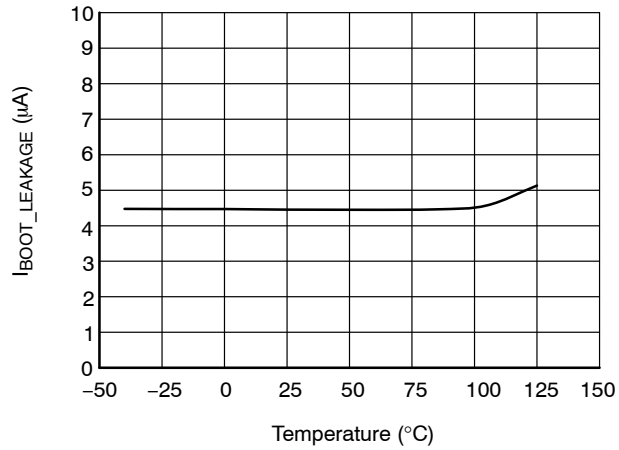



**Figure 8. $V_{BOOT}$ Pin Leakage $I_{BOOT\_LEAKAGE}$**

## TYPICAL CHARACTERISTICS (continued)

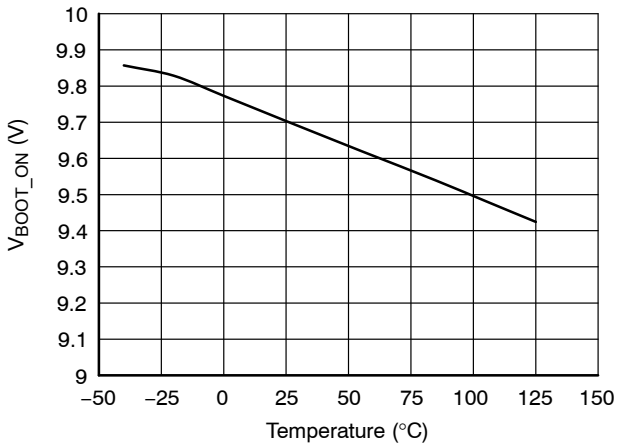



**Figure 9. Start−up Voltage of the Floating Section $V_{BOOT\_ON}$**

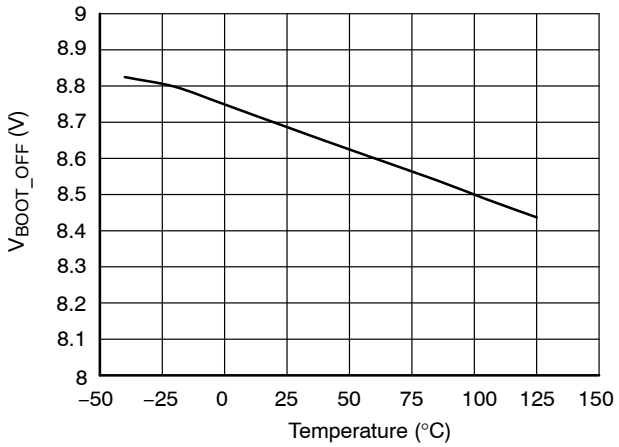



**Figure 10. Cut−off Voltage of the Floating Section $V_{BOOT\_OFF}$**

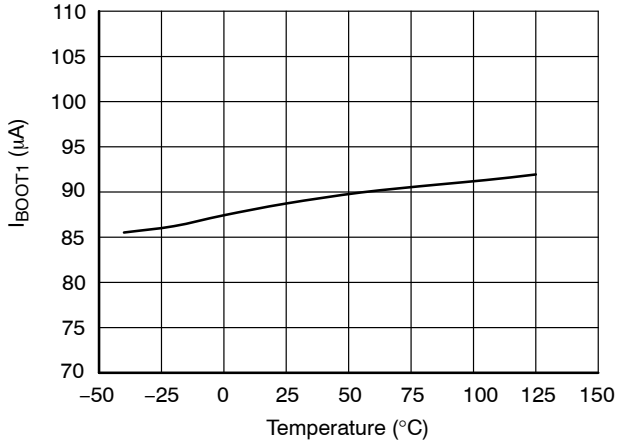



**Figure 11. Upper Driver Consumption without DRVH Pulses $I_{BOOT1}$**

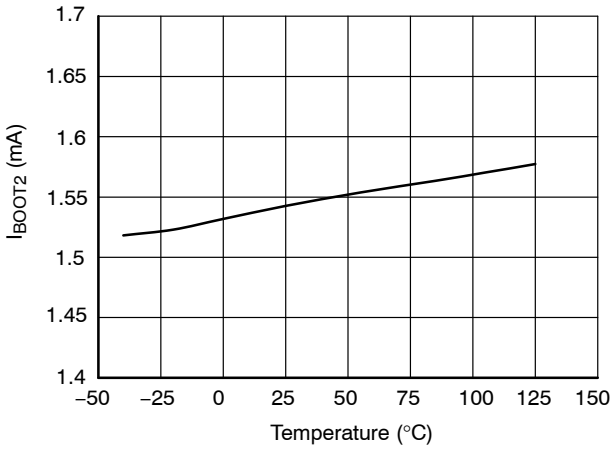



**Figure 12. Upper Driver Consumption with DRVH Pulses and Loaded by CDRVH = 1 nF between Pins 14 & 15 $I_{BOOT2}$**

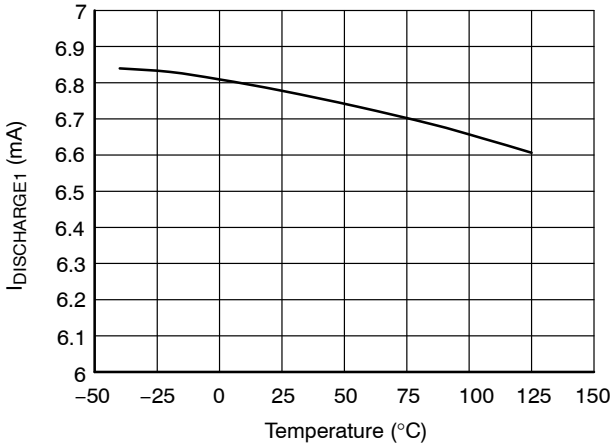



**Figure 13. HB Sink Current Capability $I_{DISCHARGE1}$**

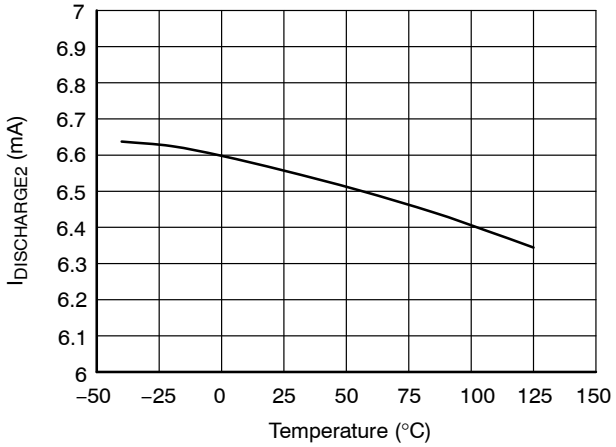



**Figure 14. HB Sink Current Capability @ $V_{HB} = V_{HB\_MIN}$**

## TYPICAL CHARACTERISTICS (continued)

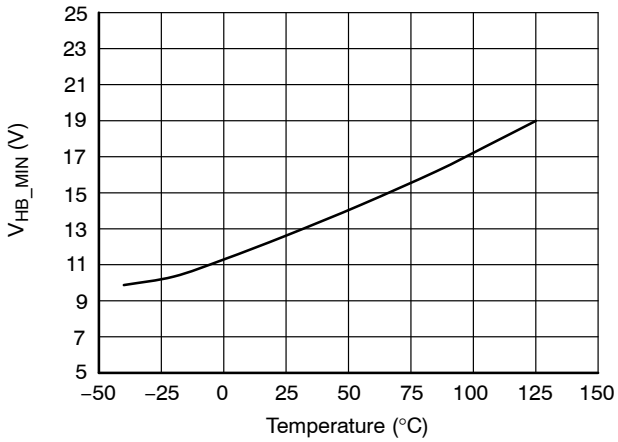



**Figure 15. HB Pin Voltage at Which $I_{DISCHARGE}$ Decreases from 6 mA to 0 mA**

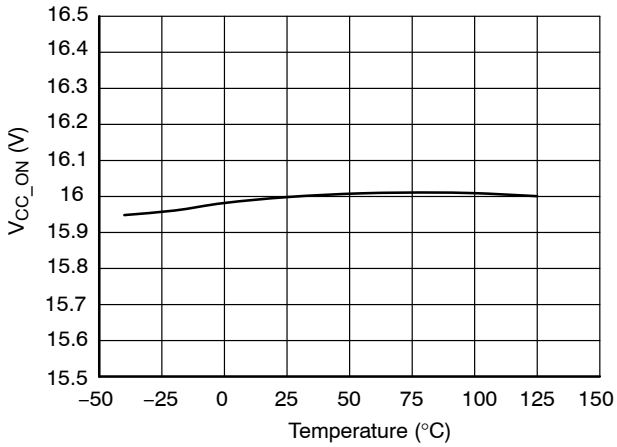



**Figure 16. $V_{CC}$ Turn−on Threshold Level, $V_{CC}$ Going Up HV Current Source Stop Threshold $V_{CC\_ON}$**

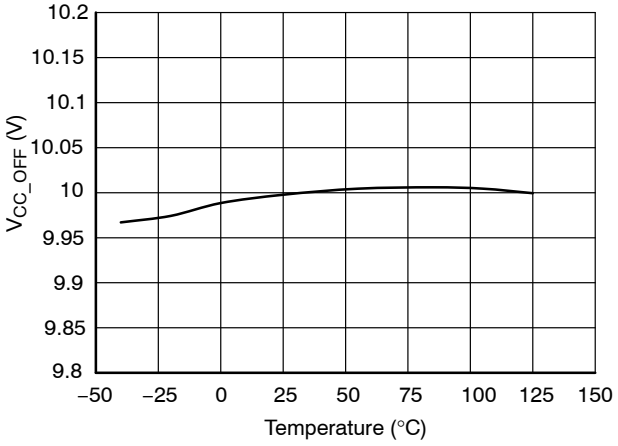



**Figure 17. $V_{CC}$ Turn−off Threshold Level (UVLO) $V_{CC\_OFF}$**

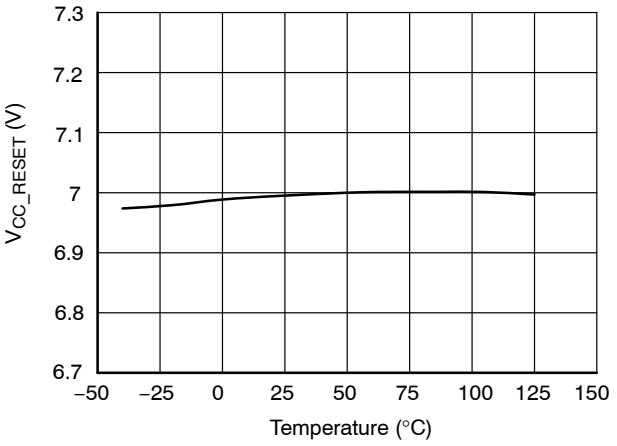



**Figure 18. $V_{CC}$ Decreasing Level at Which the Internal Logic Resets $V_{CC\_RESET}$**

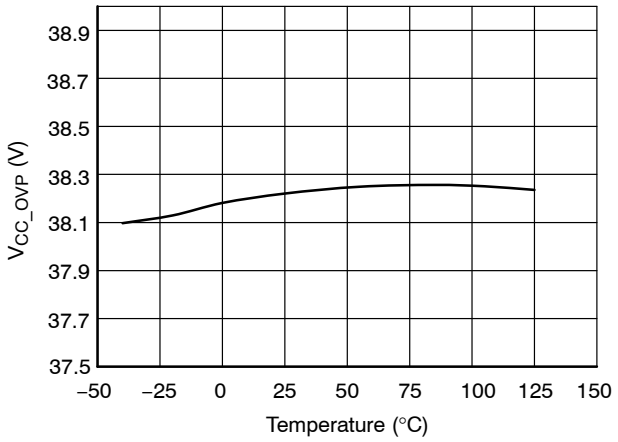



**Figure 19. $V_{CC}$ Overvoltage Threshold $V_{CC\_OVP}$**

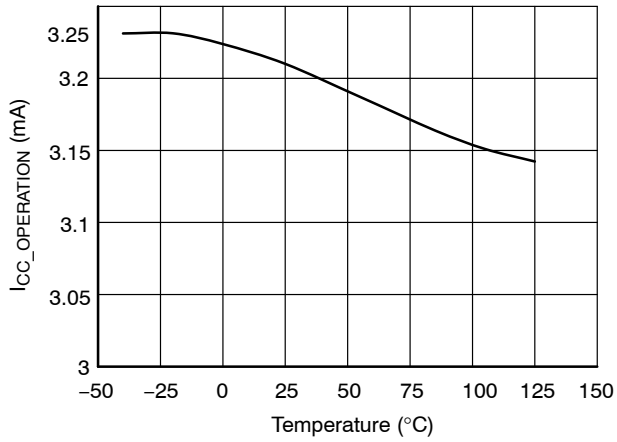



**Figure 20. Internal Current Consumption During Normal Operation $I_{CC\_OPERATION}$ @ CDRVL = 1 nF; fSW = 100 kHz**

## TYPICAL CHARACTERISTICS (continued)

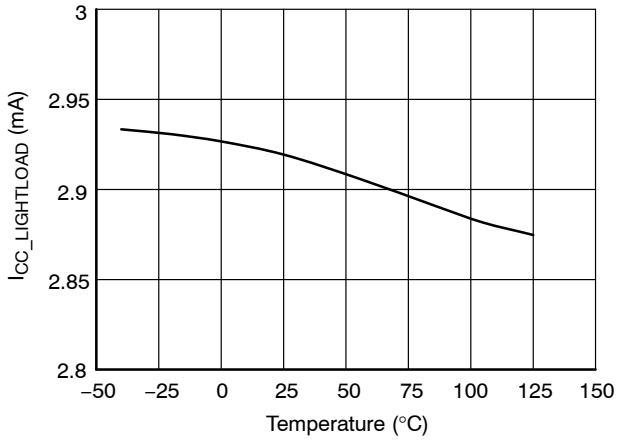



**Figure 21. Internal Current Consumption During Light Load Operation $I_{CC\_LIGHTLOAD}$ @ $C_{DRVL}$ = 1 nF; fSW = 100 kHz**

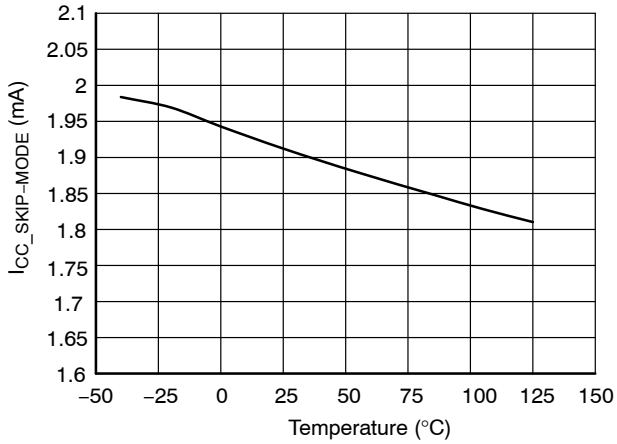



**Figure 22. Internal Current Consumption During Skip Mode $I_{CC\_SKIP-MODE}$**

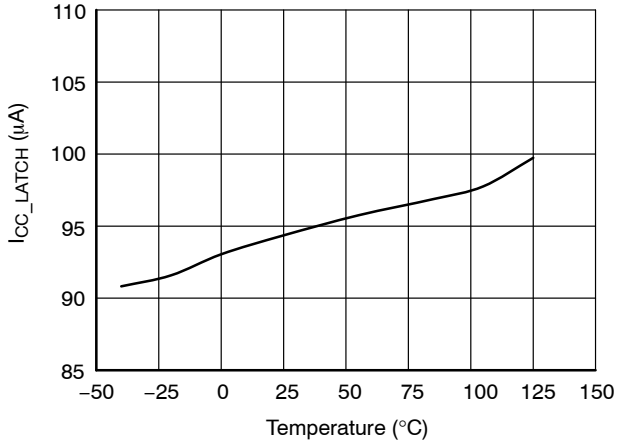



**Figure 23. Internal Current Consumption in Fault Mode (Latch) $I_{CC\_LATCH}$**

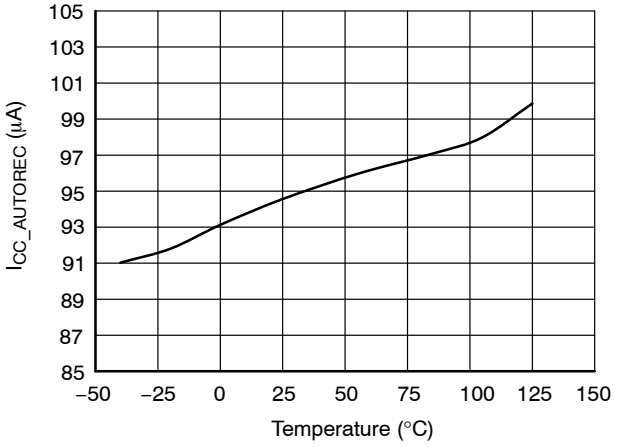



**Figure 24. Internal Current Consumption in Fault Mode (Autorecovery) $I_{CC\_AUTOREC}$**

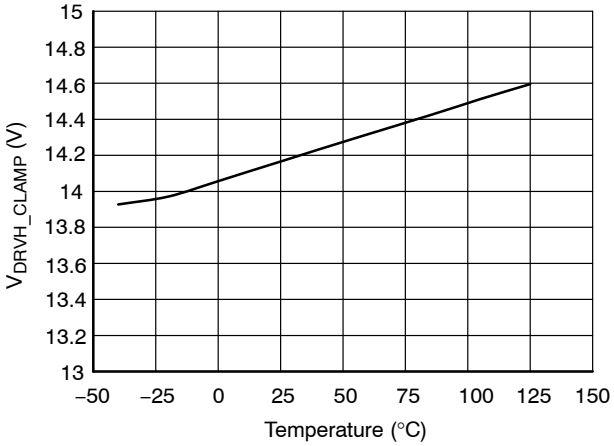



**Figure 25. High Side Driver Clamping Voltage $V_{DRVH\_CLAMP}$**

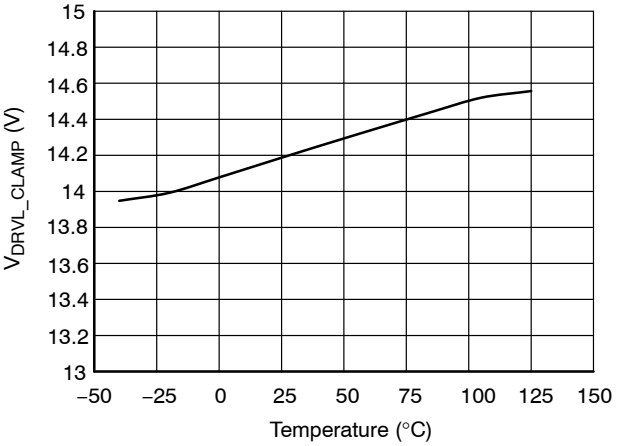



**Figure 26. Low Side Driver Clamping Voltage $V_{DRVL\_CLAMP}$**

## TYPICAL CHARACTERISTICS (continued)

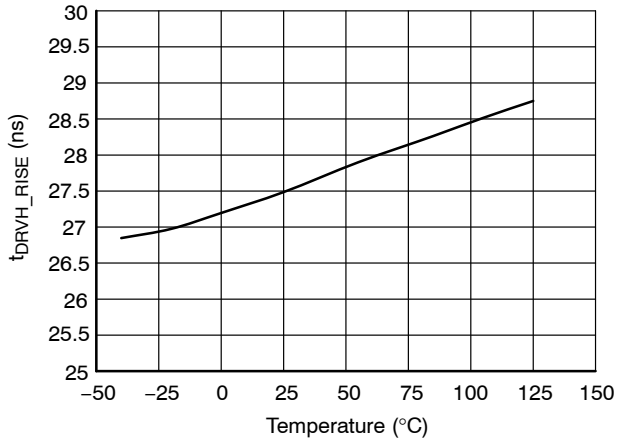



**Figure 27. High Side Driver Rise Time $t_{DRVH\_RISE}$ from 10% to 90% of DRVH Signal**

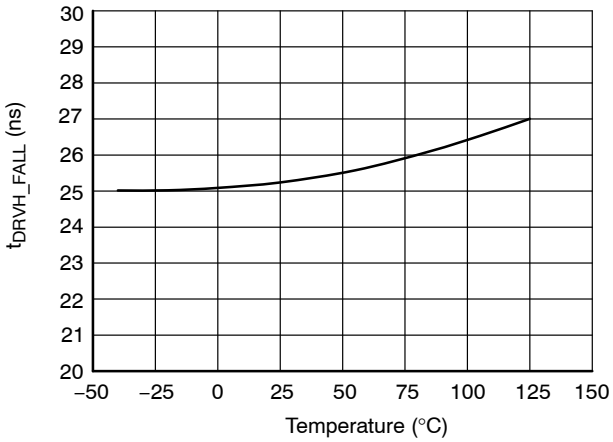



**Figure 28. High Side Driver Fall Time $t_{DRVH\_FALL}$ from 90% to 10% of DRVH Signal**

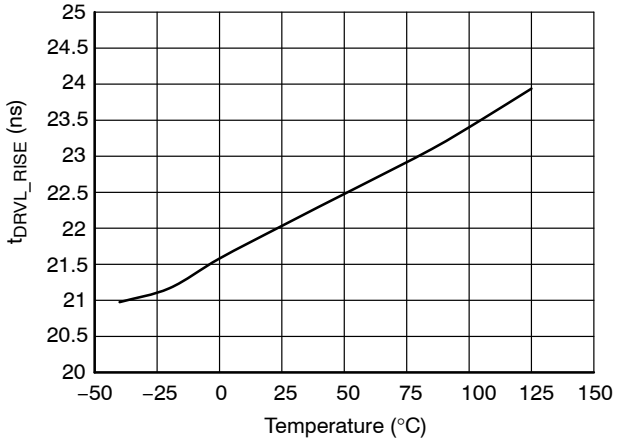



**Figure 29. Low Side Driver Rise Time $t_{DRVL\_RISE}$ from 10% to 90% of DRVL Signal**

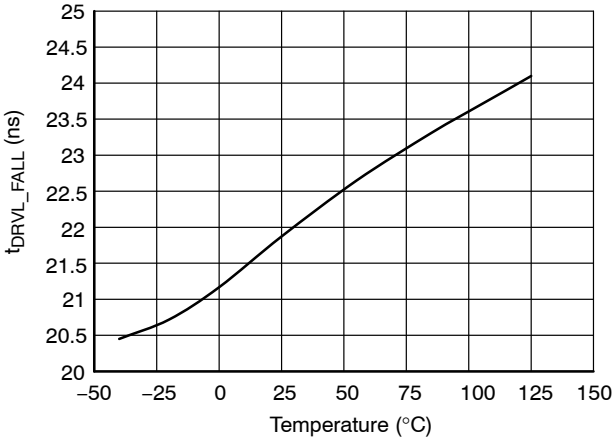



**Figure 30. Low Side Driver Fall Time $t_{DRVL\_FALL}$ from 90% to 10% of DRVL Signal**

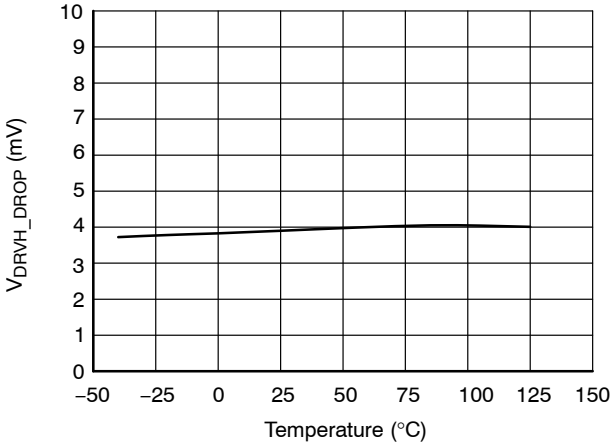



**Figure 31. High Side Driver Voltage Drop $V_{DRVH\_DROP}$**

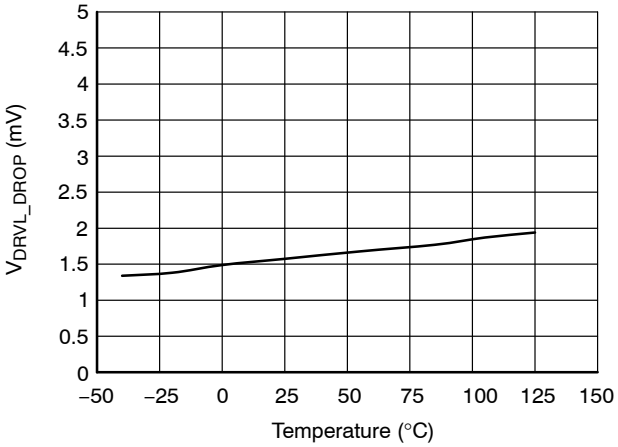



**Figure 32. Low Side Driver Voltage Drop $V_{DRVL\_DROP}$**

## TYPICAL CHARACTERISTICS (continued)

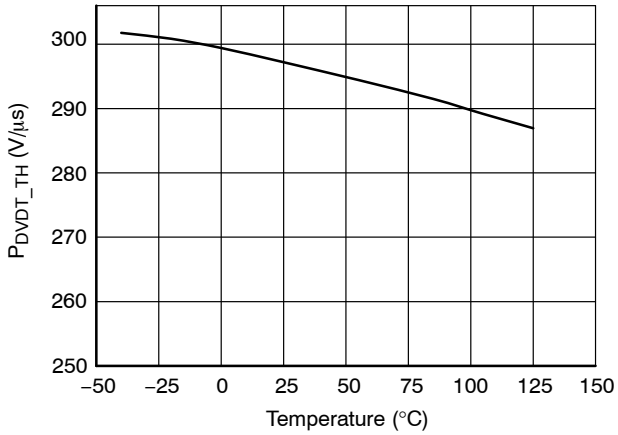



**Figure 33. Positive Slew Rate on $V_{HB}$ Pin above Which Automatic Dead−time End is Generated $P_{DVDT\_TH}$**

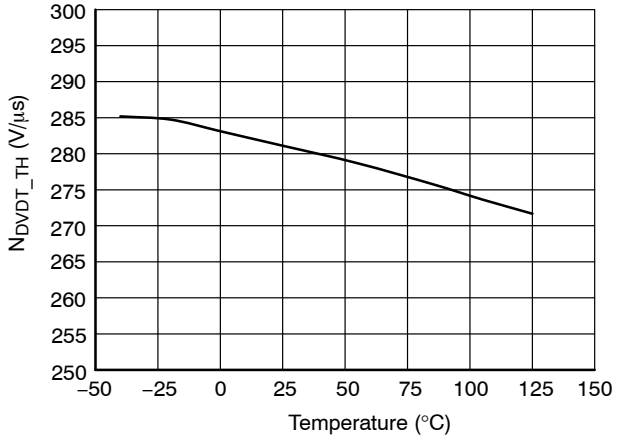



**Figure 34. Negative Slew Rate on $V_{HB}$ Pin above Which Automatic Dead−time End is Generated $N_{DVDT\_TH}$**

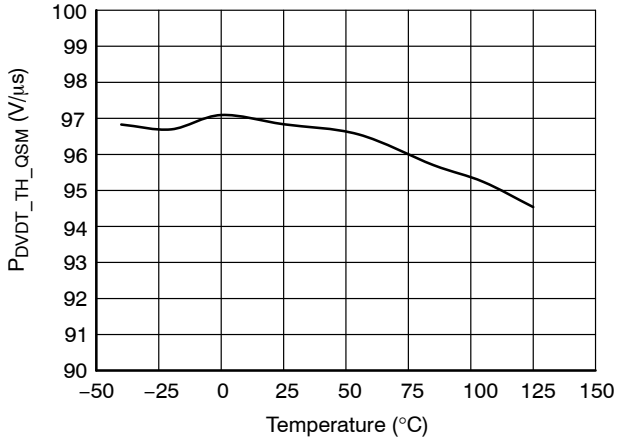



**Figure 35. Positive Slew Rate on $V_{HB}$ Pin above Which Automatic Dead−time End is Generated in QS Mode $P_{DVDT\_TH\_QSM}$**

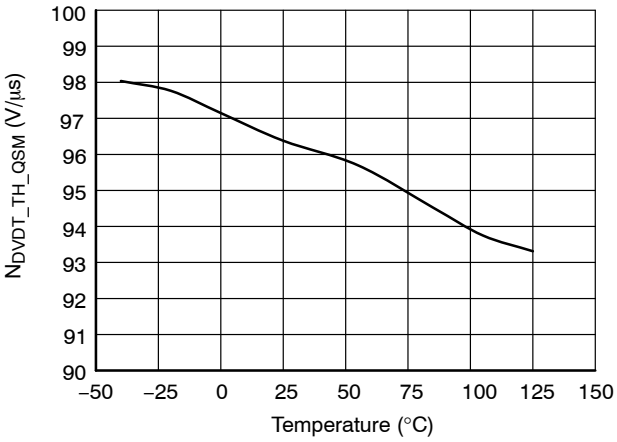



**Figure 36. Negative Slew Rate on $V_{HB}$ Pin above Which Automatic Dead−time End is Generated in QS Mode $N_{DVDT\_TH\_QSM}$**

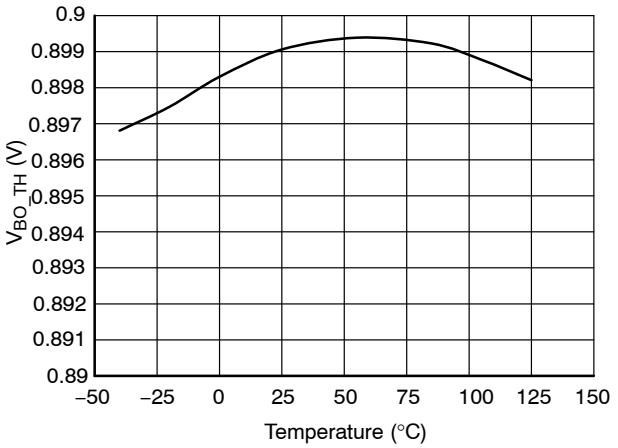



**Figure 37. Brown−out Turn−off Threshold $V_{BO\_TH}$**

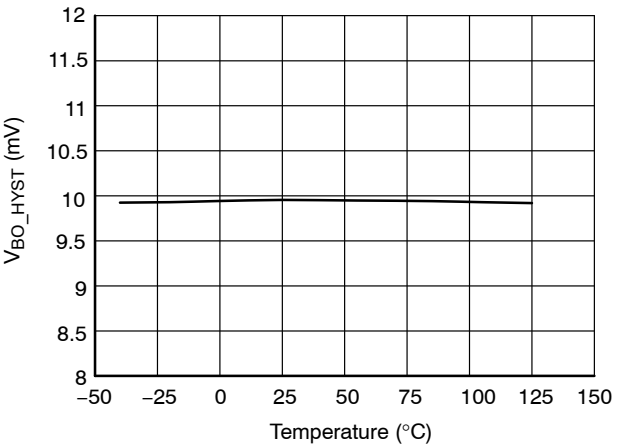



**Figure 38. Brown−out Comparator Hysteresis $V_{BO\_HYST}$**

## TYPICAL CHARACTERISTICS (continued)

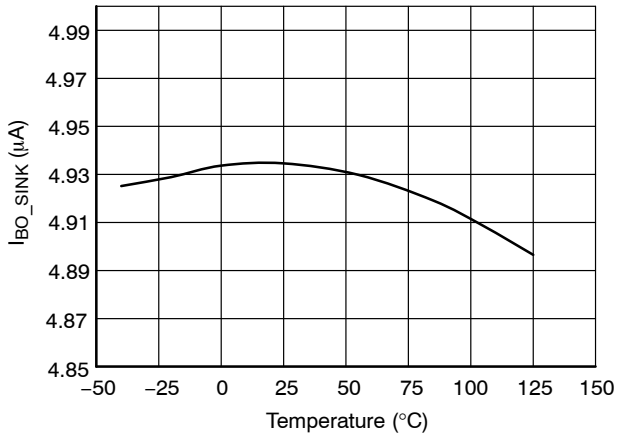



**Figure 39. Brown−out Hysteresis Current Sink $I_{BO\_SINK}$**

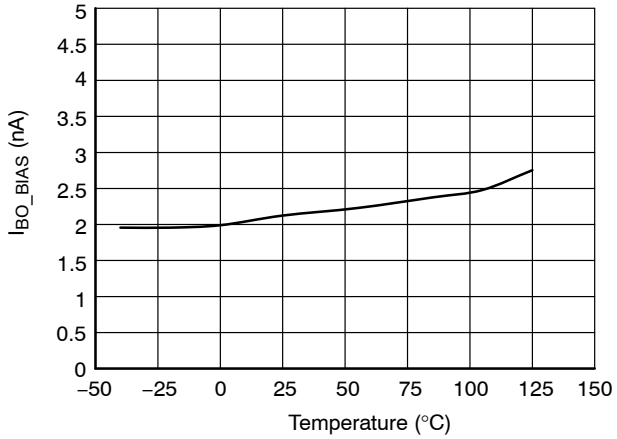



**Figure 40. Brown−out Bias Current $I_{BO\_BIAS}$**

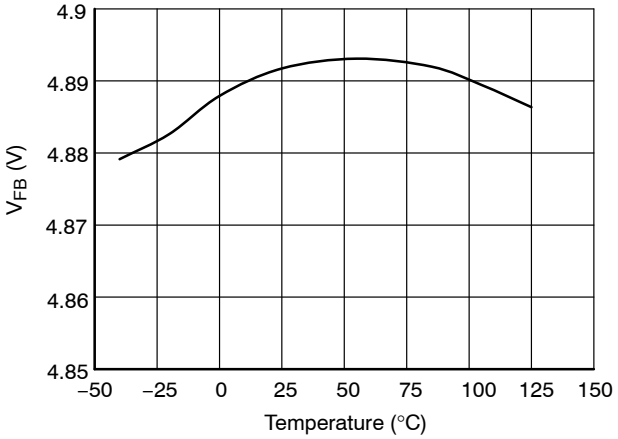



**Figure 41. Internal Voltage Reference at FB Pin $V_{FB}$**

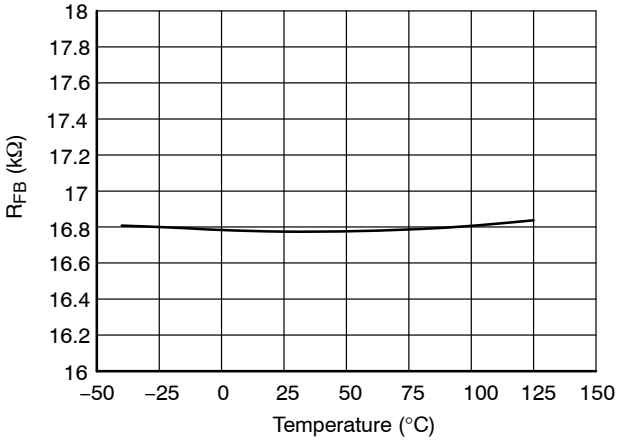



**Figure 42. Internal Pull−up Resistor on FB Pin $R_{FB}$**

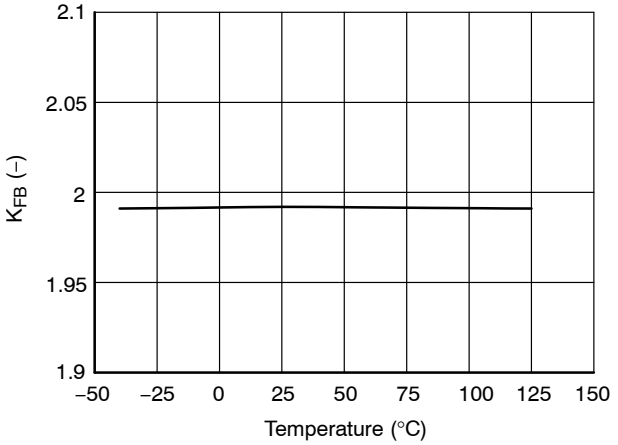



**Figure 43. $V_{FB}$ to Internal Current Setpoint Division Ratio $K_{FB}$**

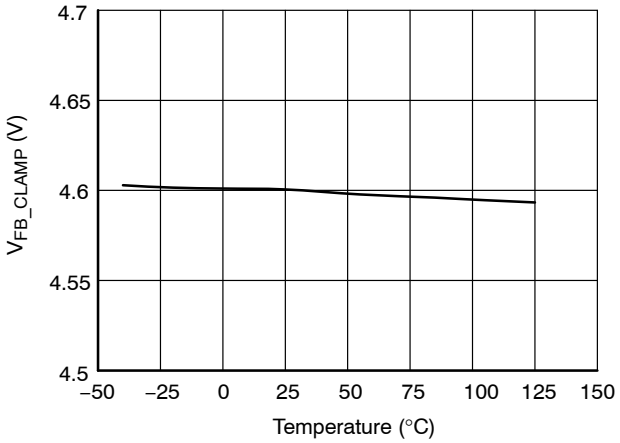



**Figure 44. Internal Clamp on FB Input of On−time Comparator Referred to External FB Pin Voltage $V_{FB\_CLAMP}$**

## TYPICAL CHARACTERISTICS (continued)

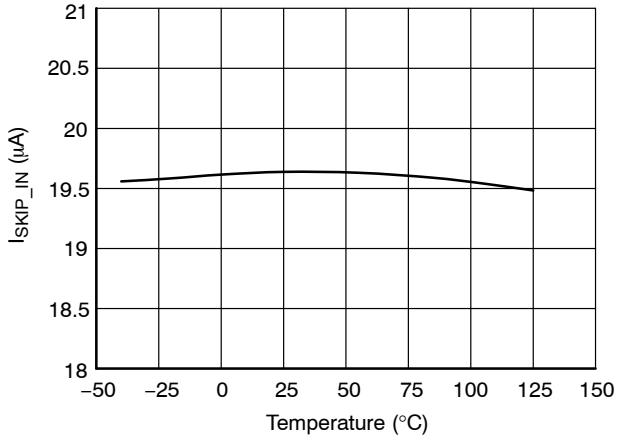



**Figure 45. Current Sourced by the Skip Pin to Define the Skip in Level $I_{SKIP\_IN}$**

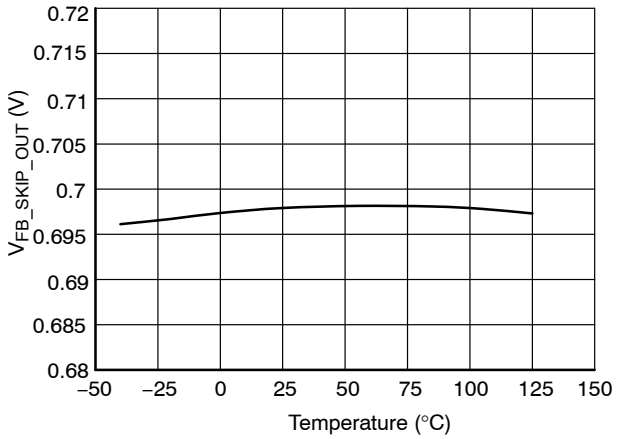



**Figure 46. Value of FB Pin Voltage above Which IC Leaves Skip Mode $V_{FB\_SKIP\_OUT}$**

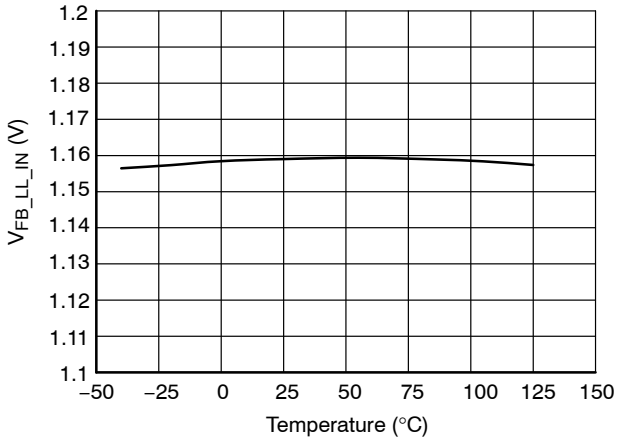



**Figure 47. Feedback Voltage Threshold to Enter Light Load Mode $V_{FB\_LL\_IN}$**

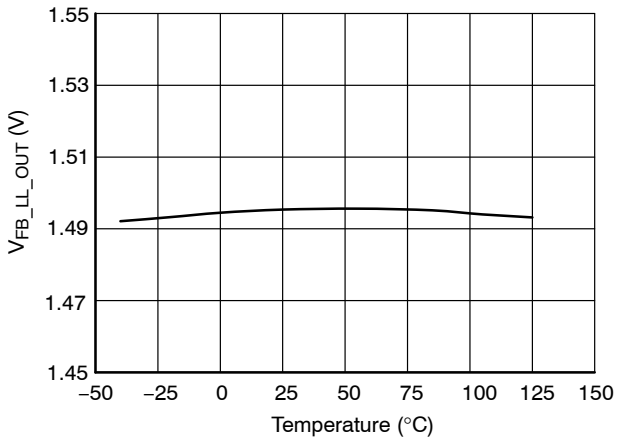



**Figure 48. Feedback Voltage Threshold to Exit Light Load Mode $V_{FB\_LL\_OUT}$**

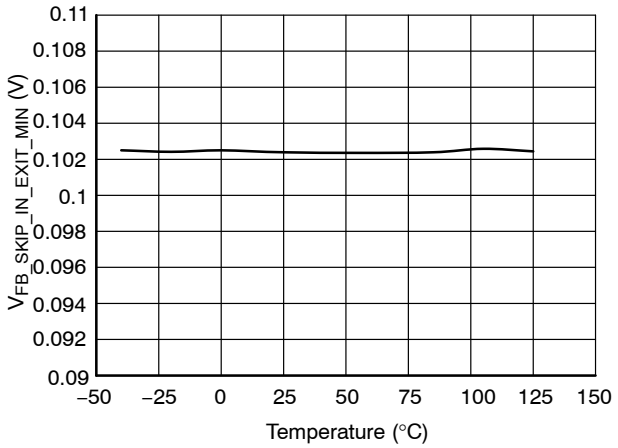



**Figure 49. Minimum Voltage on the Skip Pin to Define the Skip in Level $V_{FB\_SKIP\_IN\_EXIT\_MIN}$**

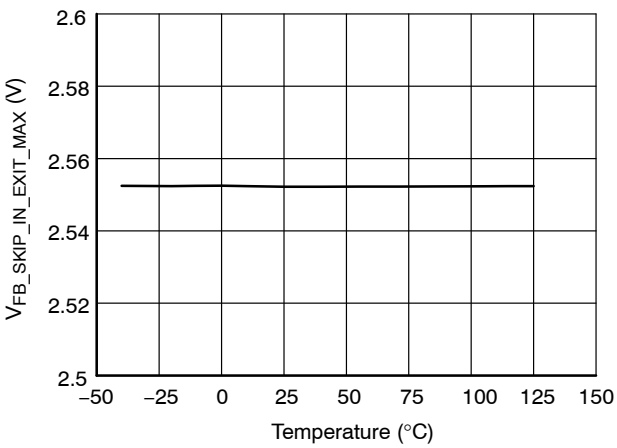



**Figure 50. Maximum Voltage on the Skip Pin to Define the Skip in Level $V_{FB\_SKIP\_IN\_EXIT\_MAX}$**

## TYPICAL CHARACTERISTICS (continued)

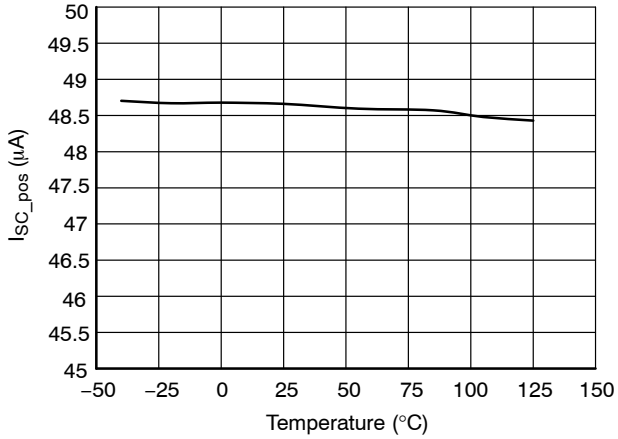



**Figure 51. Current Sense Input Current $I_{CS\_pos}$ @ $V_{CS}$ = 3 V**

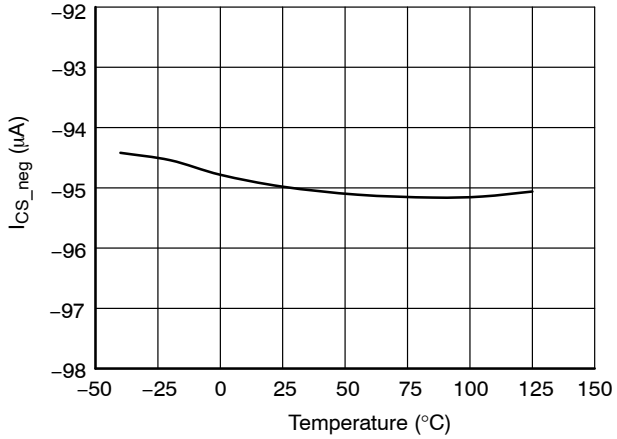



**Figure 52. Current Sense Input Current $I_{CS\_neg}$ @ $V_{CS}$ = −3 V**

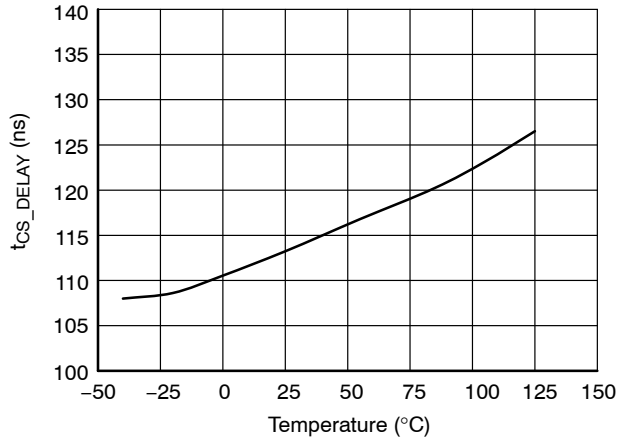



**Figure 53. On−time Comparator Delay to High Side Driver DRVH Turn Off $t_{CS\_DELAY}$**

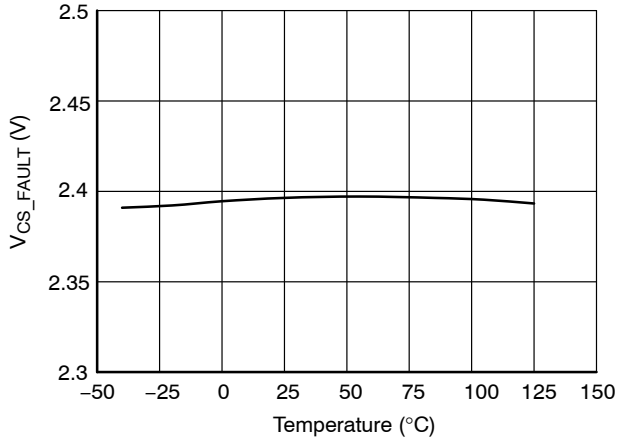



**Figure 54. CS Voltage When CS Fault is Detected $V_{CS\_FAULT}$**

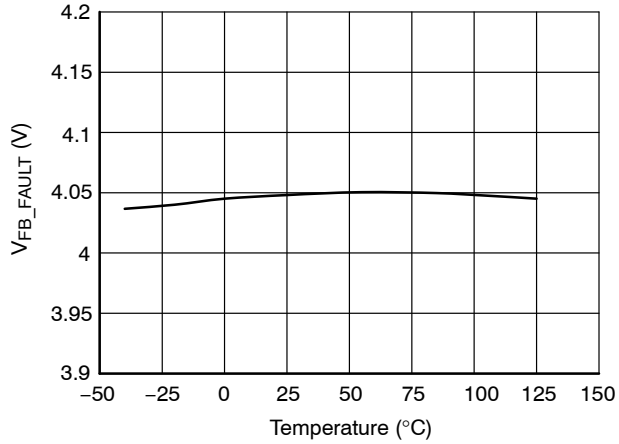



**Figure 55. Internal FB Input Voltage for FB Fault Activation $V_{FB\_FAULT}$**

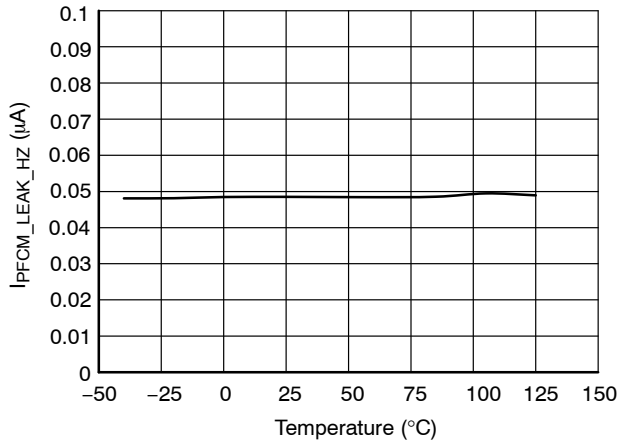



**Figure 56. PFC Mode Pin Leakage in High−Z State $I_{PFCM\_LEAK\_HZ}$**

## TYPICAL CHARACTERISTICS (continued)

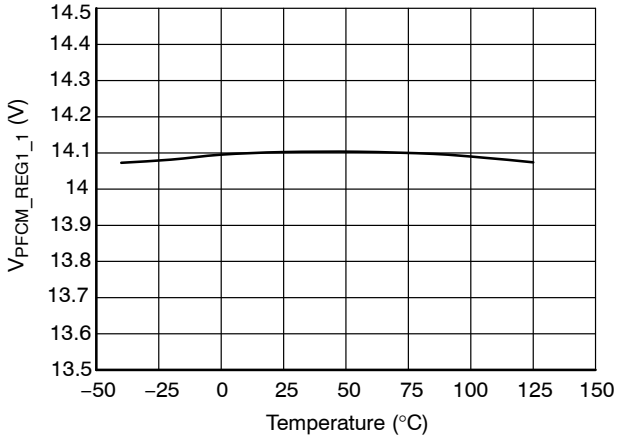



**Figure 57. PFC Mode Regulation Voltage 1 $V_{PFCM\_REG1\_1}$ When Loaded by 100 μA**

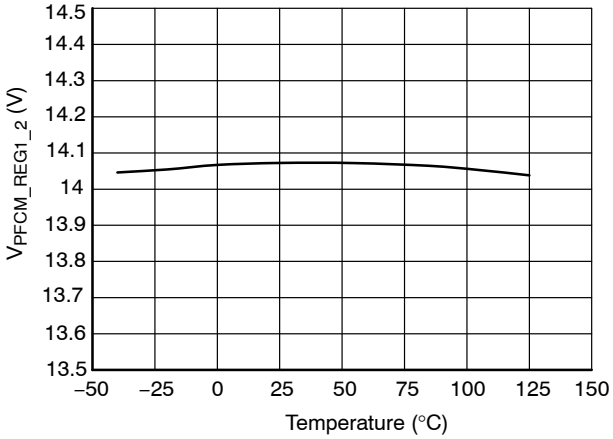



**Figure 58. PFC Mode Regulation Voltage 1 $V_{PFCM\_REG1\_2}$ When Loaded by 10 mA**

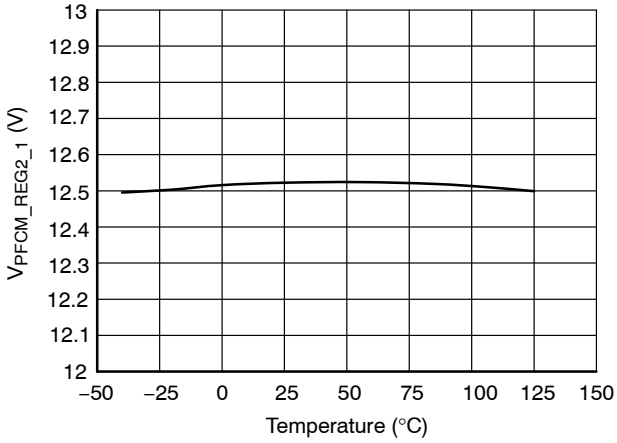



**Figure 59. PFC Mode Regulation Voltage 2 $V_{PFCM\_REG2\_1}$ When Loaded by 100 μA**

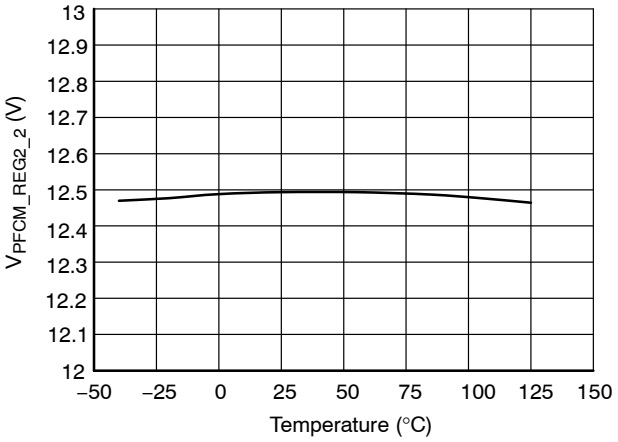



**Figure 60. PFC Mode Regulation Voltage 2 $V_{PFCM\_REG2\_2}$ When Loaded by 10 mA**

## APPLICATION INFORMATION

### Functional Description

This new controller builds on the previously−developed integrated circuits for LLC converters control. The control technique optimizes switching frequency depending on energy transferred via resonant tank and circulating in it. This device allows to control the conventional LLC converters and it is optimized for the LED lighting applications. The LLC converter control setup dedicated for LED market is the quite unique feature on the market.

### LLC Operation

Frequency modulation of today's commercially available resonant mode controllers is usually based on the output voltage regulator feedback. The feedback voltage (or current) of output regulator drives voltage (or current) controlled oscillator (VCO or CCO) in the controller. This method presents three main disadvantages:

1st − The 2nd order pole is present in small signal gain−phase characteristics => the lower cross over frequency and worse transient response is imposed by the system when voltage mode control is used. There is no direct link to the actual primary current – i.e. no line feed forward mechanism which results in poor line transient response.

2nd – Precise VCO (or CCO) is needed to assure frequency modulation with good reproducibility, $f_{min}$ and $f_{max}$ clamps need to be adjusted for each design => need for an adjustment pin(s).

3rd – Dedicated overload protection system, requiring an additional pin, is needed to assure application safety during overload and/or secondary short circuit events.

The NCL30159 resolves all disadvantages mentioned above by implementing a current mode control scheme that ensures best transient response performance and provides inherent cycle−by−cycle over−current protection feature in the same time.

### Start−up of the Controller

At start−up, the current source turns on when the voltage on the HV pin is higher than $V_{HV\_MIN}$, and turns off when $V_{CC}$ reaches $V_{CC\_ON}$, then turns on again when $V_{CC}$ reaches $V_{CC\_OFF}$, until the input voltage is high enough to ensure a proper start−up, i.e. when $V_{HV}$ reaches $V_{HV(start)}$. The controller actually starts the next time $V_{CC}$ reaches $V_{CC\_ON}$. The controller then delivers pulses, starting with a dedicated soft−start sequence during which the output voltage increases before the current−mode control takes over.

Even though the Dynamic Self−Supply is able to maintain the $V_{CC}$ voltage between $V_{CC\_ON}$ and $V_{CC\_MIN}$ by turning the HV start−up current source on and off, it can only be used in light load condition, otherwise the power dissipation on the die would be too much. As a result, an auxiliary voltage source is needed to supply $V_{CC}$ during normal operation.

The Dynamic Self−Supply is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown−out condition, or to prevent the controller from stopping during load transients when the $V_{CC}$ might drop. The NCL30159 accepts a supply voltage as high as 37 V, with an overvoltage threshold $V_{CC\_OVP}$ that latches the controller off.

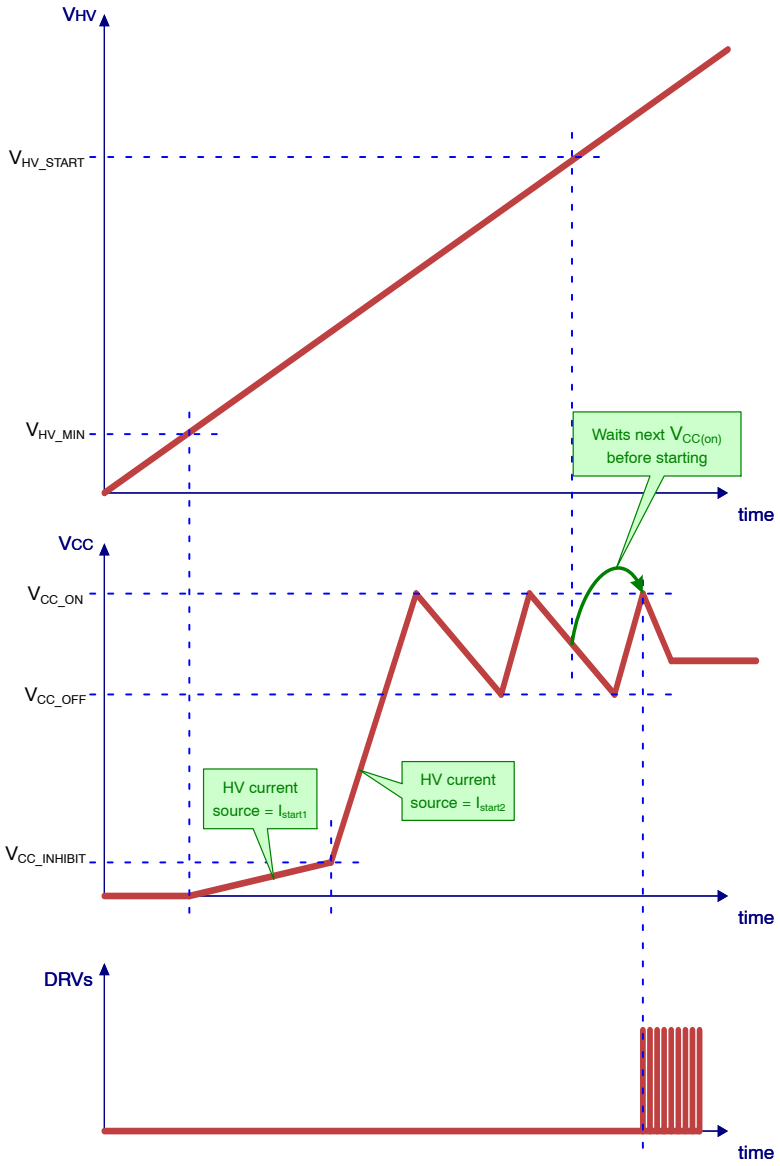



**Figure 61. Vcc Start−up Timing Diagram**

For safety reasons, the start−up current is lowered when $V_{CC}$ is below $V_{CC\_INHIBIT}$, to reduce the power dissipation in case the $V_{CC}$ pin is shorted to GND (in case of $V_{CC}$ capacitor failure, or external pull−down on $V_{CC}$ to disable the controller). There is only one condition for which the current source doesn't turn on when $V_{CC}$ reaches $V_{CC\_INHIBIT}$: the voltage on HV pin is too low (below $V_{HV\_MIN}$).

### HV Sensing of Rectified AC Voltage

The NCL30159 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start−up threshold and an autorecovery brown−out protection; both of them independent of the ripple on the input voltage. It is allowed only to work with an unfiltered, rectified ac input to ensure the X2 capacitor discharge function as well, which is described in following. The brown−out protection thresholds are fixed, but they are designed to fit most of the standard ac−dc conversion applications.

When the input voltage goes below $V_{HV\_STOP}$, a brown−out condition is detected, and the controller stops. The HV current source maintains $V_{CC}$ between $V_{CC\_ON}$ and $V_{CC\_OFF}$ levels until the input voltage is back above $V_{HV\_START}$.

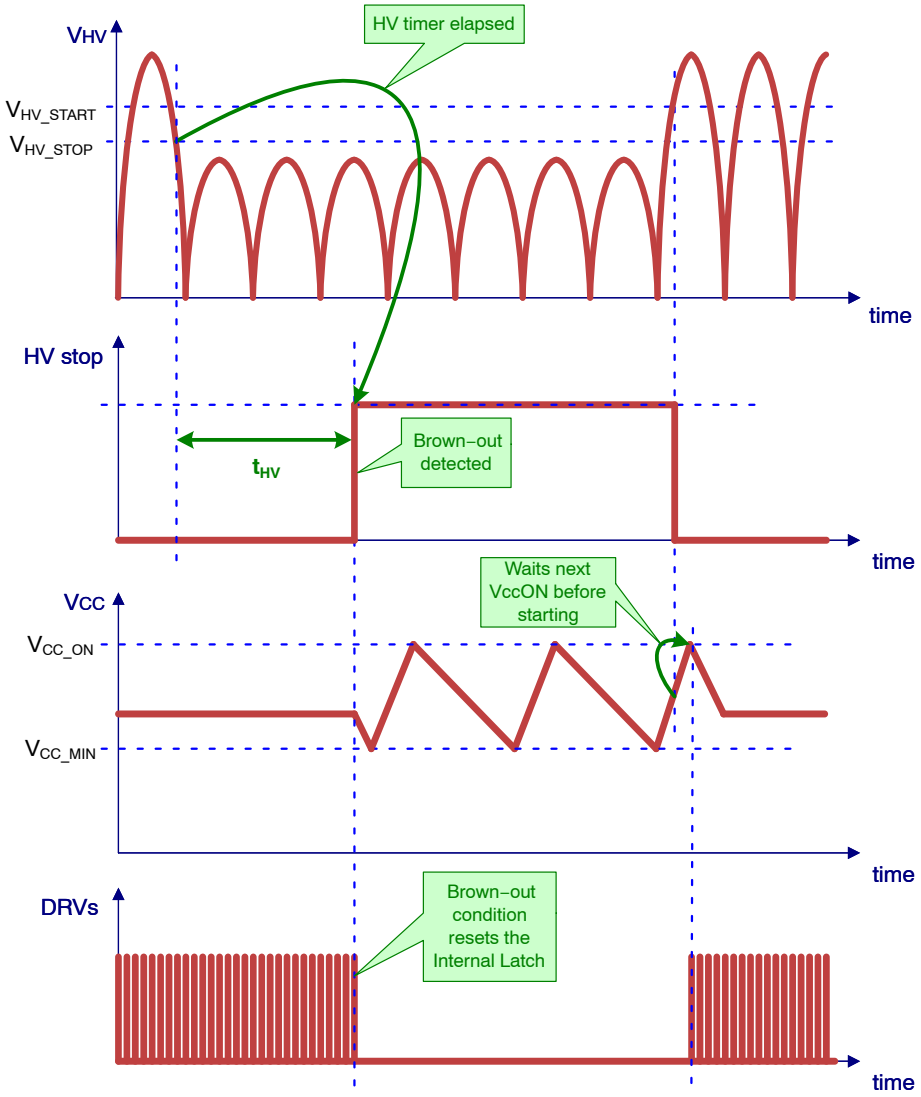



**Figure 62. Ac Line Drop−out Timing Diagram**

When $V_{HV}$ crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration $t_{HV}$, this ensures that the controller doesn't stop in case of line cycle drop−out.

When $V_{HV}$ crosses the $V_{HV(start)}$ threshold, the controller starts when the $V_{CC}$ crosses the next $V_{CC(on)}$ event. When it crosses $V_{HV(stop)}$, it triggers a timer of duration $t_{HV}$, this ensures that the controller doesn't stop in case of line cycle drop−out. The device restart after the ac line voltage drop−out is protected to the parasitic restart initiated e.g. the spikes induced at HV pin immediately after the device is stopped by the residual energy in the EMI filter.

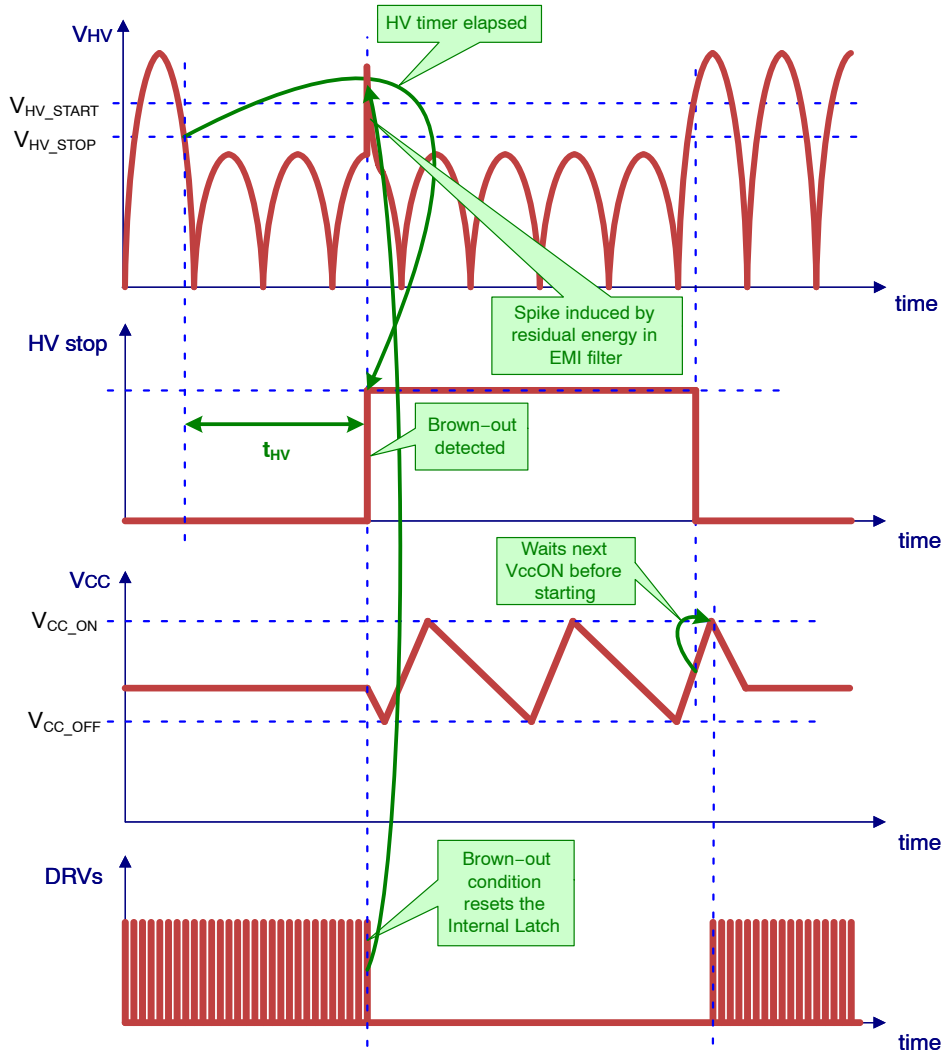



**Figure 63. Ac Line Drop−out Timing Diagram with the Parasitic Spike**

### Bulk Voltage Sensing Input BO

Resonant tank of an LLC converter is always designed to operate within a specific bulk voltage range. Operation below minimum bulk voltage level would result in current and temperature overstress of the converter power stage. The NCL30159 controller features a BO input in order to precisely adjust the bulk voltage turn−ON and turn−OFF levels. This Brown−Out protection (BO) greatly simplifies application level design.

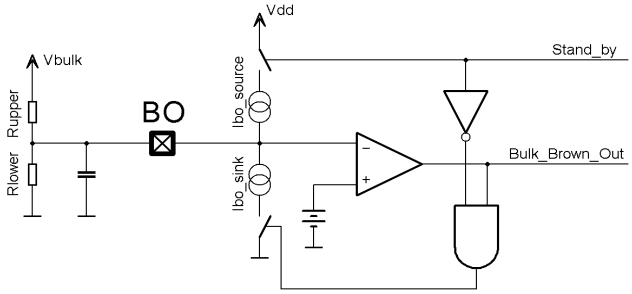



**Figure 64. Internal Connection of the Brown−out Protection Block**

The internal circuitry shown in Figure 64 allows monitoring the high−voltage input rail ($V_{bulk}$). A high−impedance resistive divider made of $R_{upper}$ and $R_{lower}$ resistors brings a portion of the $V_{bulk}$ rail to the BO pin. The Current sink ($I_{BO\_SINK}$) is active below the *bulk voltage turn−on* level ($V_{BULK\_ON}$). Therefore, the *bulk voltage* turn−on level is higher than defined by the division ratio of the resistive divider. To the contrary, when the internal BO_OK signal is high, i.e. the application is running, the $I_{BO\_DOWN}$ sink is disabled. The bulk voltage turn−off threshold ($V_{BULK\_OFF}$) is then given by BO comparator reference voltage directly on the resistor divider. The advantage of this solution is that the $V_{BULK\_OFF}$ threshold precision is not affected by $I_{BO\_DOWN}$ (hysteresis) current sink tolerance.

The $V_{BULK\_ON}$ and $V_{BULK\_OFF}$ levels can be calculated using equations below:

The $I_{BO\_SINK}$ is ON:

$$V_{BO} + V_{BOhyst} = V_{bulk\_ON} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO\_SINK} \cdot \left( \frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad \text{(eq. 1)}$$

The $I_{BO\_SINK}$ is OFF:

$$V_{BO} = V_{bulk\_OFF} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 2)}$$

One can extract $R_{lower}$ term from equation 2 and use it in equation 1 to get needed $R_{upper}$ value:

$$R_{lower} = \frac{\frac{V_{bulk\_ON} \cdot V_{BO}}{V_{bulk\_OFF}} - V_{BO} - v_{BOhyst}}{I_{BO\_SINK} \cdot \left(1 - \frac{V_{BO}}{V_{bulk\_OFF}}\right)} \quad \text{(eq. 3)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk\_OFF} - V_{BO}}{V_{BO}} \quad \text{(eq. 4)}$$

Note that the BO pin is pulled down by an internal switch when the controller is in startup phase − i.e. when the $V_{CC}$ voltage ramps up from $V_{CC} < V_{CC\_RESET}$ towards the $V_{CC\_OFF}$ level on the VCC pin. This feature assures that the BO pin voltage will not ramp up before the IC operation starts. The $I_{BO}$ hysteresis current sink is activated and BO discharge switch is disabled once the $V_{CC}$ voltage crosses $V_{CC\_OFF}$ threshold. The BO pin voltage then ramps up naturally according to the bulk voltage divider information. The BO comparator then authorizes or disables the LLC stage operation based on the actual $V_{bulk}$ level.

The current source $I_{BO\_SOURCE}$ could be used for turning off the PFC stage during the stand−by mode to decrease the consumption. The FB voltage to the PFC controller will be artificially increased so the switching of PFC stage would stop for certain period, depending on the voltage divider design, bulk capacitor volume and consumption in stand−by mode.

### The High Voltage Half−bridge Driver

The driver features a traditional bootstrap circuitry, requiring an external high voltage diode with resistor in series for the capacitor refueling path. Minimum series resistor $R_{BOOT}$ value is 3.3 Ω. Figure 65 shows the internal architecture of the drivers section. The device incorporates an upper UVLO circuitry that makes sure enough $V_{GS}$ is available for the upper side MOSFET.

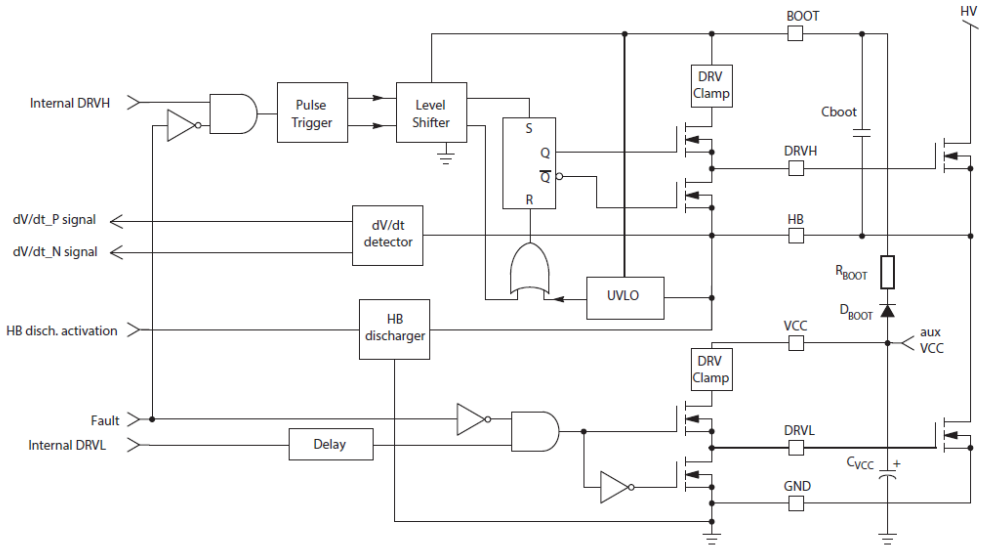



**Figure 65. The NCL30159 Internal DRVs Structure**

The internal dV/dt sensor, connected to the VBOOT pin, detects the HB pin voltage transitions in order to setup the optimum DT period – please refer to Dead−Time chapter. The internal HV discharge switch is connected to the HB pin and discharges resonant capacitor before application startup. The current through the switch is regulated to $I_{DISCHARGE}$ level until the $V_{HB\_MIN}$ threshold voltage is reached on the HB pin. The discharge system assures always the same startup conditions for application – regardless of previous operating state.

As stated in the maximum ratings section, the floating portion can go up to 730 $V_{DC}$ on the VBOOT pin. This voltage range makes the IC perfectly suitable for offline applications featuring a 400 V PFC front stage.

### Automatic Dead−time Adjust

The dead−time period between the DRVH and DRVL drivers is always needed in half bridge topologies to prevent any cross conduction through the power stage MOSFETs that would result in excessive current, high EMI noise generation or total destruction of the application. Fixed dead−time period is often used in the resonant converters because this approach is simple to implement. However, this method does not ensure optimum operating conditions in resonant topologies because the magnetizing current is changing with line and load conditions. The optimum dead−time, under a given operating conditions, is equal to the time that is needed for bridge voltage to transition between upper and lower states and vice versa – refer to Figure 66.

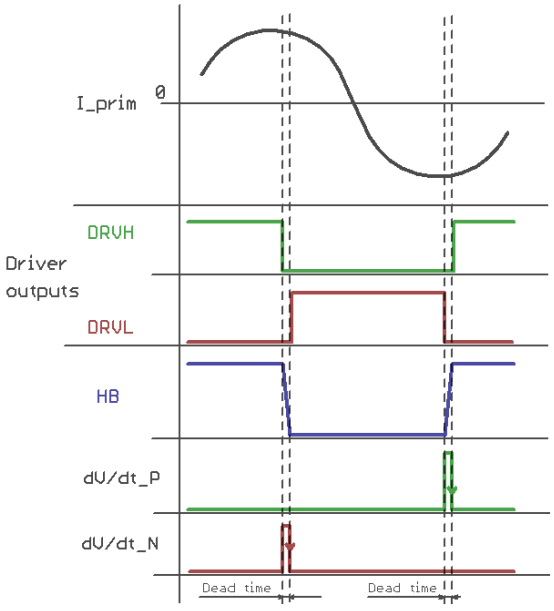



**Figure 66. Optimum Dead−time Period Adjust**

The MOSFET body diode conduction time is minimized when optimum dead−time period is used which results in maximum efficiency of a resonant converter power stage. There are several methods to determine the optimum dead−time period or to approximate it (for example using auxiliary winding on main transformer or modulating dead−time period with operating frequency of the converter). These approaches however require a dedicated pin for nominal dead−time adjust or auxiliary winding voltage sensing. The NCL30159 uses a dedicated method that senses the VBOOT pin voltage internally and adjusts the optimum dead−time period with respect to the actual operating conditions of the converter. The high−voltage dV/dt detector, connected to the VBOOT pin, delivers two internal digital signals that are indicating DRVH to DRVL and DRVL to DRVH transitions that occur on the HB and VBOOT pins after the corresponding MOSFET switch is turned−off. The controller enables the opposite MOSFET in the power stage once the corresponding dV/dt sensor output provides information about HB (or VBOOT) pin transition ends.

The ZVS transition on the bridge pin (HB) could take a longer time or even does not finish in some cases – for example with extremely low bulk voltage or when some critical failure occurs. This situation should not occur normally in correctly designed application because several other protections would prevent such a situation. The NCL30159 implements maximum DT period clamp that limits driver's off−time period to the $t_{DEAD\_TIME\_MAX}$ value. The corresponding MOSFET driver is forced to turn−on by the internal logic regardless of missing dV/dt sensor signal. This situation does not occur during normal operation and will be considered a fault state by the device. There are several possibilities on how the controller continues operation after this event occurrence – depending on the IC option:

1. The opposite MOSFET switch is forced to turn−on when $t_{DEAD\_TIME\_MAX}$ period elapses and no fault is generated
2. The controller is latched−off in case the ZVS condition is not detected within selected $t_{DEAD\_TIME\_MAX}$ period
3. The controller is latched−off in case the ZVS condition is not detected within selected $t_{DEAD\_TIME\_MAX}$ period

A DT fault counter option is available. Selected number ($N_{DT\_MAX}$) or DT fault events have to occur in order to confirm DT fault in this case.

A fixed DT option is also available for this device. The internal dV/dt sensor signal is not used for this device option and the $t_{DEAD\_TIME\_MAX}$ period is used as a regular DT period instead. The DT fault detection is disabled in this case.

### ON−time Modulation and Feedback Loop Block

The NCL30159 on−time modulation uses current mode control scheme that ensures best transient response performance and provides inherent cycle−by−cycle over−current protection feature in the same time. The current mode control principle used in this device can be seen in Figure 67.

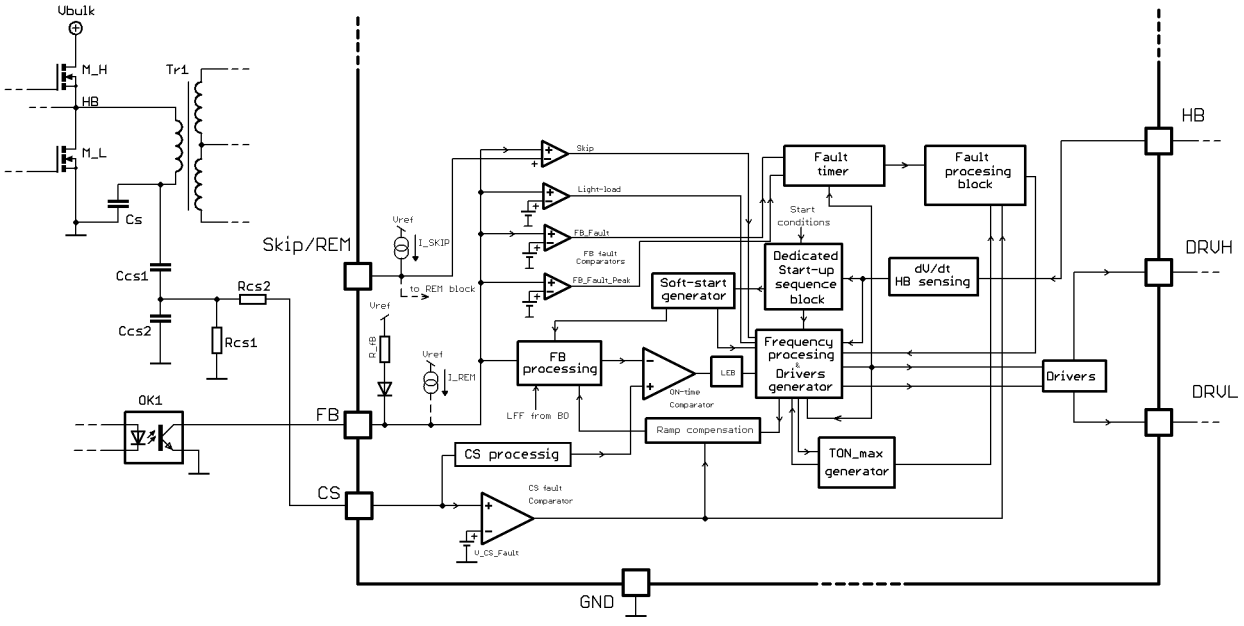



**Figure 67. Internal Connection of the NCL30159 Current Mode Control Scheme**

The basic principle of current mode control scheme implementation lies in the use of an ON−time comparator that defines upper switch on−time by comparing voltage ramp, derived from the current sense input voltage, to the divided or not divided feedback pin voltage. The upper switch on−time is then re−used for low side switch conduction period. The switching frequency is thus defined by the actual primary current and output load conditions. Digital processing with 10 ns minimum on−time resolution is implemented to ensure high noise immunity. The ON−time comparator output is blanked by the leading edge blanking ($t_{LEB}$) after the DRVH switch is turned−on. The ON−time comparator LEB period helps to avoid false triggering of the on−time modulation due to noise generated by the HB pin voltage transition.

The voltage signal for current sense input is prepared externally via natural primary current integration by the resonant tank capacitor Cs. The resonant capacitor voltage is divided down by capacitive divider (Ccs1, Ccs2, Rcs1, Rcs2) before it is provided to the CS input. The capacitive divider division ratio, which is fully externally adjustable, defines the maximum primary current level that is reached in case of maximum feedback voltage – i.e. the capacitive divider division ration defines the maximum output power of the converter for given bulk voltage. The CS pin is a bipolar input where an input voltage swing is restricted to ±5 V. The CS pin signal is also used for secondary side short circuit detection – please refer to chapter dedicated to short circuit protection.

A fixed voltage offset is internally process to the FB pin signal in order to assure enough voltage margin for operation the feedback opto−coupler − the FB opto−coupler saturation voltage is ~ 0.15 V (depending on type). However, the CS pin useful signal for frequency modulation swings from 0 V, so current mode regulation would not work under light load conditions if no offset would be added.

The second input signal for the on−time comparator is derived from the FB pin voltage. This internal FB pin signal is also used for the following purposes: skip mode operation detection, Light−load mode detection, off−mode detection and overload / open FB pin fault detection. The detailed description of these functions can be found in each dedicated chapters. The internal pull−up resistor assures that the FB pin voltage increases when the opto−coupler LED becomes less biased – i.e. when output load is increased. The higher FB pin voltage implies a higher reference level for on−time comparator i.e. longer DRVH switch on−time and thus also higher output power. The FB pin features a precise voltage clamp which limits the internal FB signal during overload and startup. The FB pin signal passes through the FB processing block before it is brought to the ON−time comparator input. The FB processing block scales the FB signal down by a $K_{FB}$ ratio in order to limit the CS input dynamic voltage range and apply ramp compensation signal (to ensure stability of the current mode control scheme), FB freeze or LFF. The processed internal FB signal could be overridden by a Soft−start generator output voltage during device starts−up.

The actual operating frequency of the converter is defined based on the CS pin and FB pin input signals. The maximum output power of the converter, under given input voltage, is limited by maximum internal FB voltage clamp that is reached when opto−coupler provides no current. The maximum output power limit is bulk voltage dependent due to changing ratio between magnetizing and load primary current components. Line Feed Forward (LFF) system is implemented in the controller to compensate for maximum output power clamp variation. The LFF signal that is apply to internal FB voltage is VBULK pin voltage proportional. The different input voltage sensed by VBULK pin creates change on internal FB signal. The DRVH switch on−time is thus changed to represent similar FB pin voltage at constant load across different input voltage. The LFF signal is provided only when BO pin voltage exceeds BO_OK threshold voltage.

Please refer to Figure 68 and below description for better understanding principle of the NCL30159 frequency modulation system.

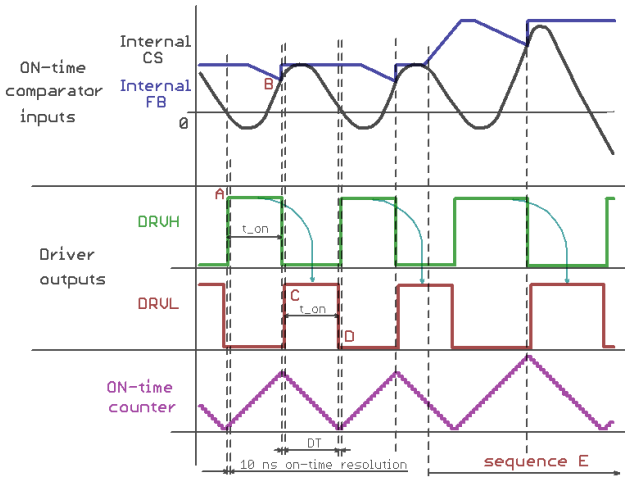



**Figure 68. NCL30159 On−time Modulation Principle**

The DRVH switch is activated by the controller after dead−time (DT) period elapses in point *A*. The frequency processing block increments the ON−time counter with 10 ns resolution until the internal CS signal crosses the internal FB set point for the ON−time comparator in point *B*. A DT period is then introduced by the controller to avoid any shoot−through current through the power stage switches. The DT period ends in point *C* and the controller activates the DRVL switch. The ON−time processing block decrements the ON_time counter down until it reaches zero. The DRVL switch is then turned−OFF at point *D* and the DT period is started. This approach results in perfect duty cycle symmetry for DRVL and DRVH switches. The DRVH switch on−time naturally increases and the operating frequency drops when the FB pin voltage is increased, i.e. when higher current is delivered by the converter output – sequence *E*.

The resonant capacitor voltage and thus also CS pin voltage can be out of balance in some cases – this is the case during transition from full load to no−load operation when skip mode is not used or adjusted correctly. The current mode operation is not possible in such case because the ON−time comparator output stays active for several switching cycles. Thus a special logic has been implemented in NCL30159 in order to repeat the last valid on−time until the current mode operation recovers – i.e. until the CS pin signal balance is restored by the system.

### Overload and Open FB Protections

The overload protection and open FB pin detection are implemented via FB pin voltage monitoring in this controller. The FB fault comparator is triggered once the FB pin voltage reaches the $V_{FB\_FAULT}$ level. The fault timer is then enabled – refer to Figure 69. The time period to the FB fault event confirmation is defined by the preselected $t_{FB\_FAULT\_TIMER}$ parameter. The fault timer is reset once the FB fault condition diminishes or timer counts down when cumulative option is selected. The speed of timer counting when timer counts up and down can be different. A digital noise filter has been added after the FB fault comparator to overcome false triggering of the FB fault timer due to possible noise on the FB input.

When FB pin voltage reaches $V_{FB\_FAULT\_PEAK}$ level (FB fault peak function is selected) the FB fault timer duration is reduced – i.e. the timer is speed up by multiplication $K_{FB\_PEAKFT\_MULT}$.

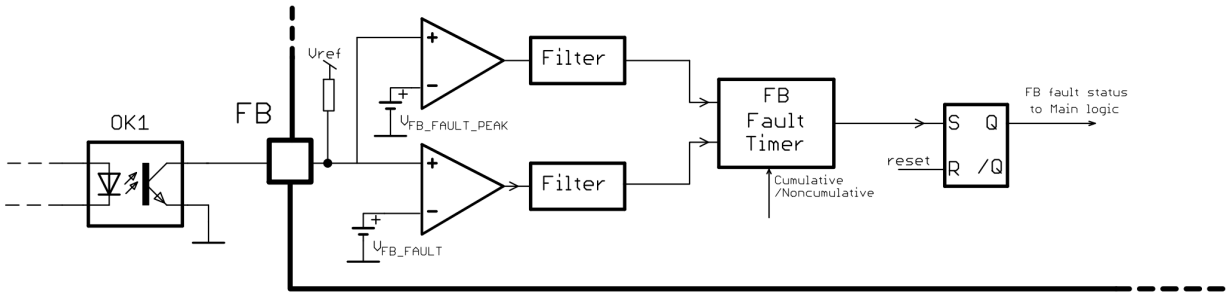



**Figure 69. Internal FB Fault Management**

The controller disables driver pulses and enters protection mode once the FB fault event is confirmed by the FB fault timer. Latched or auto−recovery operation is then triggered – depends on selected IC option. The controller adds an auto−recovery off−time period ($t_{A-REC\_TIMER}$) and restarts the operation via soft start in case of auto−recovery option. The application temperature runaway is thus avoided in case of overload while the automatic restart is still possible once the overload condition disappears. The IC with latched FB fault option stays latched−off, supplied by the HV startup current source working in DSS mode, until the $V_{CC\_RESET}$ threshold is reached on the VCC pin or Line event is detected by HV pin – i.e. until user unplug power supply from the mains.

Please refer to Figure 85 and Figure 86 for an illustration of the NCL30159 FB fault detection block.

### Secondary Short Circuit Detection with Primary and Secondary Current Reduction

The protection system described previously, implemented via FB pin voltage level detection, prevents continuous overload operation and/or open FB pin conditions. The primary current is naturally limited by the NCL30159 on−time modulation principle in this case. But the primary current increases when the output terminals are shorted. The NCL30159 controller will maintain zero voltage switching operation in such case, however high currents will flow through the power MOSFETS, transformer winding and secondary side rectification. The NCL30159 implements a dedicated secondary side short circuit protection system that will shut down the controller much faster than the regular FB fault event in order to limit the stress of the power stage components. The CS pin signal is monitored by the

dedicated CS fault comparator – refer to Figure 67. The CS fault counter is incremented each time the CS fault comparator is triggered. The controller enters auto−recovery or latched protection mode (depending on IC option) in case the CS fault counter overflows refer to Figure 70. The CS fault counter is then reset once the CS fault comparator is inactive for at least $N_{CS\_FAULT\_DEC}$ DRVH upcoming pulses. This digital filtering improves CS fault protection system noise immunity.

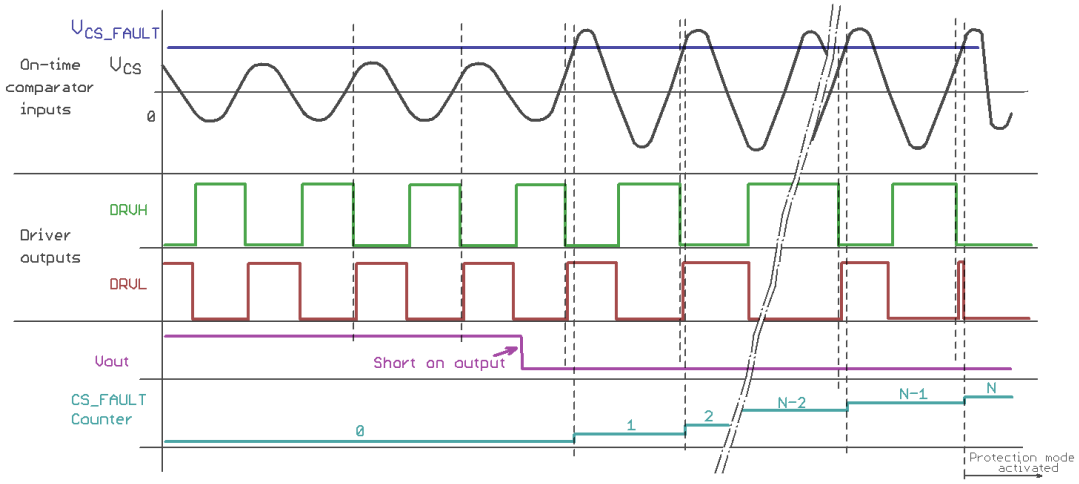



**Figure 70. NCL30159 CS Fault Principle**

The CS fault comparator event increases Ramp compensation (RC) gain by an increment $K_{RC\_GAIN\_INC}$ that is a portion of selected nominal RC gain. The RC gain is reduced to nominal level by a decrement when event of CS fault cmp. is not present for $N_{CS\_FAULT\_DEC}$ DRVH driver pulses. The decrement that is equal to increment is then placed at each followed DRVH driver pulse until RC gain reach nominal value or new CS fault cmp event is detected.

### Dedicated Startup Sequence and Soft−Start

Hard switching conditions can occur in a resonant SMPS application when the resonant tank operation is started with 50 % duty cycle symmetry – refer to Figure 71. This hard switching appears because the resonant tank initial conditions are not optimal for the clean startup.

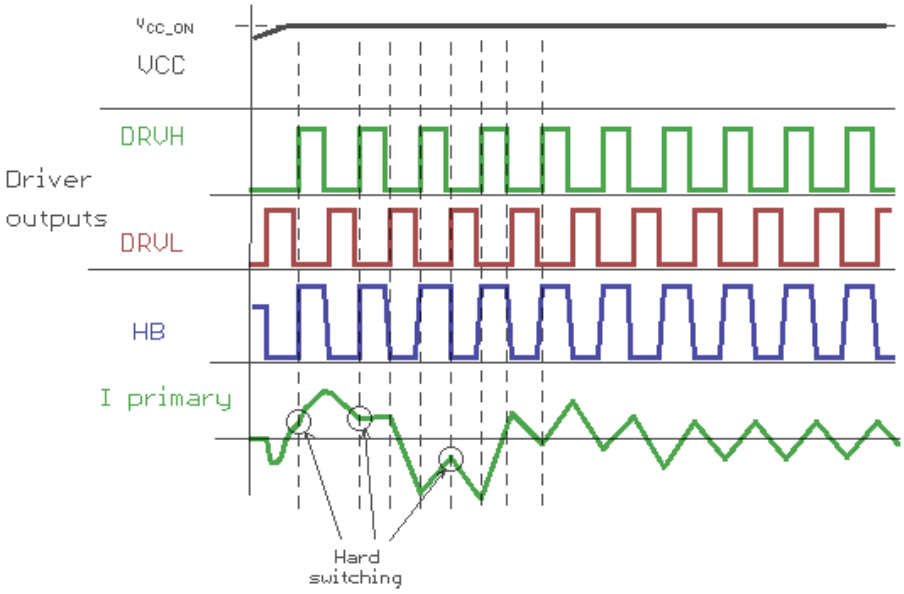



**Figure 71. Hard Switching Cycle Appears in the LLC Application when Resonant Tank is Excited by 50 % Duty Cycle During Startup**

The initial resonant capacitor voltage level can differ depending on how long delay was placed before application operation restart. The resonant capacitor voltage is close to zero level when application restarts after very long delay – for example several seconds, when the resonant capacitor is discharged by leakage to the power stage. However, the resonant capacitor voltage value can be anywhere between $V_{BULK}$ and 0 V when the application restarts operation after a short period of time – like during periodical SMPS turn−on/off. Another factor that plays significant role during resonant power supply startup is the actual load impedance seen by the power stage during the first pulses of startup sequence. This impedance is not only defined by resonant tank components but also by the output loading conditions and actual output voltage level. The load impedance of resonant tank is low when the output is loaded and/or the output voltage is low enough to made secondary rectifies conducting during first switching cycles of startup phase. The resonant frequency of the resonant tank is given by the resonant capacitor capacitance and resonant inductance −note that the magnetizing inductance does not participate in resonance in this case. However, if the application starts−up when the output capacitors is charged and there is no load connected to the output, the secondary rectification diodes is not conducting during each switching cycle of startup sequence and thus the resonant frequency of resonant tank is affected also by the magnetizing inductance. In this case, the resonant frequency is much lower than in case of startup into loaded/discharged output.

These facts show that a clean, hard switching free and parasitic oscillation free, startup of an LLC converter is not an easy task, and cannot be achieved by duty cycle imbalance and/or simple resonant capacitor pre−charge to $V_{BULK}/2$ level. These methods only work in specific startup conditions.

This explains why the NCL30159 implements a proprietary startup sequence – see Figure 72 and Figure 73. The resonant capacitor is discharged down to $V_{HB\_MIN}$ before any application restart – except when restarting from skip mode.

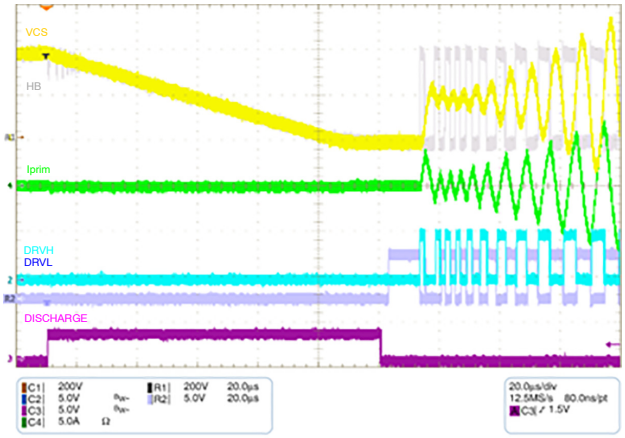



**Figure 72. Initial Resonant Capacitor Discharge Before Dedicated Startup Sequence is Placed**

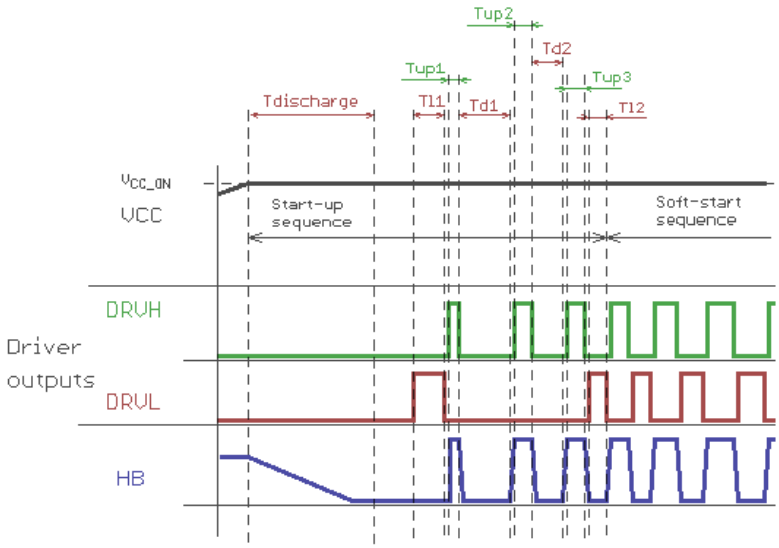



**Figure 73. Dedicated Startup Sequence Detail**

The resonant capacitor discharging process is simply implemented by activating an internal current limited switch connected between the HB pin and IC ground – refer to Figure 72. This technique assures that the resonant capacitor energy is dissipated in the controller without ringing or oscillations that could swing the resonant capacitor voltage to a positive or negative level. The controller detects that the discharge process is complete via HB pin voltage level monitoring. The discharge switch is disabled once the HB pin voltage drops below the $V_{HB\_MIN}$ threshold.

The dedicated startup sequence continues by activation of the DRVL driver output for $T_{l1}$ period (refer to Figure 73). This technique ensures that the bootstrap capacitor is fully charged before the first high−side driver pulse is introduced by the controller. The first DRVH switch on−time $T_{up1}$ period is fixed and depends on the application parameters. This period can be adjusted internally – various IC options are available. The DRVH switch is released after $T_{up1}$ period and it is not followed by the DRVL switch activation. The controller waits for a new ZVS condition for DRVH switch instead and measures actual resonant tank conditions this way. The DRVH switch is then activated again after the DRVL blank period is used for measurement purposes. The second DRVH driver conduction period is then dependent on the previously measured conditions:

a. The DRVH switch is activated for 3/2 of previous DRVH conduction period in case the measured time between previous DRVH turn−off event and upper ZVS condition detection is equal or higher than two times of the the previous DRVH pulse conduction period.

b. The DRVH switch is activated for previous DRVH conduction period in case the measured time between previous DRVH turn−off event and upper ZVS condition detection is lower than two times of previous DRVH pulse conduction period.

c. ZVS condition is not detected due to low or no positive voltage swing on HB pin. Internal logic is waiting for ZVS information without any time limitation – i.e. stuck state. The stuck state can be interrupted by IC reset (via $V_{CC\_RESET}$ threshold) or by startup watchdog timer.

The startup period then depends on the previous condition. Another blank DRVL switch period is placed by the controller in case condition a) occurred. A normal DRVL driver pulse, with DC of 50 % to previous DRVH DRV pulse, is placed in case condition b) is fulfilled.

The dedicated startup sequence is placed after the resonant capacitor is discharged (refer to Figure 72 and Figure 73) in order to exclude any hard switching cycles during the startup sequence. The first DRVH switch cycle in startup phase is always non−ZVS cycle because there is no energy in the resonant tank to prepare ZVS condition. However, there is no energy in the resonant tank at this time, there is also no possibility that the power stage MOSFET body diodes conducts any current. Thus the hard commutation of the body diode cannot occur in this case.

The IC will not start and provide regular driver output pulses until it is placed into the target application, because the startup sequence cannot be finished until HB pin signal is detected by the system. The IC features a startup watchdog timer ($t_{WATCHDOG}$) which restarted a dedicated startup sequence periodically in case the IC is powered without application (during bench testing) or in case the startup sequence is not finished correctly. The first DRVH on−time duration is automatically incremented when IC is restarted by the startup watchdog (depends on IC option). The increment is a portion of selected first DRVH duration and the first DRVH on−time duration can be incremented up to two times of preselected first DRVH duration. The IC will provide the first DRVL and first DRVH DRV pulses with a $t_{WATCHDOG}$ off−time in−between startup attempts.

### Soft−start

The dedicated startup sequence is complete when condition b) from previous chapter is fulfilled and the controller continues operation with the soft−start sequence. A fully digital non−linear soft−start sequence has been implemented in NCL30159 using a soft−start counter and D/A converter that are gradually incremented by the DRVL driver pulses. A block diagram of the NCL30159 soft−start system is shown at Figure 74.

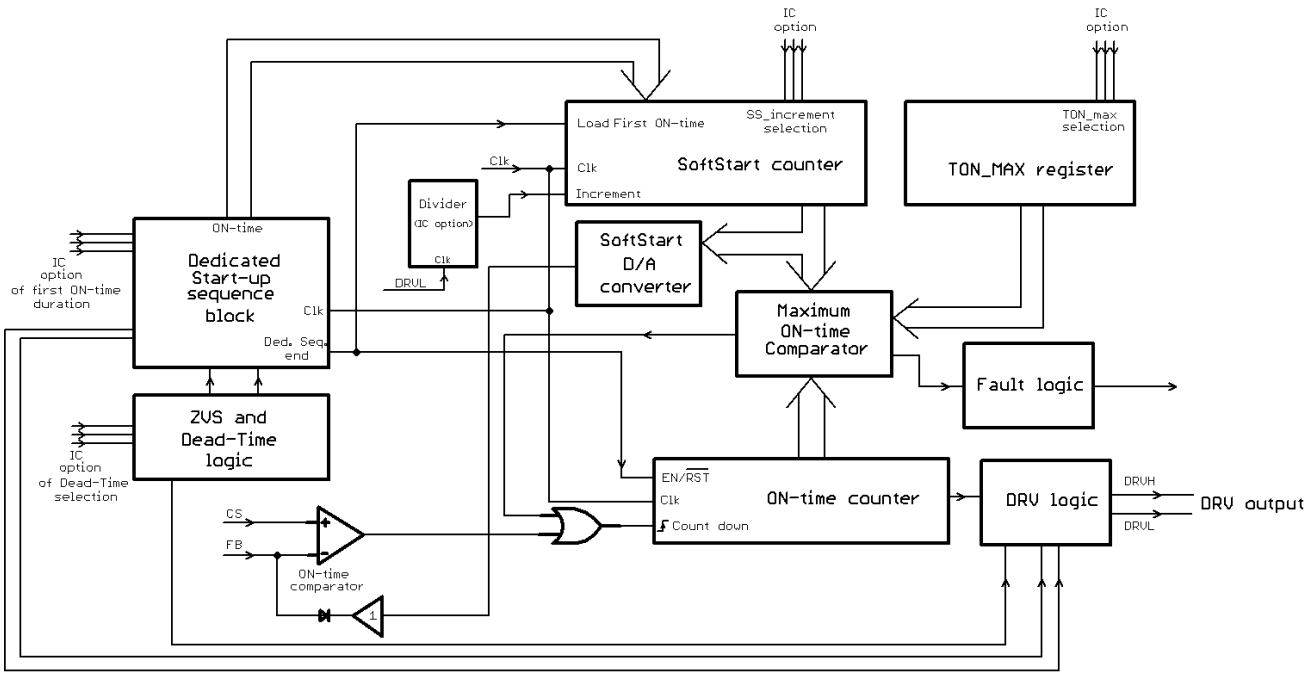



**Figure 74. Soft−start Block Internal Implementation**

The soft−start block subsystems and operation are described below:

1. The *Soft−Start counter* is a unidirectional counter that is loaded with the last DRVH on−time value that is reached at the dedicated startup sequence end (i.e. during condition b occurrence explained in previous chapter). The on−time period used in the initial period of the soft−start sequence is affected by the first DRVH on−time period selection and the dedicated startup sequence processing. The Soft−Start counter counts up from this initial on time period to its maximum value which corresponds to the IC maximum on−time ($t_{TON\_MAX}$). The Soft−Start counter is incremented by the soft−start increment number ($t_{TON\_SS\_INC}$) during each DRVL switch on−time period. The soft−start start increment, selectable via IC option, thus affects the soft−start time duration. The DRVL clock signal for the Soft−Start counter can be divided down by the SS clock divider ($K_{FB\_SS\_INC}$) in case the soft−start period needs to be prolonged further – this can be also done via IC option selection. The Soft−Start period is terminated (i.e. the counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB\_SKIP\_IN}$ level or FB pin detect that application is under regulation.
2. The *ON−time counter* is a bidirectional counter that is used as a main system counter for on−time modulation during soft−start, normal operation or overload conditions. The ON−time counter counts−up during DRVH switch conduction period and then counts down to zero – defining DRVL switch conduction period. This technique assures perfect 50 % duty cycle symmetry for both power switches as afore mentioned. The ON−time counter count−up mode can be switched to the count−down mode by either of two events: *1st* when the ON−time counter value reaches the maximum on−time value ($t_{TON\_MAX}$) or *2nd* when the actual DRVH on−time is terminated based on the current sense input information – i.e. by ON−time comparator.
3. The *Maximum ON−time comparator* compares the actual ON−time counter value with the maximum on−time value ($t_{TON\_MAX}$) and activates the latch (or auto−recovery) protection mode once IC detect requested number of TON_MAX events. The minimum operating frequency of the controller is defined the same way. The Maximum ON−time comparator reference is loaded by the Soft−Start counter value on each switching cycle during soft−start. The Maximum ON−time fault signal is ignored during Soft−Start operation. The converter DRVH switch on−time (and thus operating frequency) is thus defined by the Soft−Start counter value indirectly – via Maximum ON−time comparator. The DRVH switch on−time is increased until the Soft−Start counter reaches $t_{TON\_MAX}$ period and Maximum on−time protection is activated, or until ON−time comparator takes action and overrides the Maximum ON−time comparator.
4. The *Soft−Start D/A converter* generates a soft−start voltage ramp for ON−time comparator input synchronously with Soft−Start counter

incrementing. The internal FB signal for ON−time comparator input is artificially pulled−down and then ramped−up gradually when soft−start period is placed by the system – refer to Figure 75. The FB loop is supposed to take over at certain point when regulation loop is closed and output gets regulated so that soft−start has no other effect on the on−time modulation. The Soft−Start counter continues counting−up until it reaches its maximum value which corresponds to the IC maximum on−time value – i.e. the IC minimum operating frequency. The Soft−Start period is terminated (i.e. counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB\_SKIP\_IN}$ level. The D/A converter output evolve accordingly to the Soft−Start counter as it is loaded from its output data bus.

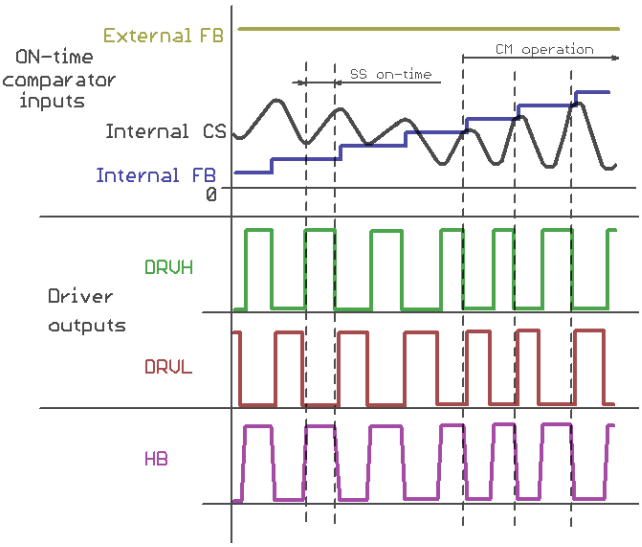



**Figure 75. Soft−start Behavior**

### The Controller Operation During Soft−start Sequence Evolves as Follows

The Soft−Start counter is loaded by last DRVH on−time value at the end of the dedicated startup sequence. The ON−time counter is released and starts count−up from zero until the value that is equal to the actual Soft−Start counter state. The DRVH switch is active during the time when ON−time counter counts−up. The Maximum ON−time comparator then changes counting mode of the ON−time comparator from count−up to count−down. A dead−time is placed and the DRVL switch is activated till the ON−time counter reaches zero value. The Soft−Start counter is incremented by selected increment during corresponding DRVL on−time period so that the following DRVH switch on−time is prolonged automatically – the frequency thus drops naturally. Because the operating frequency of the controller drops and DRVL DRV signal is used as a clock source for the Soft−start counter, the soft−start speed starts to decrease on each (or on each N−th) DRVL driver pulse (where N is defined by $K_{FB\_SS\_INC}$) of switching cycle. So we have non−linear soft−start that helps to speed up output charging in the beginning of the soft−start operation and reduces the output voltage slope when the output is close to the regulation level. The output bus of the Soft−Start counter addresses the D/A converter that defines the ON−time comparator reference voltage. This reference voltage thus also increases non−linearly from initial zero level until the level at which the current mode regulation starts to work. The on−time of the DRVH and DRVL switch is then defined by the ON−time comparator action instead of the Maximum ON−time comparator. The soft−start then continues until the regulation loop is closed and the on−time is fully controlled by the secondary regulator. The Soft−Start counter then continues in counting and saturates at its maximum possible value which corresponds to IC minimum operating frequency. The maximum on−time fault detection system is enabled when Soft−Start counter value is equal to $t_{TON\_MAX}$ value.

The previous on−time repetition feature, described above in the ON−time modulation and feedback loop chapter, is disabled in the beginning of soft start period. This is because the ON−time comparator output stays high for several cycles of soft start period – until the current mode regulation takes over. The previous on−time repetition feature is enabled once the current modulation starts to work fully, i.e. in the time when the ON−time comparator output periodically drops to low state within actual DRVH switch on−time period. Typical startup waveform of the LLC application driven by NCL30159 controller can be seen in Figure 76.

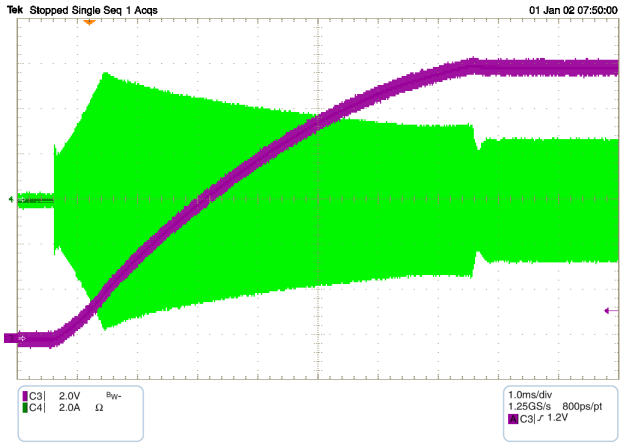



**Figure 76. Application Startup with NCL30159 – Primary Current – Green, Vout – Magenta**

### Skip Mode Operation

Then NCL30159 implements proprietary light load and quiet skip mode operating techniques that improve light load efficiency, reduce no−load power consumption and significantly reduce acoustic noise. Controller uses 50 % duty cycle symmetry under full and medium load conditions. Normal current mode frequency modulation takes place during this operating mode – refer to on−time processing section of this datasheet. The 50 % duty cycle symmetry operating mode is replaced by continues operation with minimum switching patterns repeated after controlled amount of off−time when load is decreased below preselected level. Zero voltage switching technique is still present for the power switches to achieve high light load efficiency. Quiet skip mode operation is initiated when load drops further and FB voltage drops below another FB threshold that is user adjustable on the skip pin. The frequency of skip burst is regulated by internal digital controller around preselected quiet skip frequency clamp in order to reduce acoustic noise. The skip frequency then drops to very low values during no−load conditions. Refer to Figure 77, Figure 78 and Figure 79 for typical application waveforms during light load and quiet skip mode operating modes.

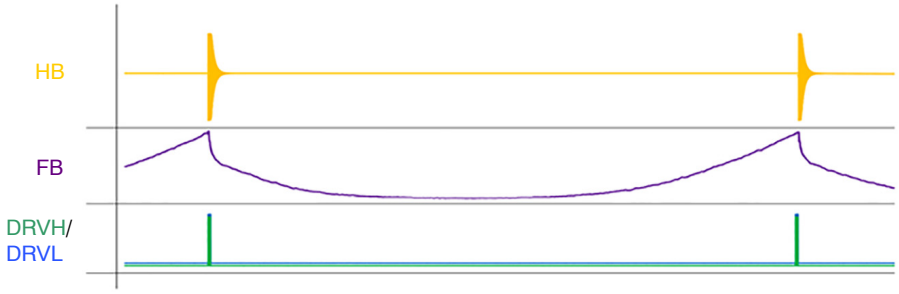



**Figure 77. No−load Operation**

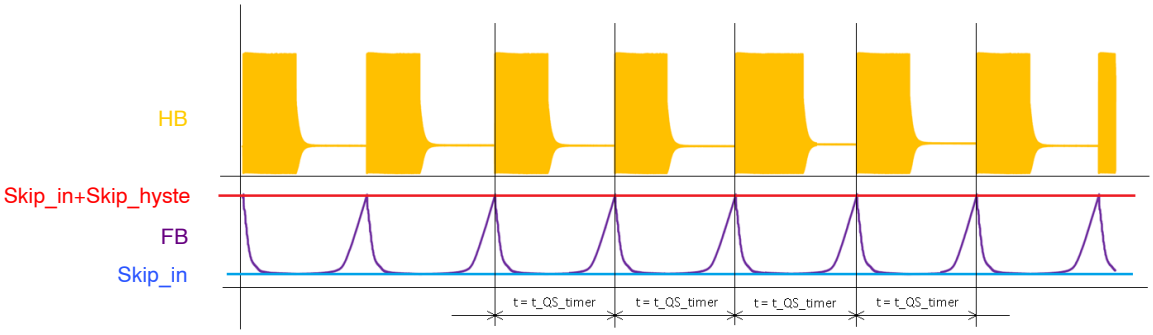



**Figure 78. Quiet Skip Mode Operation**

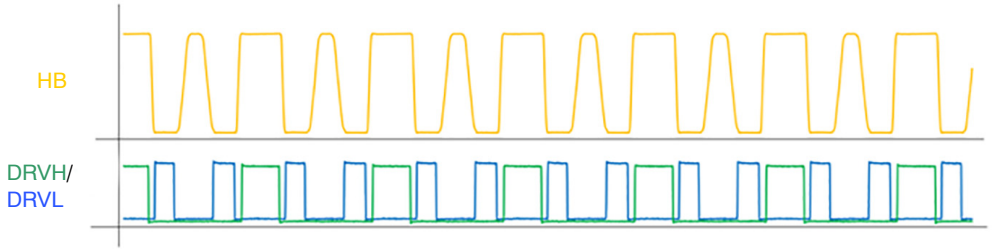



**Figure 79. Light−load Operation**

### PFC MODE Output

The NCL30159 has PFC MODE pin that can be used to disable or enable PFC stage operation based on actual application operating state – please refer to Figure 80. The PFC MODE output pin can be used for two purposes:

1st to control the external small signal HV MOSFET switch that connects the bulk voltage divider to the VBULK input.

2nd to control the PFC front stage controller operation via PFC controller supply pin.

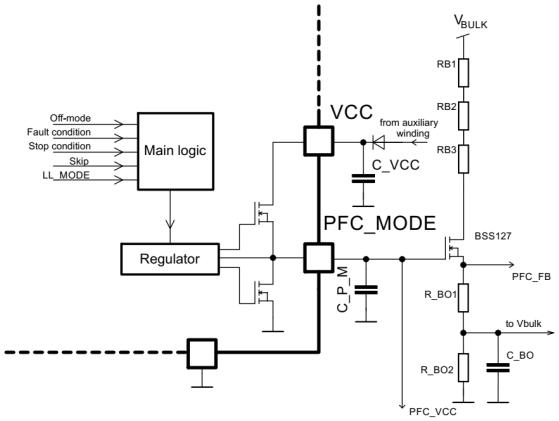



**Figure 80. Internal Connection of the PFC MODE Block**

There are three possible states of the PFC MODE output that can be placed by the controller based on the application operating conditions:

a. The PFC MODE output pin is pulled−down by an internal MOSFET switch before controller startup. This technique ensures minimum VCC pin current consumption in order to ramp $V_{CC}$ voltage in a short time from the HV startup current source. This approach speeds up the startup and restart time of an SMPS. The PFC MODE output pin is also pulled−down in off−mode, protection mode and at stop conditions (except BO event via VBUKL pin) during which the HV startup current source is operated in DSS mode. Application power consumption is reduced in above cases. The pull−down switch can be activate also in skip or light load mode (depends on IC version).

b. Second possible state of PFC MODE output is regulated voltage. The two regulated levels $V_{REG1}$ and $V_{REG2}$ are available. Regulation level $V_{REG1}$ is present on the output during normal operation and IC can switch to $V_{REG2}$ during skip or light−load modes. The purpose of switching between two voltage levels is to fully bias PFC controller during normal operation and keep limited bias (just below PFC controller VCC_off level) to keep PFC controller internal blocks biased with reduced consumption of PFC controller.

c. The PFC MODE can be also at High Z state during skip or light load mode to keep remaining charge of PFC controller VCC capacitor. The combination of High Z state with pull−down switch can be used to control Power Good (PG) opto−coupler.

**Table 1. PROTECTION MODES AND THE LATCH MODE RELEASES**

| Event | Timer Protection | Next Device Status | Release to Normal Operation Mode |
|---|---|---|---|
| Maximum current set−point sensed at CS pin | Fault timer | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| FB clamp | Fault timer | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| Maximum / constant power limit | No / Fault timer | Run at CP limit / Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| Maximum on time | $t_{TON\_MAX}$ event counter | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| Maximum Dead Time | Max $DT_{MAX}$ event counter | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| OVP | OVP filter | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| OTP | OTP filter | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| Low supply $V_{CC} < V_{CC(off)}$ | 10 μs timer | Latch | Autorecovery − depends on version Brown−out $V_{CC} < V_{CC(reset)}$ |
| Bulk Brown−out | BO filter | Device stops | $(V_{BO\_PIN} > V_{BO})\&(V_{CC} > V_{CC(on)})$ |
| AC brown−out $V_{HV} < V_{HV(stop)}$ | HV timer | Device stops | $(V_{HV} > V_{HV(start)})\&(V_{CC} > V_{CC(on)})$ |
| Internal TSD | 10 μs timer | Device stops, HV start−up current source stops | $(V_{HV} > V_{HV(start)})\&(V_{CC} > V_{CC(on)})\&$TSDb |

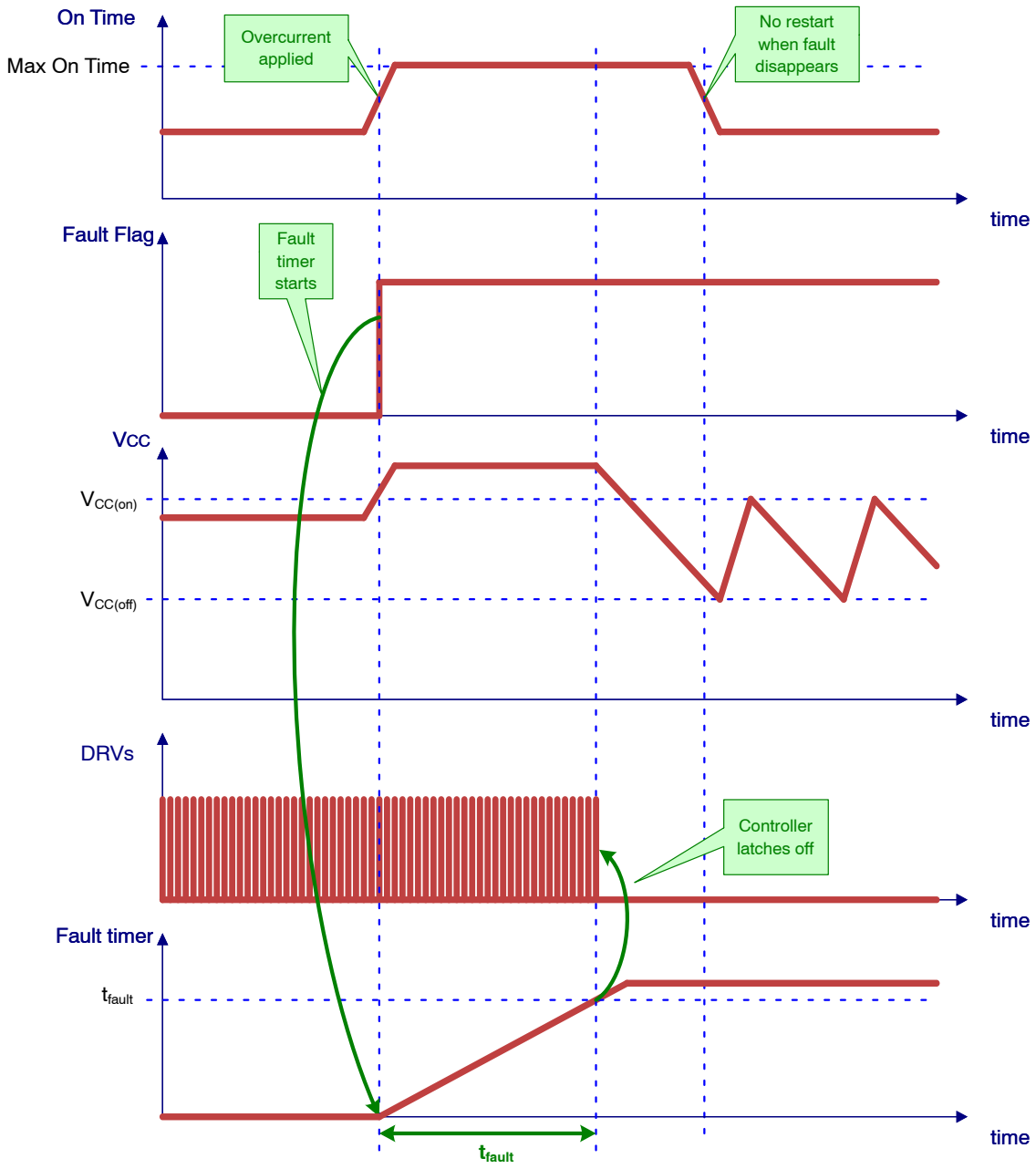



**Figure 81. Latched Timer−based Overcurrent Protection**

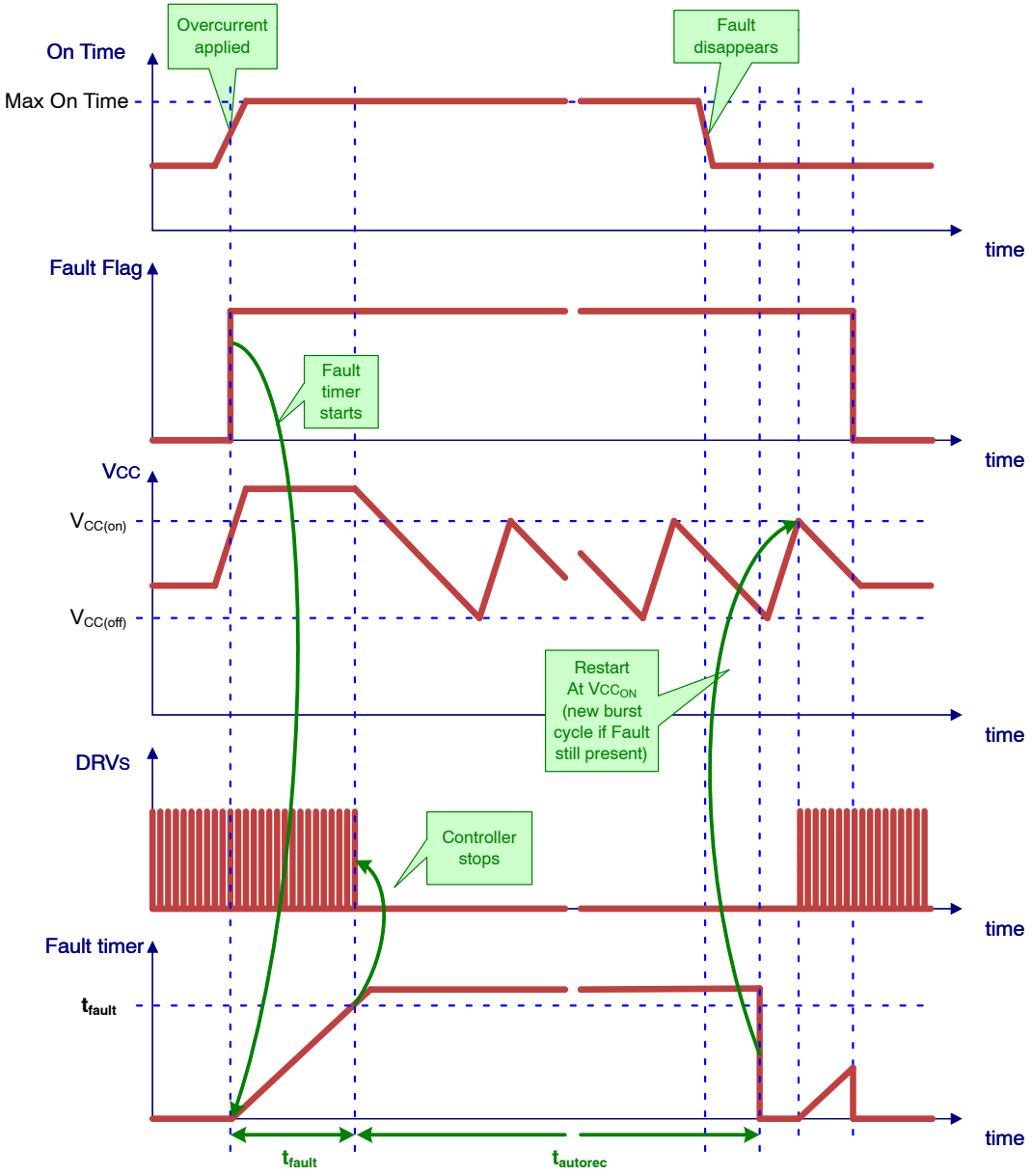



**Figure 82. Timer−based Protection Mode with Autorecovery Release from Latch−off**

### Maximum Power Limit

The NCL30159 implements maximum power limit feature. This simple system ignores the LLC stage efficiency shift at different operating points at high power level, that's why the input bulk voltage and input average current flowing into LLC stage are sensed.

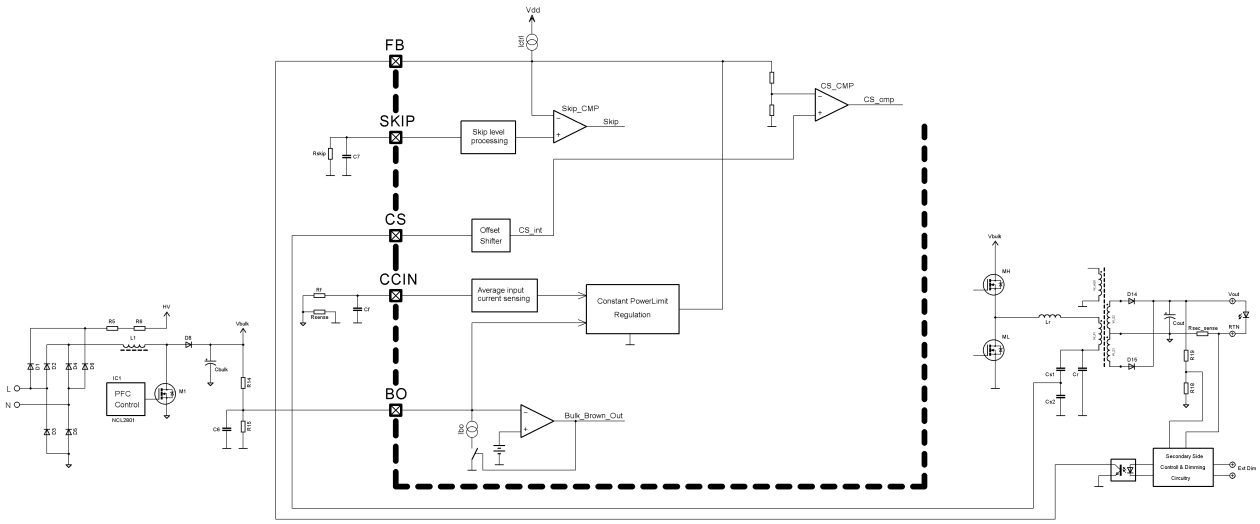



**Figure 83. Principal Schematic of the Maximum Power Limit**

### Over−voltage and Over−temperature Protection

The OVP/OTP pin is a dedicated input to allow for a simple and cost effective implementation of two key protection features that are needed in adapter applications: over−voltage (OVP) and over−temperature (OTP) protections. Both of these protections can be either latched or auto−recovery− depending on the version of NCL30159. The OVP/OTP pin has two voltage threshold levels of detection ($V_{OVP}$ and $V_{OTP}$) that define a no−fault window. The controller is allowed to run when OVP/OTP input voltage is within this working window. The controller stops the operation, after filter time delay, when the OVP/OTP input voltage is out of the no−fault window. The controller then either latches−off or or starts an auto−recovery timer − depending on the IC version − and triggered the protection threshold ($V_{OTP}$ or $V_{OVP}$).

The internal current source $I_{OTP}$ allows a simple OTP implementation by using a single negative temperature coefficient (NTC) thermistor. An active soft clamp composed from $V_{clamp}$ and $R_{clamp}$ components prevents the OVP/OTP pin voltage from reaching the $V_{OVP}$ threshold when the pin is pulled up by the $I_{OTP}$ current. An external pull−up current, higher than the pull−down capability of the internal clamp ($V_{CLAMP\_OVP/OTP}$), has to be applied to pull the OVP/OTP pin above $V_{OVP}$ threshold to activate the OVP protection. The $t_{OVP\_FILTER}$ and $t_{OTP\_FILTER}$ filters are implemented in the system to avoid any false triggering of the protections due to application noise and/or poor layout.

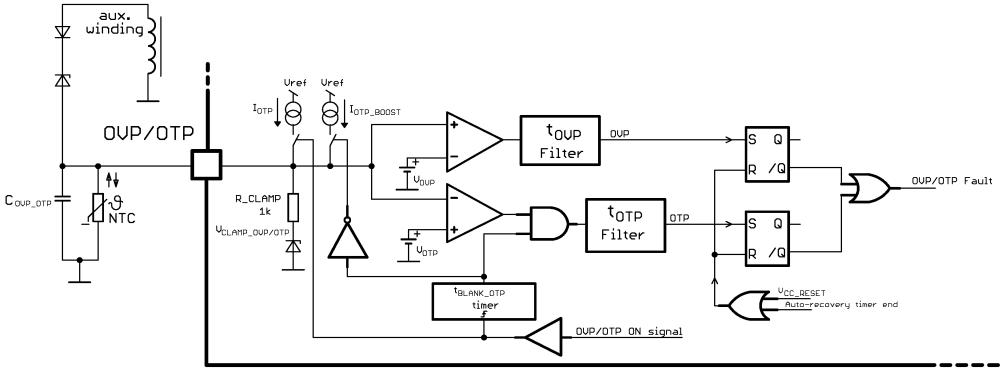



**Figure 84. Internal Connection of OVP/OTP Input**

The OTP protection could be falsely triggered during controller startup due to the external filtering capacitor charging current. Thus the $t_{BLANK\_OTP}$ period has been implemented in the system to overcome such behavior. The OTP comparator output is ignored during $t_{BLANK\_OTP}$ period. In order to speed up the charging of the external filtering capacitor $C_{OVP\_OTP}$ connected to OVP/OTP pin, the $I_{OTP}$ current has been doubled to $I_{OTP\_BOOST}$. The maximum value of filtering capacitor is 100 nF.

The OVP/OTP ON signal is set after the following events:

– the $V_{CC}$ voltage exceeds the $V_{CC\_RESET}$ threshold during first start−up phase (after VCC pin voltage was below $V_{CC\_RESET}$ threshold)

– IC returns from non−switching states to switching state (like bulk BO, line BO, line OVP and VCC_OFF protections, auto−recovery…) except hysteretic mode of OTP protection

The $I_{OTP}$ current source is disabled when:
– DRVs stop switching

IC option that keeps OVP/OTP block working during skip mode is also available. The IC consumption is increased for this version by OVP/OTP block bias.

OTP protection can operate (based on IC version) at hysteretic mode where DRVs are stopped when voltage on the pin drops below low threshold and operation is restarted once voltage on the pin increase above high threshold.

The latched OVP or OTP versions of NCL30159 enters latched protection mode when $V_{CC}$ voltage cycles between $V_{CC\_ON}$ and $V_{CC\_OFF}$ thresholds and no pulses are provided by drivers. The controller VCC pin voltage has to be cycled down below $V_{CC\_RESET}$ threshold or appropriate conditions on HV pin have to occur in order to restart operation. This would happen when the power supply is unplugged from the mains.

### Temperature Shutdown

The NCP30159 includes a temperature shutdown protection with a trip point typically at 150°C and the typical hysteresis of 40°C. When the temperature rises above the high threshold, the controller stops switching instantaneously, and goes to the off mode with extremely low power consumption. There is kept the $V_{CC}$ supply to keep the TSD information. When the temperature falls below the low threshold, the start−up of the device is enabled again, and a regular start−up sequence takes place.

### Controller Operation Sequencing of NCL30159 LLC Controller

The paragraphs below describe controller operation sequencing under several typical cases as well as transitions between them.

*Application start, Brown−out off and restart, OVP/OTP latch and then restart* – Figure 85

Application is connected to the mains at point *A* thus the HV input of the controller becomes biased. The HV startup current source starts charged VCC capacitor until $V_{CC}$ reaches $V_{CC\_ON}$ threshold.

The all analog blocks are enabled at $V_{CC\_RESET}$ threshold. A START_BLANK is activated at $V_{CC\_RESET}$ threshold also to ensure that the internal blocks are fully biased and stabilized to correctly process conditions/faults before IC start. The VCC pin voltage reached $V_{CC\_ON}$ threshold in point *B*. The PFC front stage is activated via PFC MODE pin that change status at mentioned threshold. The IC DRVs were not enabled after first $V_{CC\_ON}$ threshold in this case as the voltage on VBULK is not enough high. The IC keeps all internal blocks biased and operates in the DSS (Dynamic Self−Supply) mode as long as the stop conditions is still present.

The BO_OK condition is received (voltage on VBULK reach $V_{BO}$ level affected by hysteresis) at point *C*. The IC activates the startup current source to refill VCC capacitor in order to assure sufficient energy for a new startup. The VCC capacitor voltage reaches $V_{CC\_ON}$ level again. The DRVs are enabled and the application is started because there is no faults or stop condition at that time.

Line and also bulk voltage drops at point D so the BO_OK signal become low (voltage on VBULK drops below $V_{BO}$ level). The LLC DRVs are disabled as well as OVP/OTP block bias. The PFC MODE output stay high to keep the PFC controller biased, so the BO block still monitors the bulk voltage. The controller activates the HV startup current source into DSS mode to keep enough VCC voltage for operation of all blocks that are active while the IC is waiting for BO_OK condition.

The line voltage and thus also bulk voltage increase at point *E* so the Brown−out block provide the BO_OK signal once the $V_{BO}$ (with hysteresis) level is reached. The startup current source is activated after BO_OK signal is received to charge the VCC capacitor for a new restart. The analog blocks are enabled (biased) including START_BLANK period at time when BO_OK signal is received.

The $V_{CC\_ON}$ level is reached in point *F*. The controller restores operation via the regular startup sequence and soft−start after all startup condition are fulfil (no fault or stop condition detected and VCC is higher when $V_{CC\_ON}$ threshold).

The application then operates normally until the OVP/OTP input is pulled−up at point *G*. The controller then enters latch−off mode in which all blocks are disabled. The VCC management controls the HV startup in DSS mode in order to keep enough VCC level to hold the latch−up state memorized while the application remains plugged−in to the mains.

The power supply is removed from the mains at point *H* and the VCC voltage drops down below $V_{CC\_RESET}$ level thus the controller is released from latch. A new application start occurs when the user plugs the application the mains again.

*Application start, Brown−out off and restart, output short fault with auto−recovery restart* – Figure 86

Operating waveforms descriptions for this figure is similar to one for Figure 85 from point *A* till point *G*

The LLC converter operation is stopped in point *G* because the controller detects an overload condition (short circuit event in this case as the Vout drops abruptly). The controller disables almost all blocks. The HV startup DSS operation is initiated in order to keep enough VCC level for all internal blocks that need to be biased. Internal auto−recovery timer counts down the recovery delay period $t_{A-REC\_TIMER}$.

The auto−recovery restart delay period lapses at point *H*. The HV startup current source is activated to recharge VCC capacitor before a new restart and all block are enabled with START_BLANK period.

The $V_{CC\_ON}$ threshold is reached in point *I*. The controller restores operation via the regular startup sequence and soft−start after all startup condition are fulfil (no fault or stop condition detected and VCC is higher when $V_{CC\_ON}$ threshold). The LLC converter operation is enabled, including a dedicated startup and soft−start period. The output short circuit is removed in between thus the Vout ramped−up and the FB loop took over during the LLC converter soft−start period.

*Startup, skip−mode operation, low line detection and restart into skip−mode* – Figure 87

Application is connected to the mains at point *A* thus the HV input of the controller becomes biased. The HV startup current source starts charged VCC capacitor until $V_{CC}$ reaches $V_{CC\_ON}$ threshold.

The all analog blocks are enabled at $V_{CC\_RESET}$ threshold. A START_BLANK is activated at $V_{CC\_RESET}$ threshold also to ensure that the internal blocks are fully biased and stabilized to correctly process conditions/faults before IC start. The VCC pin voltage reached $V_{CC\_ON}$ threshold in point *B*. The PFC front stage is activated via PFC MODE pin that change status at mentioned threshold. The IC DRVs were not enabled after first $V_{CC\_ON}$ threshold in this case as the voltage on VBULK is not enough high. The IC keeps all internal blocks biased and operates in the DSS (Dynamic Self−Supply) mode as long as the stop conditions is still present.

The controller authorizes DRVs at point *C* as there are no faults conditions present. The load current is reduced thus the FB loop reduces the primary controller FB pin voltage.

The load diminished further and the FB skip threshold is reached in point *D*. The controller turns−off all the blocks that are not essential for the controller operation during skip−mode – i.e. all blocks except FB block and VCC management. This technique is used to minimize the device consumption when there are no driver pulses during skip−mode operation. The output voltage then drops naturally and the FB loop reflects this change into the primary FB pin voltage that increases accordingly. The auxiliary winding is refilling VCC capacitor during each skip burst thus the controller is supplied from the application during the skip mode operation.

The controller FB skip−out threshold is reached in point *E***;** the controller enables all blocks and LLC DRVs to refill the output capacitor. The controller did not activate the HV startup current source because there is enough voltage present on the VCC pin during skip mode. The OTP blank periods is activated at the beginning of the skip burst to mask possible OTP faults.

The line voltage drops in point *F***,** but the bulk voltage is dropping slowly as there is nearly no consumption from the bulk capacitor during skip mode – only some refilling bursts are provided by the controller. The application thus continues in skip mode operation for several skip burst cycles.

The bulk voltage level less than $V_{BO}$ threshold is detected by the controller in point *G* during one of the skip burst pulses. The controller thus disabled DRVs and enters DSS mode of operation in which the OVP/OTP block is disabled and the controller is waiting for BO_OK event. The PFC MODE provides the $V_{PFCM\_REG1}$ voltage in this case to allow the PFC stage to refill bulk capacitors.

The line voltage is increased at point *H* thus the controller receives the BO_OK signal. The startup current source is activated after BO_OK signal is received to charge the VCC capacitor for a new restart. The analog blocks are enabled (biased) including START_BLANK period at time when BO_OK signal is received.

The $V_{CC\_ON}$ level is reached in point *I*. The controller restores operation via the regular startup sequence and soft−start after all startup condition are fulfil (no fault or stop condition detected and VCC is higher when $V_{CC\_ON}$ threshold). The application then enters skip mode again as the load current is low.

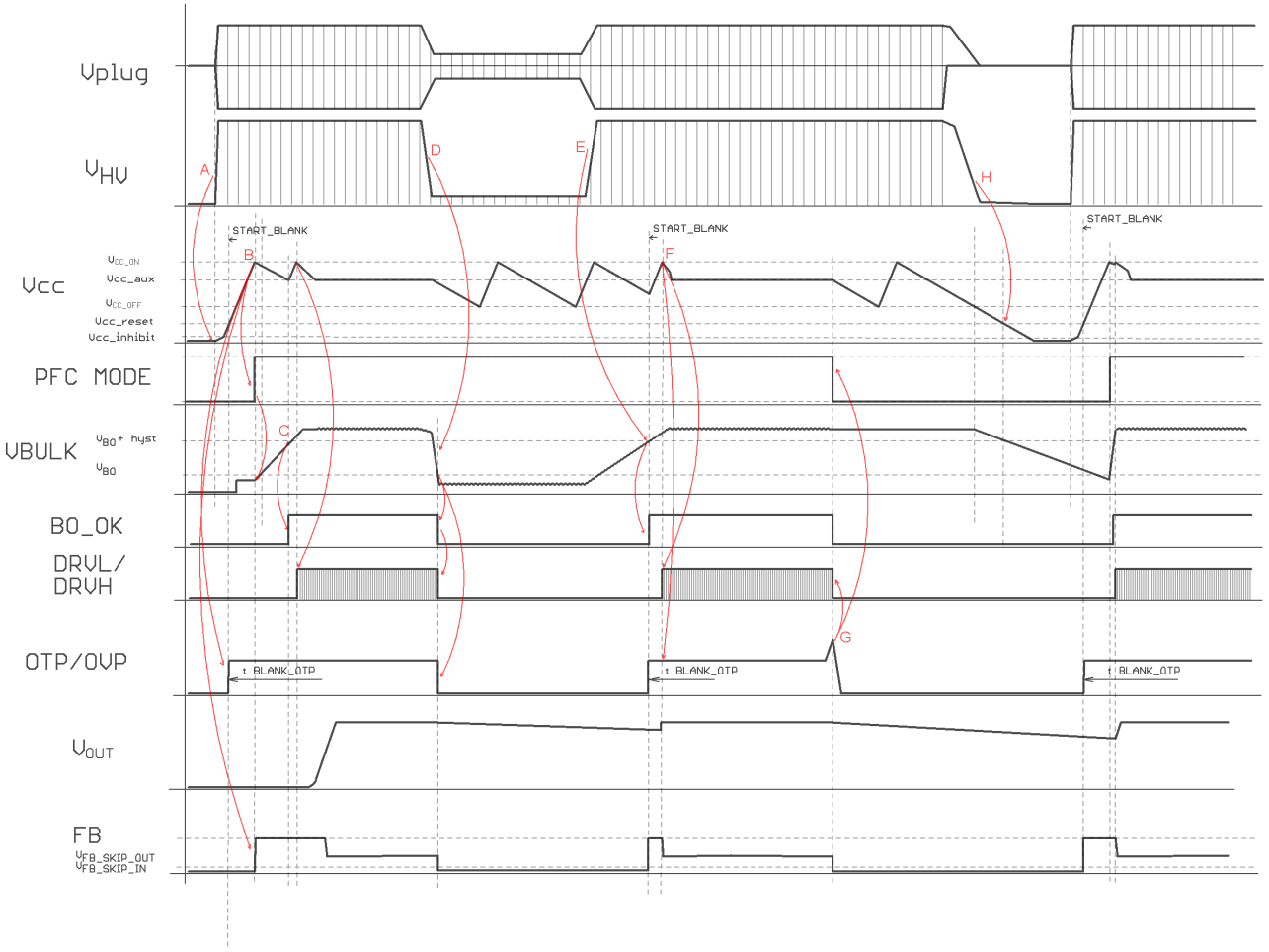



**Figure 85. Application Start, Brown−out Off and Restart, OVP/OTP Latch and then Restart**

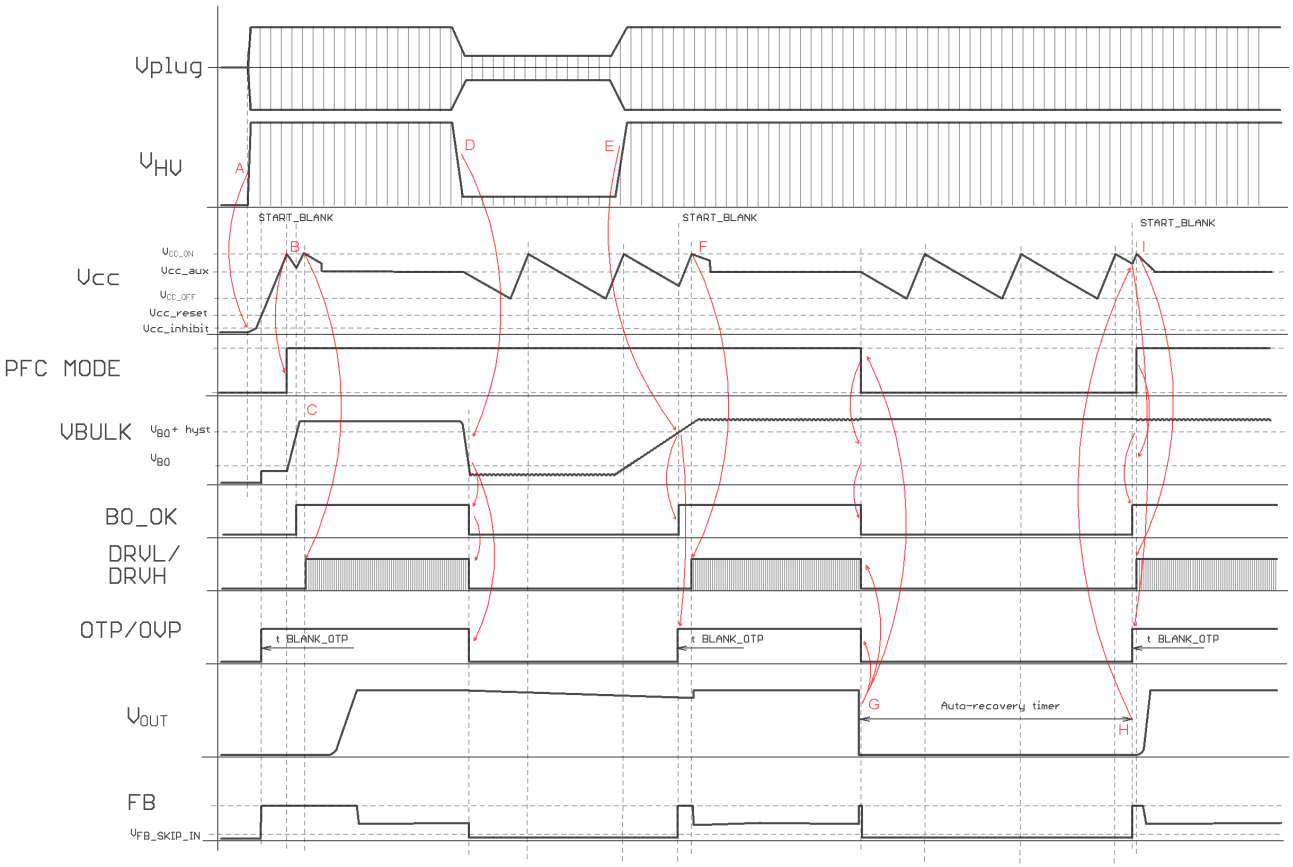



**Figure 86. Application Start, Brown−out Off and Restart, Output Short Fault with Auto−recovery Restart**

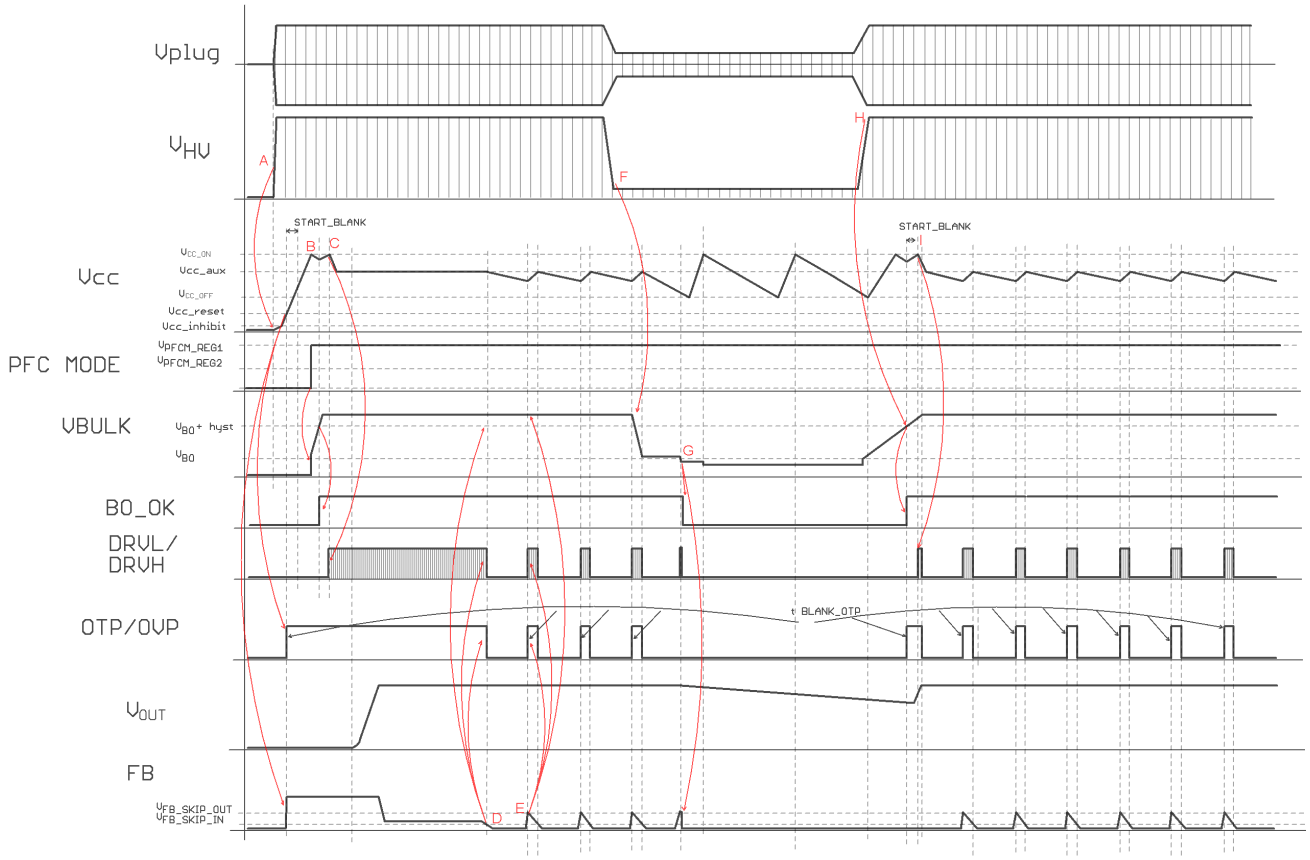



**Figure 87. Startup, Skip−mode Operation, Low Line Detection and Restart into Skip**

## ORDERING INFORMATION

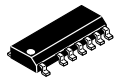
| Device | Package Marking | Package Type | Shipping† |
|---|---|---|---|
| NCL30159AADR2G | NCL30159AA | SOIC−16 NB MISSING PINS 2 AND 13 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

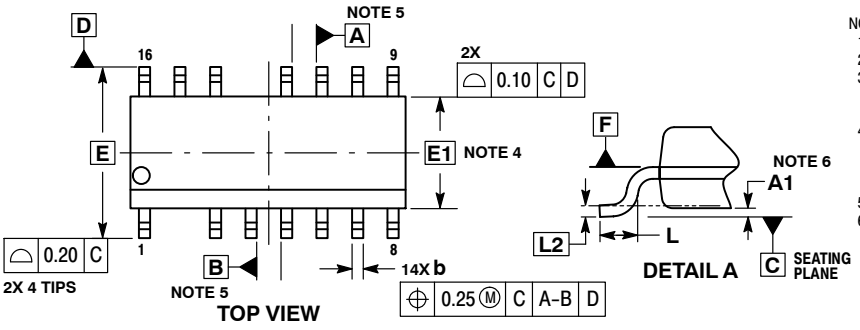
## SOIC−16 NB MISSING PINS 2 AND 13

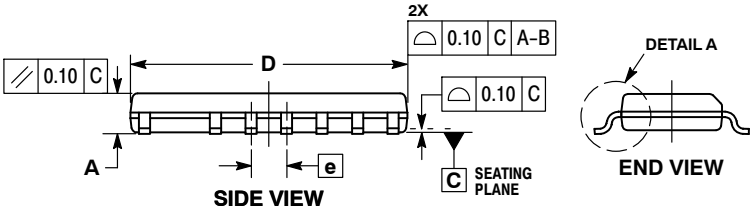
CASE 751DU
ISSUE O

DATE 18 OCT 2013



SCALE 1:1

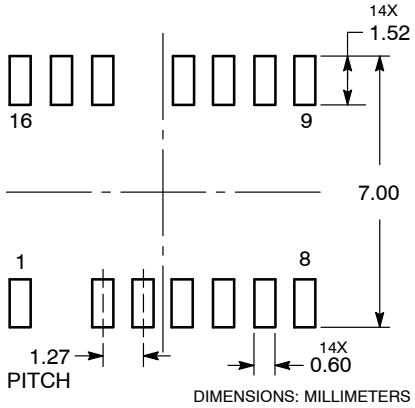



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

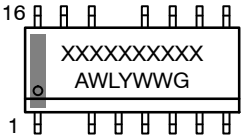
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.17 | 0.25 |
| D | 9.80 | 10.00 |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| L2 | 0.203 BSC | |

### RECOMMENDED SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

| | | |
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