1.8 V/3 V SIMカード電源および レベル・シフタ

NCN4555は、SIMカードと外部マイクロコントローラまたは MPU間で電圧を変換するように設計されたレベル・シフタ・アナログ回路です。内蔵LDO型DC-DCコンバータにより、NCN4555は1.8 Vおよび3.0 VのSIMカードのドライブに使用できます。このデバイスはISO7816-3スマート・カード・インタフェース規格、GSM 11.11および関連規格(11.12および11.18)、3Gモバイル要件(IMT-2000/3G UICC規格)に準拠しています。 \overline{STOP} ピンを使用して、低電流シャットダウン・モードを起動して、バッテリ寿命を延ばすことができます。カードの電源電圧(SIM_ V_{CC})は、1本のピン(MOD_ V_{CC})を使用して選択されます。

特長

- 1.8 Vまたは3.0 V動作のSIMカードをサポート
- LDOは1.8 Vおよび3.0 Vで50 mAを超える電流を供給可能
- 両方向のI/Oピンに対する内蔵プルアップ抵抗
- SIMピンでの7kVを超えるESD保護(人体モデル)を規定した ISO-7816仕様に準拠し、すべてのピンを完全にESD保護
- 最大5MHz超のクロックをサポート
- 低プロフィール3x3 QFN-16パッケージ
- 鉛フリー・デバイス*

代表的アプリケーション

- 2G、2.5G、および3G携帯電話用SIMカード・インタフェース 回路
- 識別モジュール
- スマート・カード・リーダ
- ワイヤレスPCカード

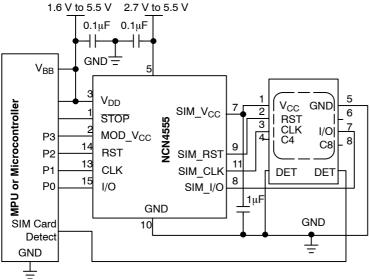


Figure 1. Typical Interface Application

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

1



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MARKING DIAGRAM

QFN-16 MN SUFFIX CASE 488AK



A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NCN4555MNG	QFN-16 (Pb-Free)	123 Units / Rail
NCN4555MNR2G	QFN-16 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

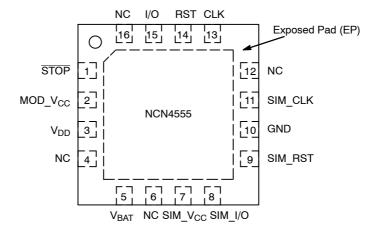


Figure 2. QFN-16 Pinout (Top View)

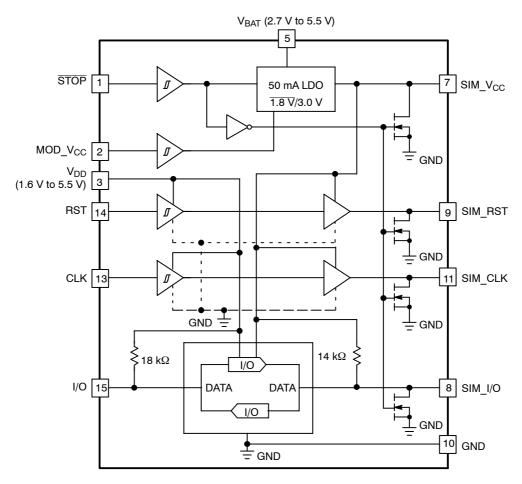


Figure 3. NCN4555 Block Diagram

PIN DESCRIPTIONS

PIN	Name	Туре	Description
1	STOP	INPUT	Power Down Mode pin: STOP = Low → Low current shutdown mode activated STOP = High → Normal Operation A Low level on this pin resets the SIM interface, switching off the SIM_V _{CC} .
2	MOD_V _{CC}	INPUT	The signal present on this pin programs the SIM_V _{CC} value: $ \begin{array}{l} \text{MOD_V}_{CC} = \text{Low} \rightarrow \text{SIM_V}_{CC} = 1.8 \text{ V} \\ \text{MOD_V}_{CC} = \text{High} \rightarrow \text{SIM_V}_{CC} = 3 \text{ V} \\ \end{array} $
3	V _{DD}	POWER	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the microprocessor. A 0.1 μ F capacitor shall be used to bypass the power supply voltage. When V _{DD} is below 1.1 V typical the SIM_V _{CC} is disabled. The NCN4555 comes into a shutdown mode.
4	NC		No Connect
5	V_{BAT}	POWER	DC–DC converter supply input. The input voltage ranges from 2.7V up to 5.5V. This pin has to be bypass by a 0.1 μ F capacitor.
6	NC		No Connect
7	SIM_V _{CC}	POWER	This pin is connected to the SIM card power supply pin. An internal LDO converter is programmable by the external MPU to supply either 1.8 V or 3.0 V output voltage. An external 1.0 μ F minimum ceramic capacitor recommended must be connected across SIM_V _{CC} and GND. During a normal operation, the SIM_V _{CC} voltage can be set to 1.8 V followed by a 3.0 V value, or can start directly to any of these two values.
8	SIM_I/O	INPUT/ OUTPUT	This pin handles the connection to the serial I/O of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the micro controller. A 14 k Ω (typical) pullup resistor provides a High impedance state for the SIM card I/O link.
9	SIM_RST	OUTPUT	This pin is connected to the RESET pin of the card connector. A level translator adapts the external Reset (RST) signal to the SIM card.
10	GND	GROUND	This pin is the GROUND reference for the integrated circuit and associated signals. Care must be taken to avoid voltage spikes when the device operates in a normal operation.
11	SIM_CLK	OUTPUT	This pin is connected to the CLOCK pin of the card connector. The CLOCK (CLK) signal comes from the external clock generator, the internal level shifter being used to adapt the voltage defined for the SIM $_{\rm VCC}$.
12	NC		No Connect
13	CLK	INPUT	The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max values defined by the specification (typically 50%). The built–in level shifter translates the input signal to the external SIM card CLK input.
14	RST	INPUT	The RESET signal present at this pin is connected to the SIM card through the internal level shifter which translates the level according to the SIM_V _{CC} programmed value.
15	I/O	INPUT/ OUTPUT	This pin is connected to an external microcontroller or cellular phone management unit. A bidirectional level translator adapts the serial I/O signal between the smart card and the external controller. A built–in constant 18 k Ω (typical) resistor provides a high impedance state when not activated.
16	NC		No Connect

ATTRIBUTES

Characteristics	Values	
ESD protection HBM, SIM card pins (7, 8, 9, 10 & 11) (Note 1) HBM, All other pins (Note 1) MM, SIM card pins (7, 8, 9, 10 & 11) (Note 2) MM, All other pins (Note 2) CDM, SIM card pins (7, 8, 9, 10 & 11) (Note 3) CDM, All other pins (Note 3)	> 7 kV > 2 kV > 600 V > 200 V > 2 kV > 600 V	
Moisture sensitivity (Note 4) QFN-16	Level 1	
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

- 1. Human Body Model, R = 1500 Ω , C = 100 pF. 2. Machine Model.

- CDM, Charged Device Model.
 For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 5)

Rating	Symbol	Value	Unit
LDO Power Supply Voltage	V_{BAT}	-0.5 ≤ V _{BAT} ≤ 6	V
Power Supply from Microcontroller Side	V _{DD}	$-0.5 \le V_{DD} \le 6$	V
External Card Power Supply	SIM_V _{CC}	$-0.5 \le SIM_{VCC} \le 6$	V
Digital Input Pins	V _{in}	$-0.5 \le V_{in} \le V_{DD} + 0.5$ but < 6.0 ±5	V mA
Digital Output Pins	V _{out}	$-0.5 \le V_{out} \le V_{DD} + 0.5$ but < 6.0 ±10	V mA
SIM card Output Pins	V _{out}	$-0.5 \le V_{out} \le SIM_{VCC} + 0.5$ but $< 6.\overline{0}$ 15 (internally limited)	V mA
QFN-16 Low Profile package Power Dissipation @ T _A = + 85°C Thermal Resistance Junction-to-Air	P _D R _{θJA}	440 90	mW °C/W
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature Range	TJ	-40 to +125	°C
Maximum Junction Temperature	T _{Jmax}	+125	°C
Storage Temperature Range	T _{stg}	-65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at $T_A = +25$ °C

POWER SUPPLY SECTION (-40°C to +85°C)

Pin	Symbol	Rating	Min	Тур	Max	Unit
5	V _{BAT}	Power Supply	2.7		5.5	V
5	I _{VBAT}	Operating current – I _{CC} = 0 mA (Note 6)		22	30	μΑ
5	I _{VBAT_SD}	Shutdown current – STOP= Low (Note 7)			3.0	μΑ
3	V_{DD}	Operating Voltage	1.6		5.5	V
3	I _{VDD}	Operating Current – f _{CLK} = 1 MHz (Note 8)		7.0	12	μΑ
3	I _{VDD_SD}	Shutdown Current – STOP = Low			1.0	μΑ
3	V_{DD}	Undervoltage Lockout	0.6		1.5	V
7	SIM_V _{CC}	$\begin{array}{l} \text{MOD_V}_{CC} = \text{High, V}_{BAT} = 3.0 \text{ V, I}_{SIM_VCC} = 50 \text{ mA} \\ \text{MOD_V}_{CC} = \text{High, V}_{BAT} = 3.3 \text{ V to } 5.5 \text{ V, I}_{SIM_VCC} = 0 \text{ mA to } 50 \text{ mA} \\ \text{MOD_V}_{CC} = \text{Low, V}_{BAT} = 2.7 \text{ V to } 5.5 \text{ V, I}_{SIM_VCC} = 0 \text{ mA to } 50 \text{ mA} \\ \end{array}$	2.8 1.7	2.8 3.0 1.8	3.2 1.9	V V V
7	I _{SIM_VCC_SC}	Short –Circuit Current – SIM_V _{CC} shorted to ground , T _A =25°C			175	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 6. As long as $V_{BAT} V_{DD} \le 2.5$ V. For $V_{BAT} V_{DD} > 2.5$ V the maximum value increases up to 35 μ A (typical being in the +25 μ A range). 7. As long as $V_{BAT} V_{DD} \le 2.5$ V.
- 8. Guaranteed by design over the operating temperature range specified.

DIGITAL INPUT/OUTPUT SECTION CLOCK, RESET, I/O, STOP, MOD_VCC

Pin	Symbol	Rating	Min	Тур	Max	Unit
1,2, 13, 14, 15	V _{in}	V _{in} Input Voltage Range (STOP, MOD_V _{CC} , RST, CLK, I/O)			V _{DD}	V
11,10	I _{IH} & I _{IL}	Input Current (STOP, MOD_V _{CC} , RST, CLK)	-100		100	nA
13, 14	V _{IH} V _{IL}	High Level Input Voltage (RST, CLK) Low Level Input Voltage (RST, CLK)	0.7 * V _{DD} (Note 9)		V _{DD} 0.4	V V
1, 2	V _{IH}	High Level Input Voltage (STOP, MOD_V _{CC})	0.7 * V _{DD} (Note 9)		V_{DD}	V
	V _{IL}	Low Level Input Voltage (STOP, MOD_V _{CC})	0		0.4	V
15	V _{OH_I/O} V _{OL_I/O} I _{IH} I _{IL}	High Level Output Voltage (SIM_I/O = SIM_V _{CC} , I _{OH_I/O} = -20 μA) Low Level Output Voltage (SIM_I/O = 0 V, I _{OH_I/O} = 200 μA) High Level Input Current (I/O) Low Level Input Current (I/O)	0.7 * V _{DD} 0 -20		V _{DD} 0.4 20 1.0	V V μA mA
15	R _{pu_I/O}	I/0 Pullup Resistor	12	18	24	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. If 1.6 V \leq V_{DD} \leq 1.8 V then V_{IHmin} = 1.26 V.

SIM INTERFACE SECTION (Note 10)

Pin	Symbol	Rating	Min	Тур	Max	Unit
9	SIM_RST	SIM_V _{CC} = +3.0 V (MOD_V _{CC} = High) Output RESET V _{OH} @ I_{sim_rst} = -20 μ A Output RESET V _{OL} @ I_{sim_rst} = +200 μ A Output RESET Rise Time @ Cout = 30 pF Output RESET Fall Time @ Cout = 30 pF SIM_V _{CC} = +1.8 V (MOD_V _{CC} = Low) Output RESET V _{OH} @ I_{sim_rst} = -20 μ A Output RESET V _{OL} @ I_{sim_rst} = +200 μ A Output RESET Rise Time @ Cout = 30 pF	0.9 * SIM_V _{CC} 0		SIM_V _{CC} 0.4 1 1 1 SIM_V _{CC} 0.4 1	V γ μs μs V V
		Output RESET Fall Time @ Cout = 30 pF			ı	μs
11	SIM_CLK	$\begin{split} &\text{SIM_V}_{CC} = +3.0 \text{ V (MOD_V}_{CC} = \text{High)} \\ &\text{Output Duty Cycle} \\ &\text{Max Output Frequency} \\ &\text{Output V}_{OH} @ I_{\text{sim_clk}} = -20 \ \mu\text{A} \\ &\text{Output V}_{OL} @ I_{\text{sim_clk}} = +200 \ \mu\text{A} \\ &\text{Output SIM_CLK Rise Time @ Cout} = 30 \ \text{pF} \\ &\text{Output SIM_CLK Fall Time @ Cout} = 30 \ \text{pF} \\ \end{aligned}$	40 5 0.9 * SIM_V _{CC} 0		60 SIM_V _{CC} 0.4 18 18	% MHz V V ns
		SIM_V _{CC} = +1.8 V (MOD_V _{CC} = Low) Output Duty Cycle Max Output Frequency Output V _{OH} @ I_{sim_clk} = -20 μ A Output V _{OL} @ I_{sim_clk} = +200 μ A Output SIM_CLK Rise Time @ Cout = 30 pF Output SIM_CLK Fall Time @ Cout = 30 pF	40 5 0.9 * SIM_V _{CC} 0		60 SIM_V _{CC} 0.4 18 18	% MHz V V ns
8	SIM_I/O	$\begin{split} &\text{SIM_V}_{CC} = +3.0 \text{ V (MOD_V}_{CC} = \text{High)} \\ &\text{Output V}_{OH} \textcircled{Q} \text{ I}_{\text{SIM_IO}} = -20 \text{ μA, V$}_{I/O} = \text{V}_{DD} \\ &\text{Output V}_{OL} \textcircled{Q} \text{ I}_{\text{SIM_IO}} = +1 \text{ mA, V$}_{I/O} = 0 \text{ V} \\ &\text{SIM_I/O Rise Time} \textcircled{Q} \text{ C}_{out} = 30 \text{ pF} \\ &\text{SIM_I/O Fall Time} \textcircled{Q} \text{ C}_{out} = 30 \text{ pF} \end{split}$	0.8 * SIM_V _{CC}		SIM_V _{CC} 0.4 1 1	ν γ μs μs
		$\begin{split} &\text{SIM_V_{CC}} = +1.8 \text{ V (MOD_V_{CC}} = \text{High)} \\ &\text{Output V}_{OH} \textcircled{0} \text{ I}_{\text{SIM_IO}} = -20 \mu\text{A, V}_{\text{I/O}} = \text{V}_{DD} \\ &\text{Output V}_{OL} \textcircled{0} \text{ I}_{\text{SIM_IO}} = +1.0 \text{ mA, V}_{\text{I/O}} = 0 \text{ V} \\ &\text{SIM_I/O Rise Time} \textcircled{0} \text{ C}_{\text{out}} = 30 \text{ pF} \\ &\text{SIM_I/O Fall Time} \textcircled{0} \text{ C}_{\text{out}} = 30 \text{ pF} \end{split}$	0.8 * SIM_V _{CC} 0		SIM_V _{CC} 0.3 1 1	V γ μs μs
8	R _{pu_SIM_I/O}	Card I/O Pullup Resistor	10	14	18	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

^{10.} All the dynamic specifications (AC specifications) are guaranteed by design over the operating temperature range.

TYPICAL CHARACTERISTICS

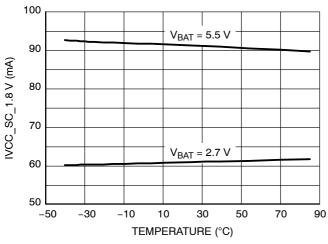


Figure 4. Short Circuit Current IV $_{CC}$ SC vs Temperature at SIM $_{VCC}$ = 1.8 V (MOD $_{VCC}$ = LOW)

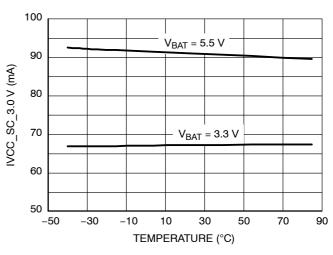


Figure 5. Short Circuit Current IV $_{CC}$ SC vs Temperature at SIM $_{CC}$ = 3.0 V (MOD $_{CC}$ = HIGH)

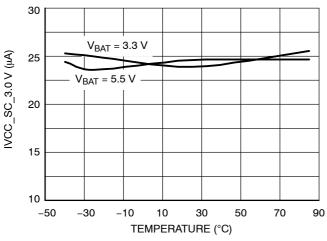


Figure 6. I_{BAT} vs temperature at 3.0 V

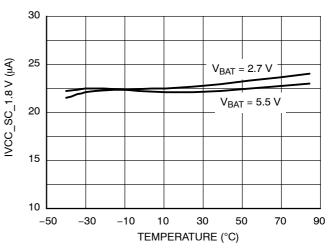


Figure 7. IV_{BAT} vs Temperature at 1.8 V

アプリケーション情報

カード電源コンバータ

NCN4555インタフェースDC-DCコンバータは、 1.8 Vまたは3.0 Vで50 mAを超える電流を供給できる 低ドロップアウト電圧レギュレータです。このデバ イスは、標準25µA未満の超低静止電流を特長として います (Figure 6および7)。MOD V_{CC}は、1.8 V $(MOD_V_{CC} = ロー)$ または3.0 $V(MOD_V_{CC} = ハイ)$ の安 定化電圧を選択するロジック・レベル信号を受け入 れる選択入力です。また、NCN4555にはレギュレー タ出力のターン・オフまたはターン・オンを可能に するシャットダウン入力があります。シャットダウ ン・モードでの消費電力は一般に数10 nA程度です (30 nA標準)。Figure 8に、NCN4555電圧レギュレー タの簡略図を示します。SIM V_{CC}出力は内部で電流 制限され、短絡から保護されています。短絡電流 IV_{CC}は、温度によって変化せずSIM_V_{CC}です。この 電流は V_{BAT} によって通常60~90 mAの範囲で変化し ます (Figure 4および5)。

安定した満足のいくLDO動作を保証するために、 SIM_V_{CC} 出力は $1.0~\mu F$ のバイパス・セラミック・コンデンサを介してグランドに接続されます。この入力で、 V_{BAT} は $0.1~\mu F$ のセラミック・コンデンサでグランドにバイパスされます。

レベル・シフタ

レベル・シフタは、マイクロコントローラとスマート・カード間に存在する可能性のある電圧差に対応します。RESETおよびCLOCKレベル・シフタは単方向で、両方とも同じ構成を備えています。

双方向I/Oラインは、MCUとSIMカード間の電圧差を両方向で自動的に適合させる方法を提供します。 プルアップ抵抗に加えて、アクティブなプルアップ 回路(Figure 8、Q1およびQ2)が浮遊容量の高速充 電を提供し、立ち上がり時間が完全にISO7816仕様 の範囲内になります。

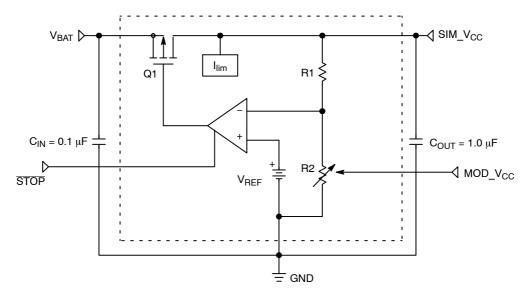


Figure 8. Simplified Block Diagram of the LDO Voltage Regulator

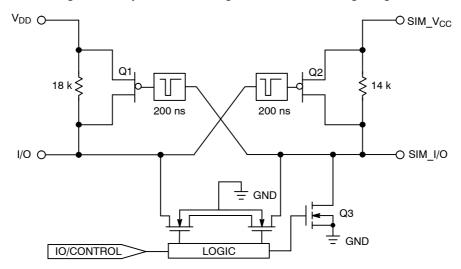


Figure 9. Basic I/O Line Interface

Figure 10に示す標準的な波形は、アクセラレータの動作を示しています。最初の200 ns(標準)の間、立ち上がり時間の傾きは浮遊容量に関連するプルアップ抵抗にのみ関係します。この期間中、PMOSデバイスは入力電圧が V_{gs} スレッショルド未満なのでアクティブになりません。Figure 10に示すとおり、入力の傾きが V_{gsth} と交差すると、反対側のワンショットがアクティブになり、低インピーダンスを提供してコンデンサを充電して、立ち上がり時間を長くします。ラインの反対側にも同じメカニズムが適用され、システムの最適化が図られます。

入力シュミット・トリガ

すべてのロジック入力ピン(I/OおよびSIM_I/Oを除く、Figure 3参照)に、シュミット・トリガ回路が内蔵され、NCN4555動作が無制御状態になるのを防止します。関連ピンの標準ダイナミック特性をFigure 11に記載します。

出力信号は、入力電圧が $0.7 \times V_{DD}$ を超えると確実にハイに、また出力が $0.4 \times V_{A}$ 満になると確実にローになることが保証されます。

シャットダウン動作

アプリケーションに必要な電力の節減やその他の目的のために、ピン \overline{STOP} をローに設定して、NCN4555をシャットダウン・モードにすることができます。他方、 V_{DD} が1.1 V(標準)より低くなると、デバイスは自動的にシャットダウン・モードに入ります。

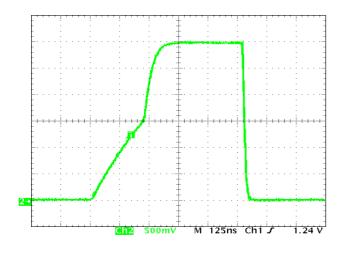


Figure 10. SIM_IO Typical Rise and Fall Times with Stray Capacitance > 30 pF (33 pF Capacitor Connected on the Board)

ESD保護回路

NCN4555 SIMインタフェースは、すべてのSIMピン(SIM_IO、SIM_CLK、SIM_RST、SIM_V_{CC}、GND)に対して7kVを超えるHBM ESD電圧保護を備えています。それ以外のすべてのピン(マイクロコントローラ側)は最小2 kVを維持します。これらの値は、回路が適切に動作するために追加された外付けコンデンサを考慮に入れないで、完全な状態のデバイスに対して保証されています。結果的に動作条件では、SIMピンで7 kVよりずっと大きな値を維持できるため、ISO7816規格(4 kV)に必要なHBM ESD電圧をはるかに超える静電気放電から完全に保護されます。

プリント基板レイアウト

モバイルまたはポータブル環境で良好かつ効率的なデバイス動作を達成し、性能を十分に活用するために、慎重なレイアウト・ルーチングが適用されます。

バイパス・コンデンサをデバイス・ピンのできるだけ近くに接続して (SIM_V_{CC}, V_{DD}) 、または (V_{BAT}) 、寄生的動作(リップルやノイズ)をできるだけ減らす必要があります。セラミック・コンデンサの使用を推奨します。

QFN-16パッケージの露出パッドをグランドと未接 続ピン(NC)に接続します。比較的大きなグランド・ プレーンを推奨します。

Figures 12および13に、評価環境におけるPCBデバイスの実装例を示します。

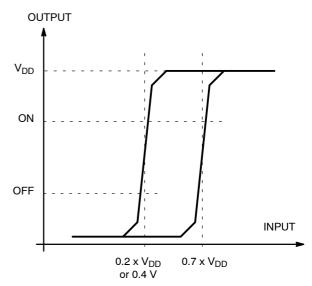


Figure 11. Typical Schmitt Trigger Characteristics

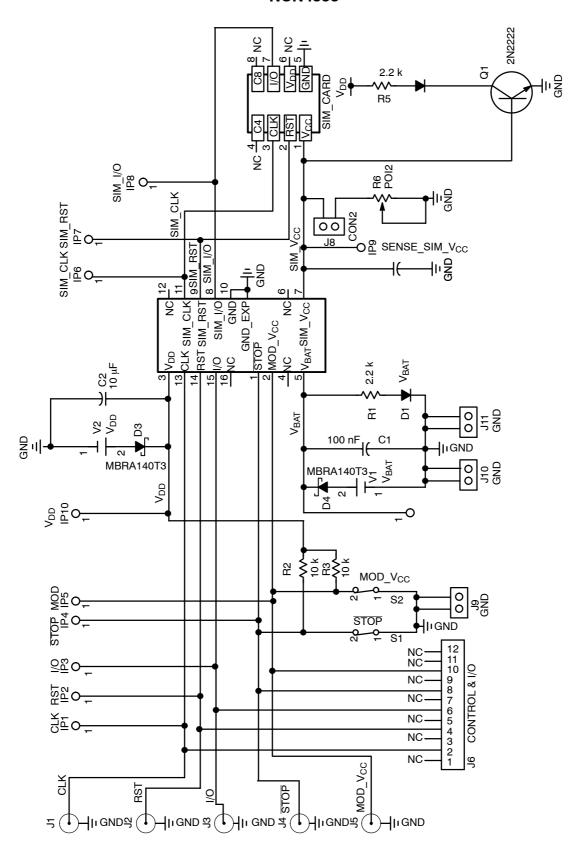
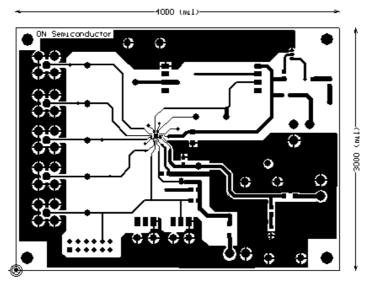


Figure 12. NCN4555 engineering test board schematic diagram



Top Layer

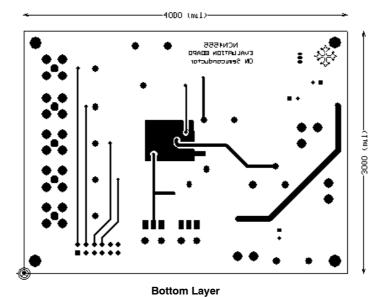


Figure 13. NCN4555 Printed Circuit Board Layout (Engineering board)



QFN16 3*3*0.75 MM, 0.5 P CASE 488AK **ISSUE O**



SCALE 2:1

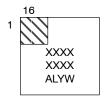
DATE 13 SEP 2004

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION 6 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 COPLANARITY APPLIES TO THE EXPOSED
- PAD AS WELL AS THE TERMINALS. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

	MILLIMETERS				
DIM	MIN MAX				
Α	0.70	0.80			
A1	0.00	0.05			
A3	0.20	REF			
b	0.18	0.30			
D	3.00	BSC			
D2	1.65	1.85			
E	3.00	BSC			
E2	1.65	1.85			
е	0.50 BSC				
K	0.20				
L	0.30 0.50				

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code

= Assembly Location Α

= Wafer Lot L Υ = Year W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

ļ	D A B
PIN 1 LOCATION _	+ E
○ 0.15 C ○ 0.15 C	TOP VIEW
// 0.10 C	(A3) -
16 X 0.08 C	SIDE VIEW A1 C
16X L NOTE 5 4	D2 5 8 EXPOSED PAD 9 —————————————————————————————————
16X b	16 13
0.10 C A B 0.05 C NOTE 3	BOTTOM VIEW

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DESCRIPTION:	QFN16, 3*3*0.75 MM, 0.5 P	QFN16, 3*3*0.75 MM, 0.5 PITCH	

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