NCP1611

Enhanced, High-Efficiency Power Factor Controller

The NCP1611 is designed to drive PFC boost stages based on an innovative ***C***urrent ***C***ontrolled ***F***requency ***F***old−back (***CCFF***) method. In this mode, the circuit classically operates in ***Cr***itical conduction ***M***ode (***CrM***) when the inductor current exceeds a programmable value. When the current is below this preset level, the NCP1611 linearly decays the frequency down to about 20 kHz when the current is null. ***CCFF*** maximizes the efficiency at both nominal and light load. In particular, the stand−by losses are reduced to a minimum.

Like in ***FCCrM*** controllers, internal circuitry allows near−unity power factor even when the switching frequency is reduced. Housed in a SO−8 package, the circuit also incorporates the features necessary for robust and compact PFC stages, with few external components.

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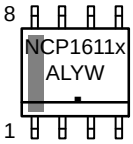
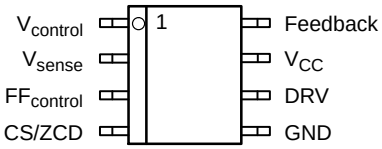
MARKING DIAGRAM

SOIC−8
CASE 751
SUFFIX D



NCP1611x = Specific Device Code
x = A or B
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 28 of this data sheet.

Features

- Near−Unity Power Factor
- Critical Conduction Mode (CrM)
- Current Controlled Frequency Fold−back (CCFF): Low Frequency Operation is Forced at Low Current Levels
- On−time Modulation to Maintain a Proper Current Shaping in CCFF Mode
- Skip Mode Near the Line Zero Crossing
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer)
- Valley Turn on
- High Drive Capability: −500 mA / +800 mA
- V_{CC} Range: from 9.5 V to 35 V
- Low Start−up Consumption
- A Version: Low V_{CC} Start−up Level (10.5 V), B Version: High V_{CC} Start−up level (17.0 V)
- Line Range Detection
- Configurable for Low Harmonic Content across Wide Line/Load Range
- EN61000−3−2 Class C Compliant across Wide Load Range for Dimmable Light Ballasts
- This is a Pb−Free Device

Safety Features

- Non−latching, Over−Voltage Protection
- Brown−Out Detection
- Soft−Start for Smooth Start−up Operation (A version)
- Over Current Limitation
- Disable Protection if the Feedback Pin is Not Connected
- Thermal Shutdown
- Low Duty−Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring
- Saturated Inductor Protection
- Detailed Safety Testing Analysis (Refer to Application Note AND9064/D)

Typical Applications

- PC, TV, Adapters Power Supplies
- LED Drivers and Light Ballasts (including dimmable versions)
- All Off−Line Applications Requiring Power Factor Correction

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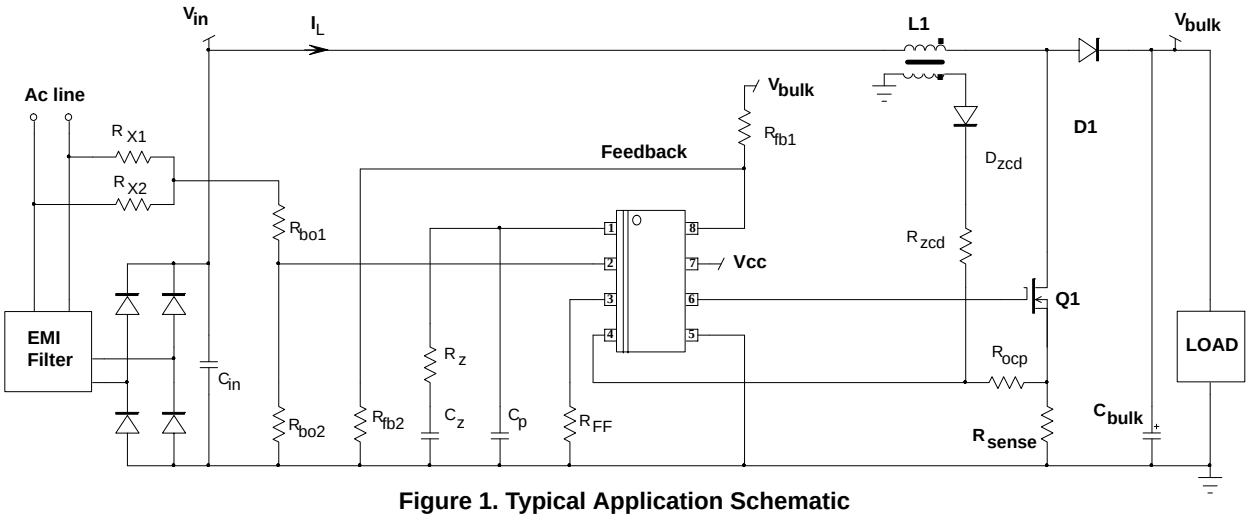


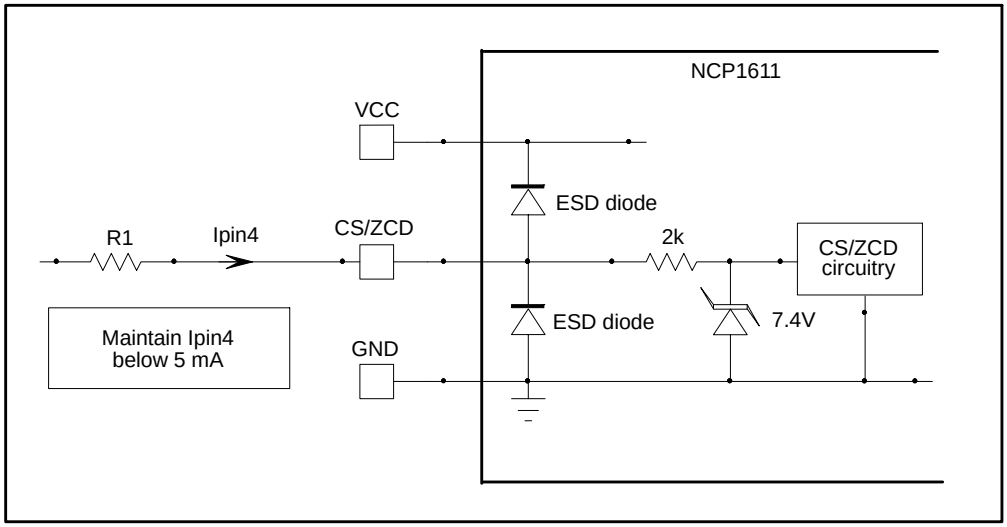
Figure 1. Typical Application Schematic

MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
V_{CC}	7	Power Supply Input	−0.3, + 35	V
$V_{CONTROL}$	1	$V_{CONTROL}$ pin (Note 1)	−0.3, $V_{CONTROL}$MAX (*)	V
V_{sense}	2	V_{sense} pin (Note 5)	−0.3, +10	V
FFcontrol	3	FFcontrol pin	−0.3, +10	V
CS/ZCD	4	Input Voltage Current Injected to pin 4 (Note 4)	−0.3, +35 +5	V mA
DRV	6	Driver Voltage (Note 1) Driver Current	−0.3, V_{DRV} (*) −500, +800	V mA
FB	8	Feedback pin	−0.3, +10	V
P_D $R_{\theta JA}$		Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	550 145	mW °C/W
T_J		Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}		Maximum Junction Temperature	150	°C
T_{Smax}		Storage Temperature Range	−65 to 150	°C
T_{Lmax}		Lead Temperature (Soldering, 10s)	300	°C
ESD_{HBM}		ESD Capability, HBM model (Note 2)	> 2000	V
ESD_{MM}		ESD Capability, Machine Model (Note 2)	> 200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. "$V_{CONTROL}$MAX" is the pin1 clamp voltage and "V_{DRV}" is the DRV clamp voltage ($V_{DRVhigh}$). If V_{CC} is below $V_{DRVhigh}$, "V_{DRV}" is V_{CC}.
2. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
4. Maximum CS/ZCD current that can be injected into pin4



5. Recommended maximum V_{sense} voltage for optimal operation is 4.5 V.

TYPICAL ELECTRICAL CHARACTERISTICS (Conditions: V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
START−UP AND SUPPLY CIRCUIT					
$V_{CC(on)}$	Start−Up Threshold, V_{CC} increasing: A version B version	 9.75 15.80	 10.50 17.00	 11.25 18.20	V
$V_{CC(off)}$	Minimum Operating Voltage, V_{CC} falling	8.50	9.00	9.50	V
$V_{CC(HYST)}$	Hysteresis ($V_{CC(on)} - V_{CC(off)}$) A version B version	 0.75 6.00	 1.50 8.00	 − −	V
$I_{CC(start)}$	Start−Up Current, V_{CC} = 9.4 V	−	20	50	μA
$I_{CC(op)1}$	Operating Consumption, no switching (V_{sense} pin being grounded)	−	0.5	1.0	mA
$I_{CC(op)2}$	Operating Consumption, 50 kHz switching, no load on DRV pin	−	2.0	3.0	mA
CURRENT CONTROLLED FREQUENCY FOLD−BACK					
T_{DT1}	Dead−Time, $V_{FFcontrol}$ = 2.60 V (Note 6)	−	−	0	μs
T_{DT2}	Dead−Time, $V_{FFcontrol}$ = 1.75 V	14	18	22	μs
T_{DT3}	Dead−Time, $V_{FFcontrol}$ = 1.00 V	32	38	44	μs
I_{DT1}	FFcontrol pin current, V_{sense} = 1.4 V and $V_{control}$ maximum	180	200	220	μA
I_{DT2}	FFcontrol pin current, V_{sense} = 2.8 V and $V_{control}$ maximum	110	135	160	μA
V_{SKIP-H}	FFcontrol pin Skip Level, $V_{FFcontrol}$ rising	−	0.75	0.85	V
V_{SKIP-L}	FFcontrol pin Skip Level, $V_{FFcontrol}$ falling	0.55	0.65	−	V
$V_{SKIP-HYST}$	FFcontrol pin Skip Hysteresis	50	−	−	mV
GATE DRIVE					
T_R	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	−	30	−	ns
T_F	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	−	20	−	ns
R_{OH}	Source resistance	−	10	−	Ω
R_{OL}	Sink resistance	−	7.0	−	Ω
I_{SOURCE}	Peak source current, V_{DRV} = 0 V (guaranteed by design)	−	500	−	mA
I_{SINK}	Peak sink current, V_{DRV} = 12 V (guaranteed by design)	−	800	−	mA
V_{DRVlow}	DRV pin level at V_{CC} close to $V_{CC(off)}$ with a 10 kΩ resistor to GND	8.0	−	−	V
$V_{DRVhigh}$	DRV pin level at V_{CC} = 35 V (R_L = 33 kΩ, C_L = 1 nF)	10	12	14	V
REGULATION BLOCK					
V_{REF}	Feedback Voltage Reference: from 0°C to 125°C Over the temperature range	 2.44 2.42	 2.50 2.50	 2.54 2.54	V
I_{EA}	Error Amplifier Current Capability	−	±20	−	μA
G_{EA}	Error Amplifier Gain	110	220	290	μS
$V_{CONTROL}$ $-V_{CONTROL}MAX$ $-V_{CONTROL}MIN$	$V_{control}$ Pin Voltage − @ V_{FB} = 2 V − @ V_{FB} = 3 V	 − −	 4.5 0.5	 − −	V
$V_{OUT}L$ / V_{REF}	Ratio (V_{OUT} Low Detect Threshold / V_{REF}) (guaranteed by design)	95.0	95.5	96.0	%
$H_{OUT}L$ / V_{REF}	Ratio (V_{OUT} Low Detect Hysteresis / V_{REF}) (guaranteed by design)	−	−	0.5	%
I_{BOOST}	$V_{control}$ Pin Source Current when (V_{OUT} Low Detect) is activated	180	220	250	μA
CURRENT SENSE AND ZERO CURRENT DETECTION BLOCKS					
$V_{CS(th)}$	Current Sense Voltage Reference	450	500	550	mV

6. There is actually a minimum dead−time that is the delay between the core reset detection and the DRV turning on (T_{ZD} parameter of the “Current Sense and Zero Current Detection Blocks” section).

TYPICAL ELECTRICAL CHARACTERISTICS (Conditions: V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
CURRENT SENSE AND ZERO CURRENT DETECTION BLOCKS					
$T_{LEB,OCP}$	Over−Current Protection Leading Edge Blanking Time (guaranteed by design)	100	200	350	ns
$T_{LEB,OVS}$	“Overstress” Leading Edge Blanking Time (guaranteed by design)	50	100	170	ns
T_{OCP}	Over−Current Protection Delay from $V_{CS/ZCD} > V_{CS(th)}$ to DRV low ($dV_{CS/ZCD}$ / dt = 10 V/μs)	–	40	200	ns
$V_{ZCD(th)H}$	Zero Current Detection, $V_{CS/ZCD}$ rising	675	750	825	mV
$V_{ZCD(th)L}$	Zero Current Detection, $V_{CS/ZCD}$ falling	200	250	300	mV
$V_{ZCD(hyst)}$	Hysteresis of the Zero Current Detection Comparator	375	500	–	mV
$R_{ZCD/CS}$	$V_{ZCD(th)H}$ over $V_{CS(th)}$ Ratio	1.4	1.5	1.6	–
$V_{CL(pos)}$	CS/ZCD Positive Clamp @ $I_{CS/ZCD}$ = 5 mA	–	15.6	–	V
$I_{ZCD(bias)}$	CS/ZCD Pin Bias Current, $V_{CS/ZCD}$ = 0.75 V	0.5	–	2.0	μA
$I_{ZCD(bias)}$	CS/ZCD Pin Bias Current, $V_{CS/ZCD}$ = 0.25 V	0.5	–	2.0	μA
T_{ZCD}	($V_{CS/ZCD} < V_{ZCD(th)L}$) to (DRV high)	–	60	200	ns
T_{SYNC}	Minimum ZCD Pulse Width	–	110	200	ns
T_{WDG}	Watch Dog Timer	80	200	320	μs
$T_{WDG(OS)}$	Watch Dog Timer in “OverStress” Situation	400	800	1200	μs
T_{TMO}	Time−Out Timer	20	30	50	μs
$I_{ZCD(gnd)}$	Source Current for CS/ZCD pin impedance Testing	–	250	–	μA
STATIC OVP					
D_{MIN}	Duty Cycle, V_{FB} = 3 V, $V_{control}$ Pin Open	–	–	0	%
ON−TIME CONTROL					
$T_{ON(LL)}$	Maximum On Time, V_{sense} = 1.4 V and $V_{control}$ maximum (CrM)	22	25	29	μs
$T_{ON(LL)2}$	On Time, V_{sense} = 1.4 V and $V_{control}$ = 2.5 V (CrM)	10.5	12.5	14.0	μs
$T_{ON(HL)}$	Maximum On Time, V_{sense} = 2.8 V and $V_{control}$ maximum (CrM)	7.3	8.5	9.6	μs
$T_{ON(LL)(MIN)}$	Minimum On Time, V_{sense} = 1.4 V (not tested, guaranteed by characterization)	–	–	200	ns
$T_{ON(HL)(MIN)}$	Minimum On Time, V_{sense} = 2.8 V (not tested, guaranteed by characterization)	–	–	100	ns
FEED−BACK OVER AND UNDER−VOLTAGE PROTECTIONS (OVP AND UVP)					
$R_{softOVP}$	Ratio (Soft OVP Threshold, V_{FB} rising) over V_{REF} ($V_{softOVP}/V_{REF}$) (guaranteed by design)	104	105	106	%
$R_{softOVP(HYST)}$	Ratio (Soft OVP Hysteresis) over V_{REF} (guaranteed by design)	1.5	2.0	2.5	%
$R_{fastOVP2}$	Ratio (Fast OVP Threshold, V_{FB} rising) over V_{REF} ($V_{fastOVP}/V_{REF}$) (guaranteed by design)	106	107	108	%
R_{UVP}	Ratio (UVP Threshold, V_{FB} rising) over V_{REF} (V_{UVP}/V_{REF}) (guaranteed by design)	8	12	16	%
$R_{UVP(HYST)}$	Ratio (UVP Hysteresis) over V_{REF} (guaranteed by design)	–	–	1	%
$(I_B)_{FB}$	FB Pin Bias Current @ $V_{FB} = V_{OVP}$ and $V_{FB} = V_{UVP}$	50	200	450	nA
BROWN−OUT PROTECTION AND FEED−FORWARD					
V_{BOH}	Brown−Out Threshold, V_{sense} rising	0.96	1.00	1.04	V
V_{BOL}	Brown−Out Threshold, V_{sense} falling	0.86	0.90	0.94	V
$V_{BO(HYST)}$	Brown−Out Comparator Hysteresis	60	100	–	mV
$T_{BO(blank)}$	Brown−Out Blanking Time	35	50	65	ms
$I_{CONTROL(BO)}$	$V_{control}$ Pin Sink Current, $V_{sense} < V_{BOL}$	40	50	60	μA

6. There is actually a minimum dead−time that is the delay between the core reset detection and the DRV turning on (T_{ZD} parameter of the “Current Sense and Zero Current Detection Blocks” section).

TYPICAL ELECTRICAL CHARACTERISTICS (Conditions: V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
BROWN−OUT PROTECTION AND FEED−FORWARD					
V_{HL}	Comparator Threshold for Line Range Detection, V_{sense} rising	2.1	2.2	2.3	V
V_{LL}	Comparator Threshold for Line Range Detection, V_{sense} falling	1.6	1.7	1.8	V
$V_{HL(hyst)}$	Comparator Hysteresis for Line Range Detection	400	500	600	mV
$T_{HL(blank)}$	Blanking Time for Line Range Detection	15	25	35	ms
$I_{BO(bias)}$	Brown−Out Pin Bias Current, $V_{sense} = V_{BOH}$	−250	−	250	nA
THERMAL SHUTDOWN					
T_{LIMIT}	Thermal Shutdown Threshold	−	150	−	°C
H_{TEMP}	Thermal Shutdown Hysteresis	−	50	−	°C

6. There is actually a minimum dead−time that is the delay between the core reset detection and the DRV turning on (T_{ZD} parameter of the “Current Sense and Zero Current Detection Blocks” section).

DETAILED PIN DESCRIPTION

Pin Number	Name	Function
1	$V_{CONTROL}$	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. Pin1 is grounded when the circuit is off so that when it starts operation, the power increases slowly to provide a soft−start function.
2	V_{SENSE}	A portion of the instantaneous input voltage is to be applied to pin 2 in order to detect brown−out conditions. If V_{pin2} is lower than 0.9 V for more than 50 ms, the circuit stops pulsing until the pin voltage rises again and exceeds 1.0 V. This pin also detects the line range. By default, the circuit operates the “low−line gain” mode. If V_{pin2} exceeds 2.2 V, the circuit detects a high−line condition and reduces the loop gain by 3. Conversely, if the pin voltage remains lower than 1.7 V for more than 25 ms, the low−line gain is set. Connecting the pin 2 to ground disables the part once the 50 ms blanking time has elapsed.
3	$FF_{CONTROL}$	This pin sources a current representative to the line current. Connect a resistor between pin3 and ground to generate a voltage representative of the line current. When this voltage exceeds the internal 2.5 V reference (V_{REF}), the circuit operates in critical conduction mode. If the pin voltage is below 2.5 V, a dead−time is generated that approximately equates [66 μs x (1 − (V_{pin3}/V_{REF}))]. By this means, the circuit forces a longer dead−time when the current is small and a shorter one as the current increases. The circuit skips cycles whenever V_{pin3} is below 0.65 V to prevent the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient. This does result in a slightly increased distortion of the current. If superior power factor is required, offset pin 3 by more than 0.75 V offset to inhibit the skip function.
4	CS / ZCD	This pin monitors the MOSFET current to limit its maximum current. This pin is also connected to an internal comparator for Zero Current Detection (ZCD). This comparator is designed to monitor a signal from an auxiliary winding and to detect the core reset when this voltage drops to zero. The auxiliary winding voltage is to be applied through a diode to avoid altering the current sense information for the on−time (see application schematic).
5	Ground	Connect this pin to the PFC stage ground.
6	Drive	The high−current capability of the totem pole gate drive (−0.5/+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
7	V_{CC}	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 10.5 V (A version, 17.0 V for the B version) and turns off when V_{CC} goes below 9.0 V (typical values). After start−up, the operating range is 9.5 V up to 35 V. The A version is preferred in applications where the circuit is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start−up level (11.25 V) is set low enough so that the circuit can be powered from a 12 V rail. The B version is optimized for applications where the PFC stage is self−powered.
8	Feedback	This pin receives a portion of the PFC output voltage for the regulation and the Dynamic Response Enhancer (DRE) that drastically speeds−up the loop response when the output voltage drops below 95.5% of the desired output level. V_{pin8} is also the input signal for the (non−latching) Over−Voltage (OVP) and Under−Voltage (UVP) comparators. The UVP comparator prevents operation as long as V_{pin8} is lower than 12% of the reference voltage (V_{REF}). A soft OVP comparator gradually reduces the duty−ratio when V_{pin8} exceeds 105% of V_{REF}. If despite of this, the output voltage still increases, the driver is immediately disabled if the output voltage exceeds 107% of the desired level (fast OVP). A 250 nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidentally open.

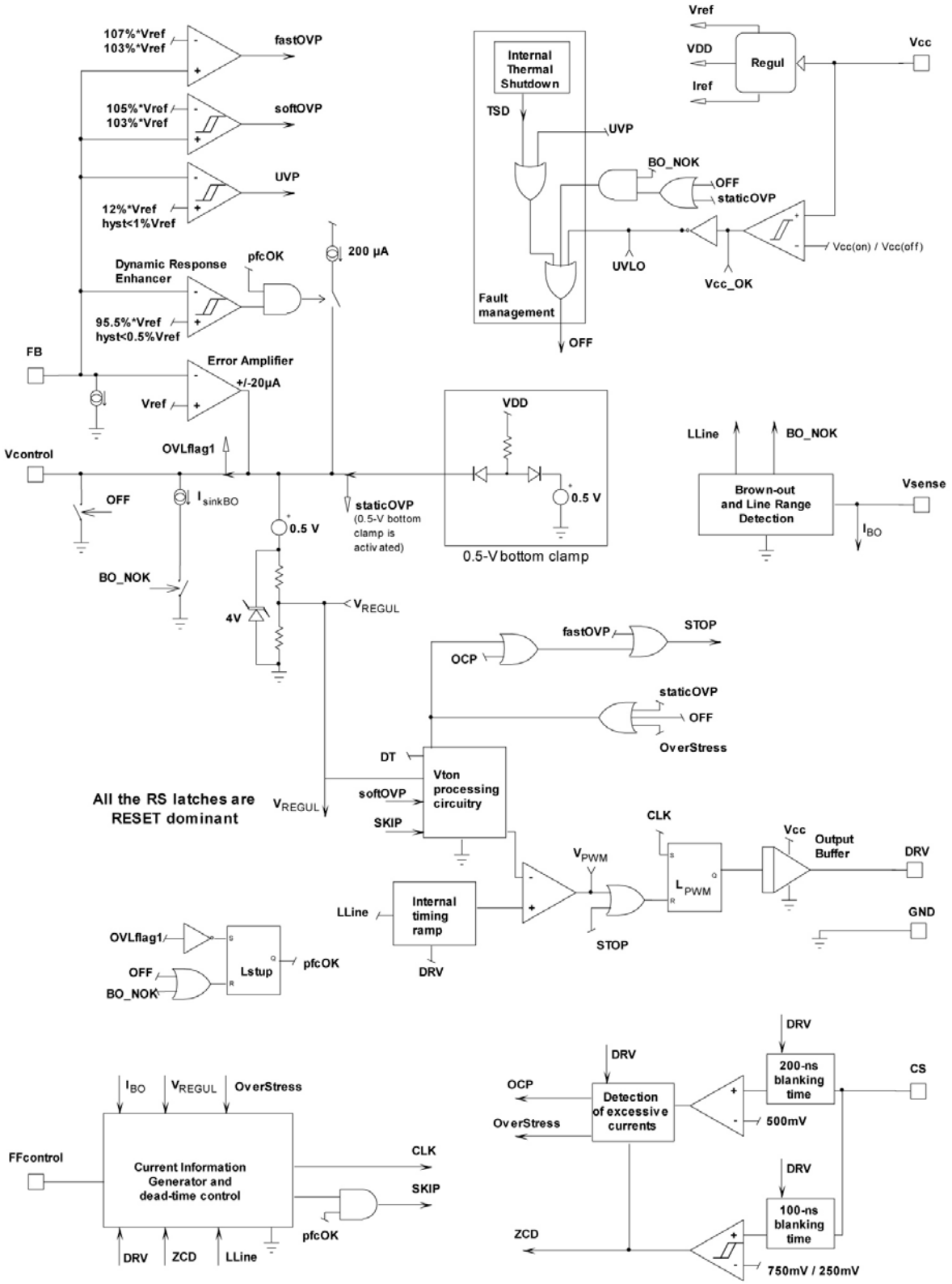


Figure 2. Block Diagram

TYPICAL CHARACTERISTICS

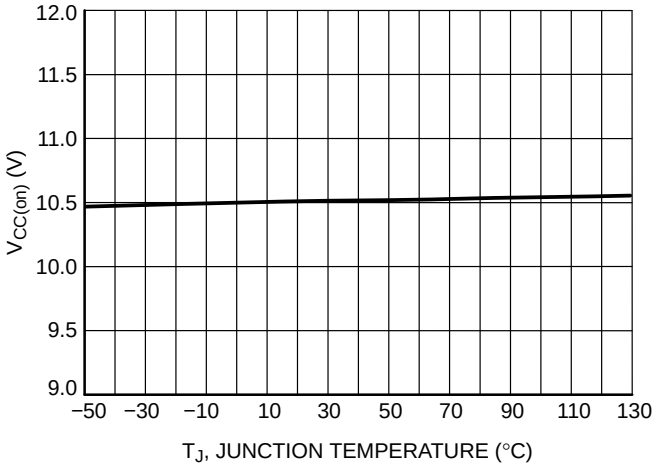


Figure 3. Start−Up Threshold, V_{CC} Increasing ($V_{CC(on)}$) vs. Temperature (A Version)

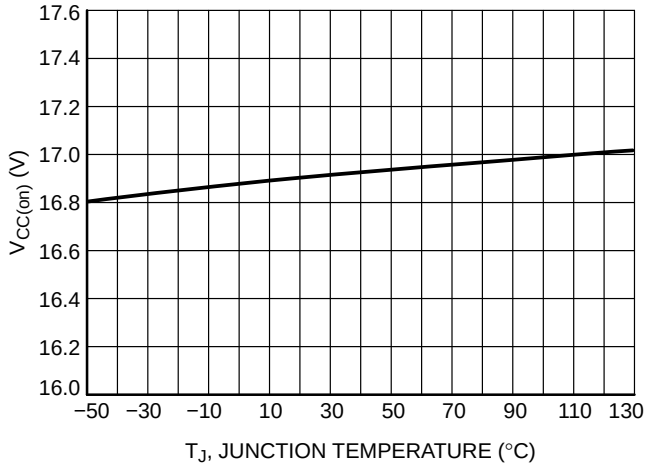


Figure 4. Start−Up Threshold, V_{CC} Increasing ($V_{CC(on)}$) vs. Temperature (B Version)

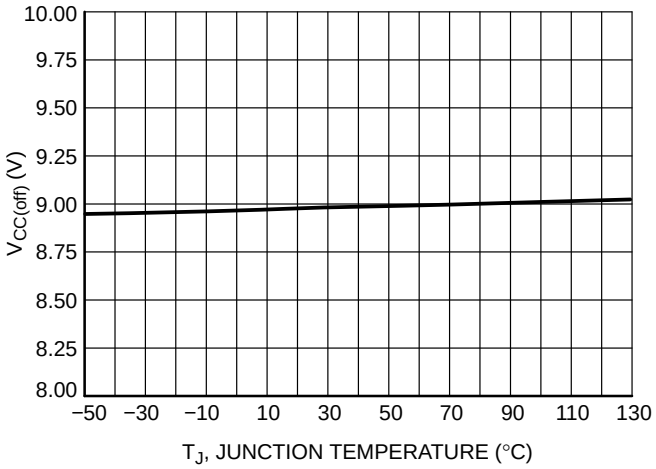


Figure 5. V_{CC} Minimum Operating Voltage, V_{CC} Falling ($V_{CC(off)}$) vs. Temperature

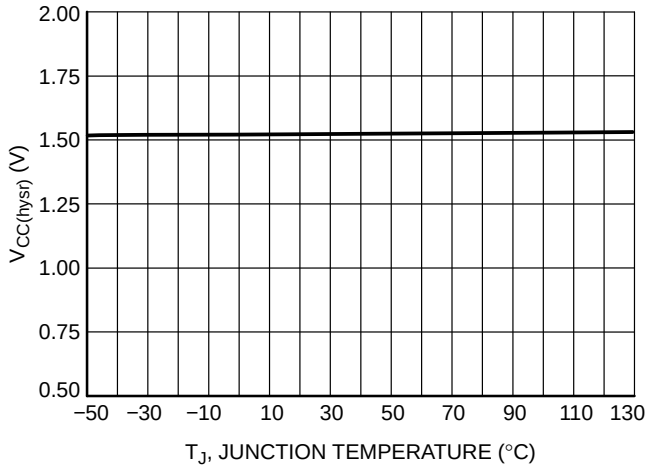


Figure 6. Hysteresis ($V_{CC(on)}$ − $V_{CC(off)}$) vs. Temperature (A Version)

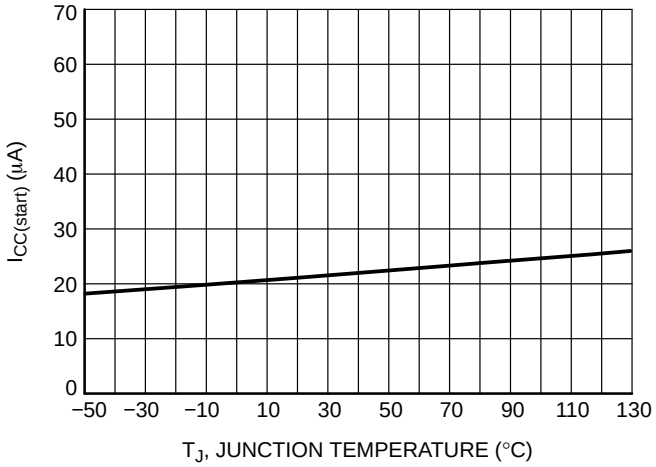


Figure 7. Start−Up Current @ V_{CC} = 9.4 V vs. Temperature

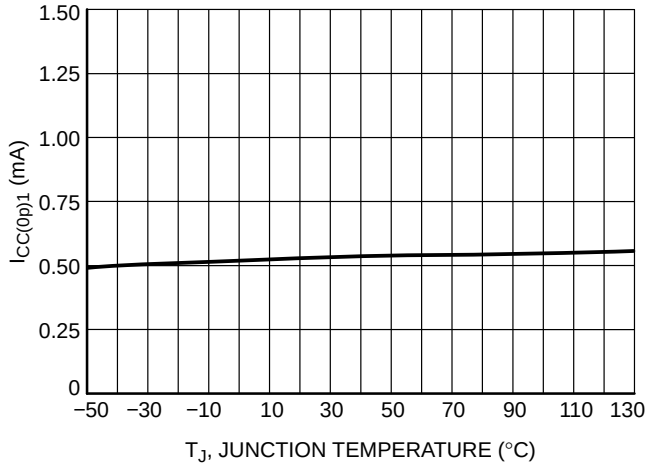


Figure 8. Operating Current, No Switching (V_{SENSE} Grounded) vs. Temperature

TYPICAL CHARACTERISTICS

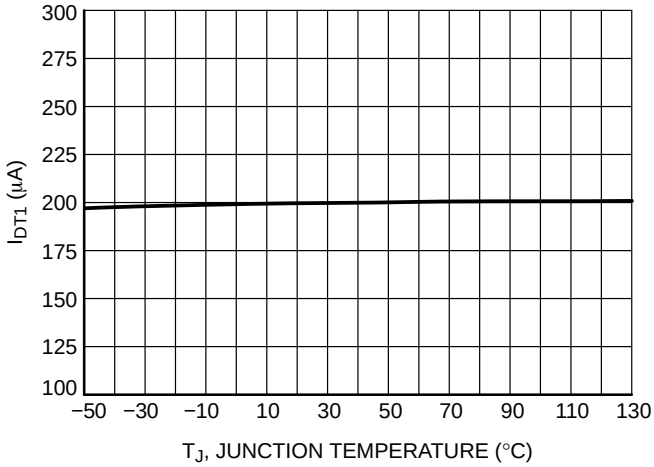


Figure 9. FFcontrol Pin Current, V_{SENSE} = 1.4 V and $V_{CONTROL}$ Maximum vs. Temperature

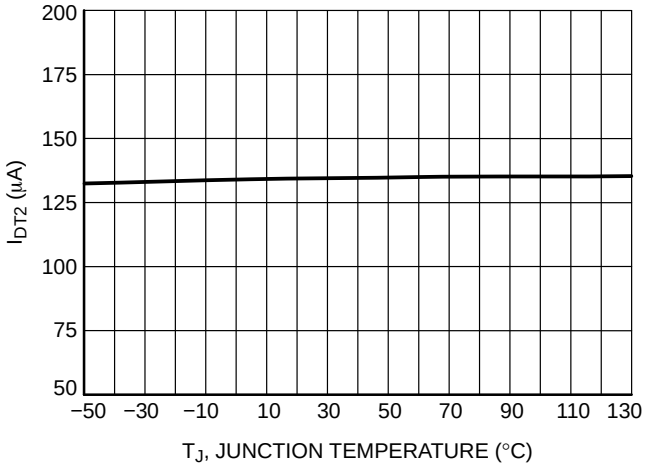


Figure 10. FFcontrol Pin Current, V_{SENSE} = 2.8 V and $V_{CONTROL}$ Maximum vs. Temperature

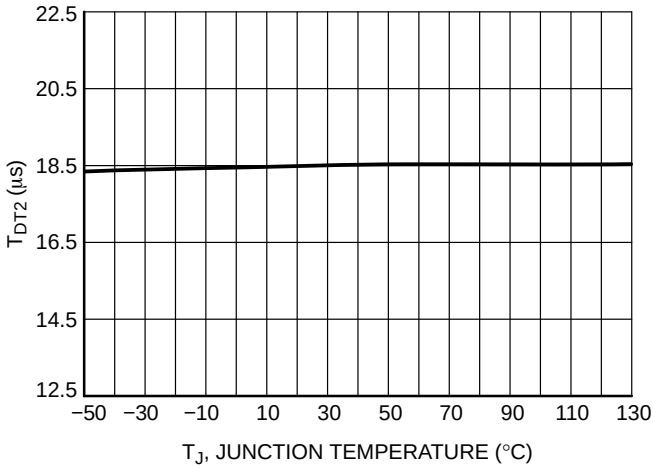


Figure 11. Dead−Time, $V_{FFcontrol}$ = 1.75 V vs. Temperature

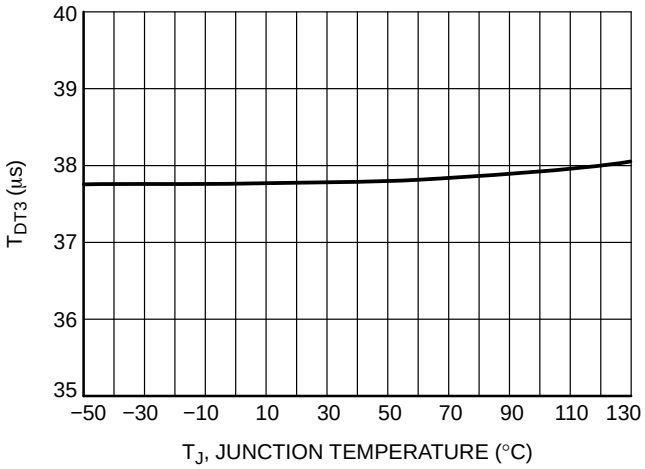


Figure 12. Dead−Time, $V_{FFcontrol}$ = 1.00 V vs. Temperature

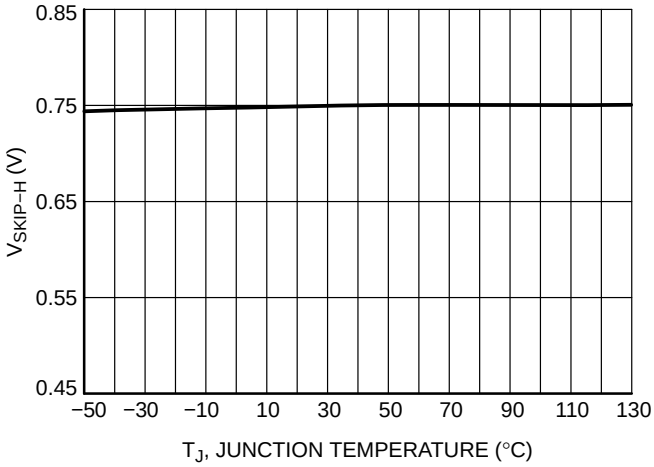


Figure 13. FFcontrol Pin Skip Level ($V_{FFcontrol}$ Rising) vs. Temperature

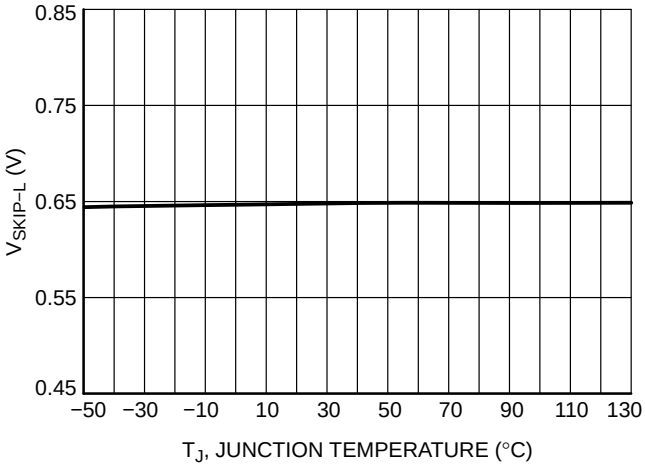


Figure 14. FFcontrol Pin Skip Level ($V_{FFcontrol}$ Falling) vs. Temperature

TYPICAL CHARACTERISTICS

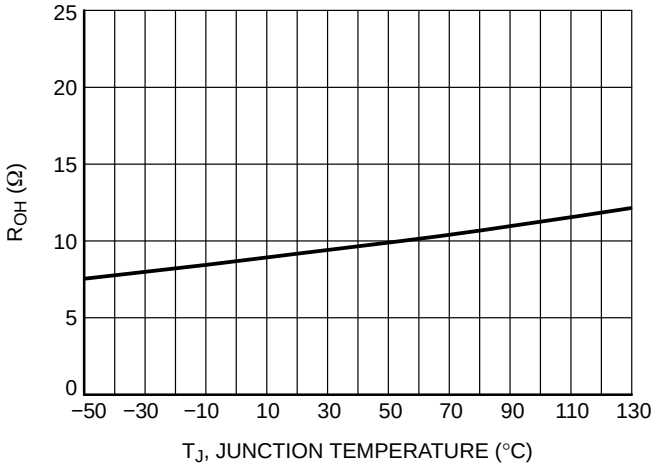


Figure 15. DRV Source Resistance vs. Temperature

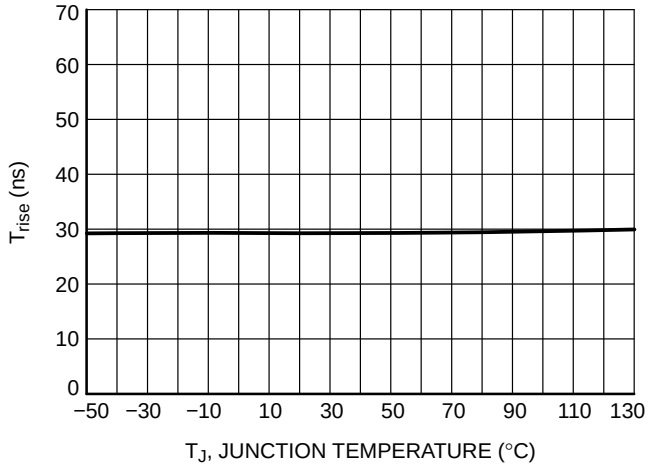


Figure 16. DRV Voltage Rise−Time (C_L = 1 nF, 10−90% of Output Signal) vs. Temperature

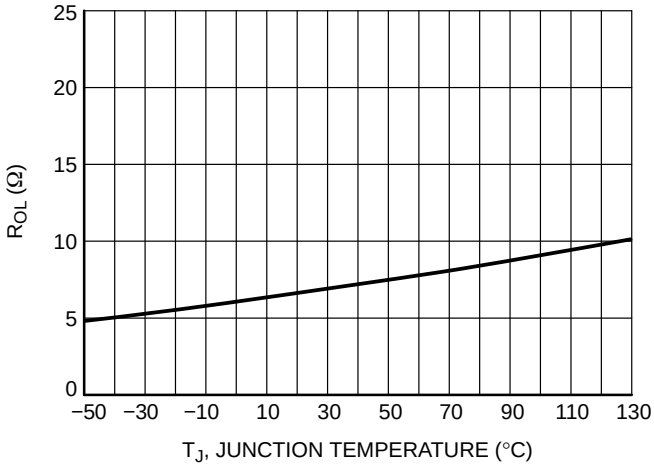


Figure 17. DRV Sink Resistance vs. Temperature

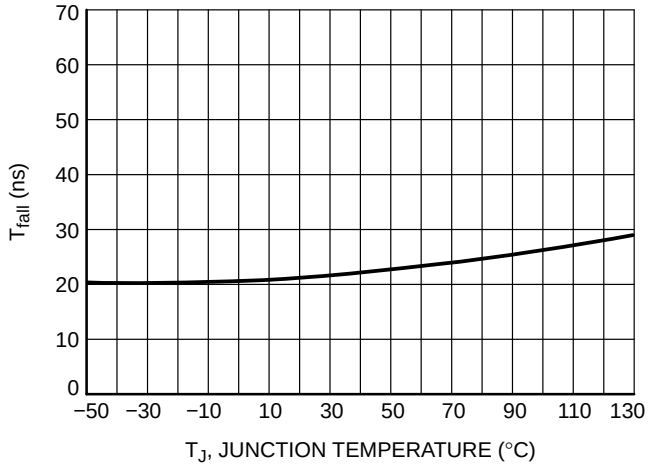


Figure 18. DRV Voltage Fall−Time (C_L = 1 nF, 10−90% of Output Signal) vs. Temperature

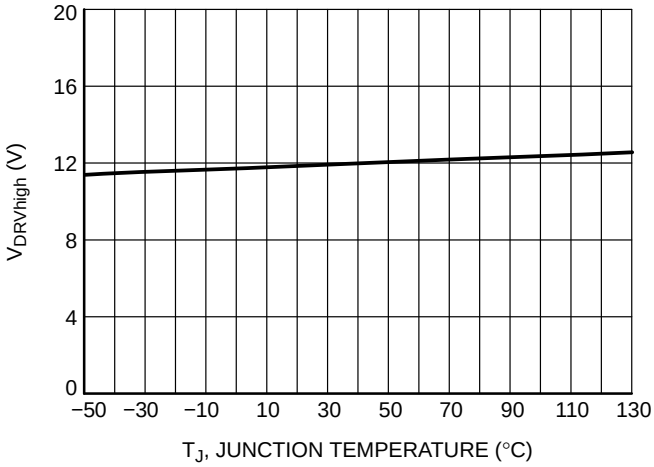


Figure 19. DRV Pin Level @ V_{CC} = 35 V (R_L = 33 kΩ, C_L = 1 nF) vs. Temperature

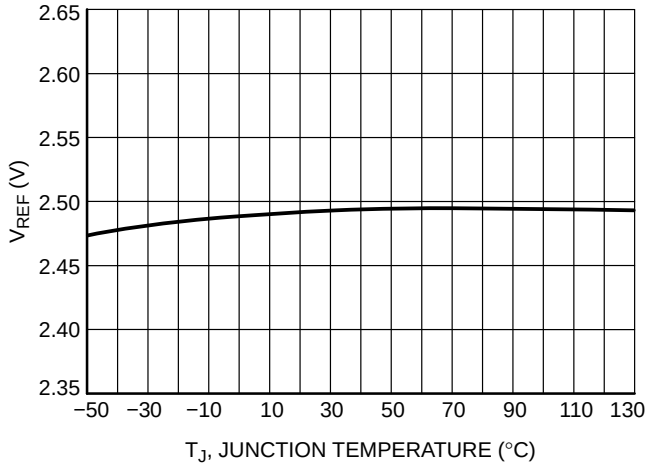


Figure 20. Feedback Reference Voltage vs. Temperature

TYPICAL CHARACTERISTICS

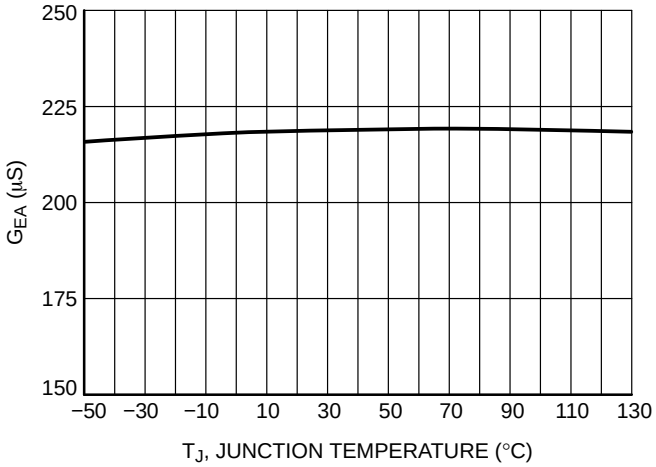


Figure 21. Error Amplifier Transconductance Gain vs. Temperature

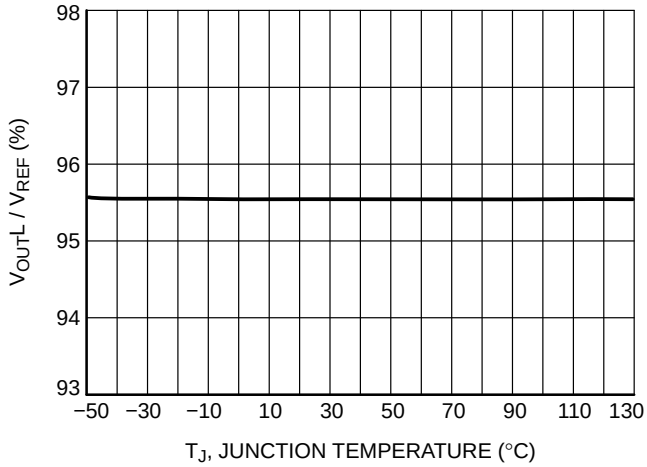


Figure 22. Ratio (V_{OUT} Low Detect Threshold / V_{REF}) vs. Temperature

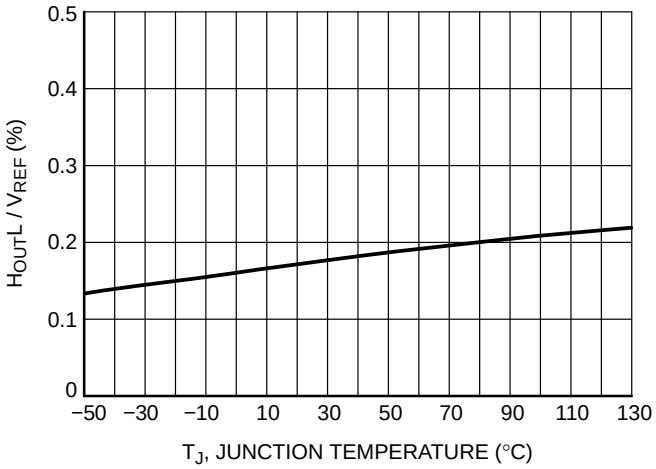


Figure 23. Ratio (V_{OUT} Low Detect Hysteresis / V_{REF}) vs. Temperature

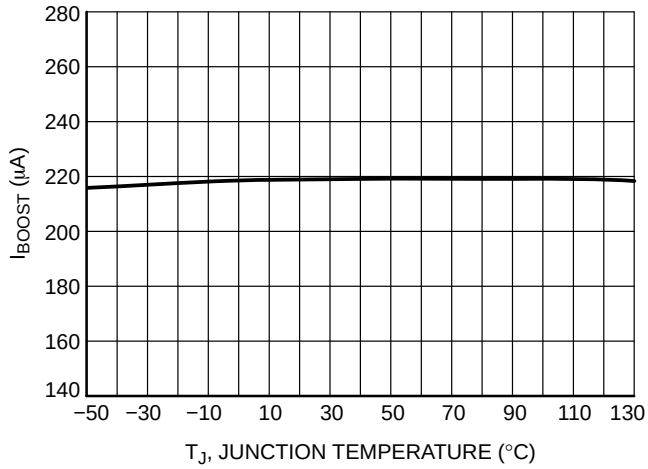


Figure 24. $V_{CONTROL}$ Source Current when (V_{OUT} Low Detect) is Activated for Dynamic Response Enhancer (DRE) vs. Temperature

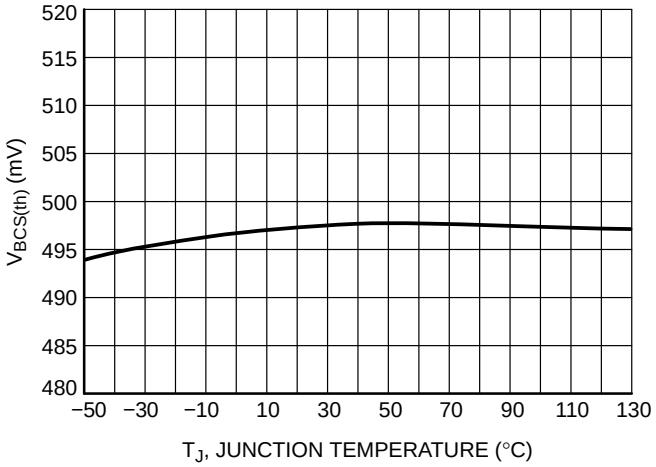


Figure 25. Current Sense Voltage Threshold vs. Temperature

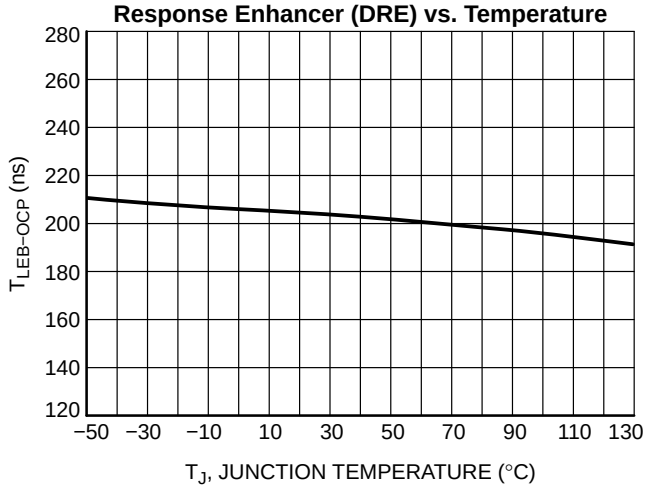


Figure 26. Over−Current Protection Leading Edge Blanking vs. Temperature

TYPICAL CHARACTERISTICS

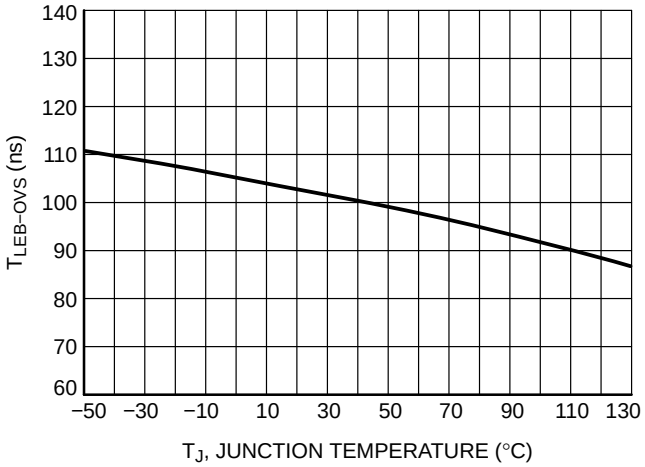


Figure 27. "Overstress" Protection Leading Edge Blanking vs. Temperature

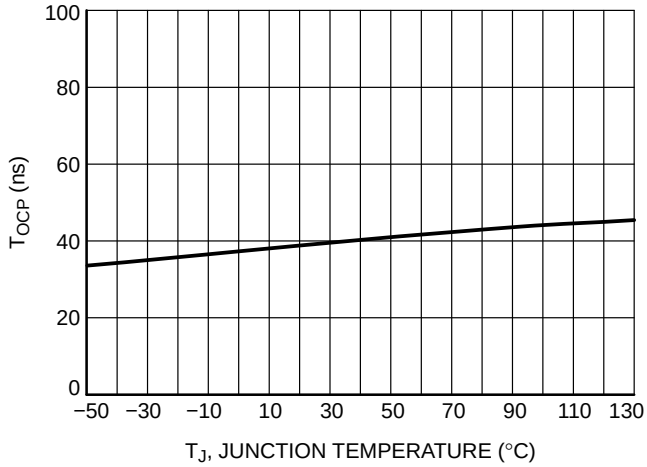


Figure 28. Over−Current Protection Delay from $V_{CS/ZCD} > V_{CS(th)}$ to DRV Low ($dV_{CS/ZCD}$ / dt = 10 V/μs) vs. Temperature

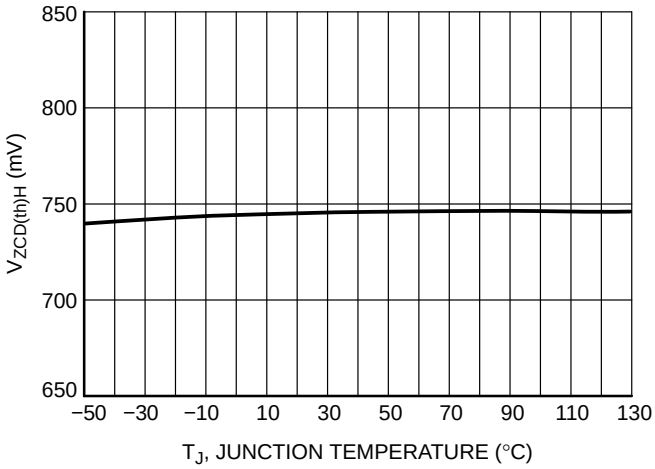


Figure 29. Zero Current Detection, $V_{CS/ZCD}$ Rising vs. Temperature

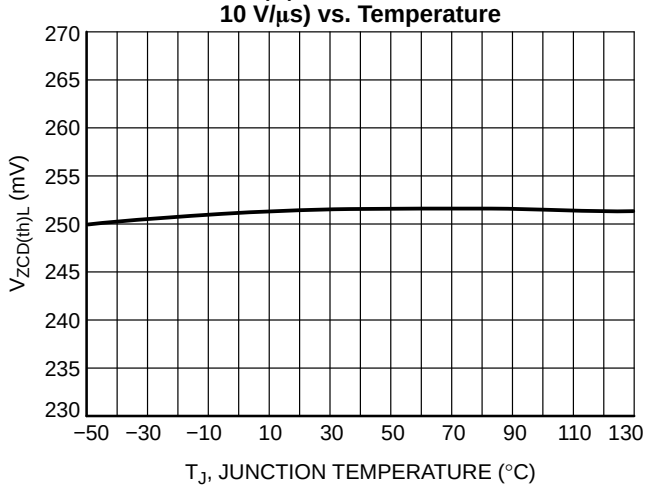


Figure 30. Zero Current Detection, $V_{CS/ZCD}$ Falling vs. Temperature

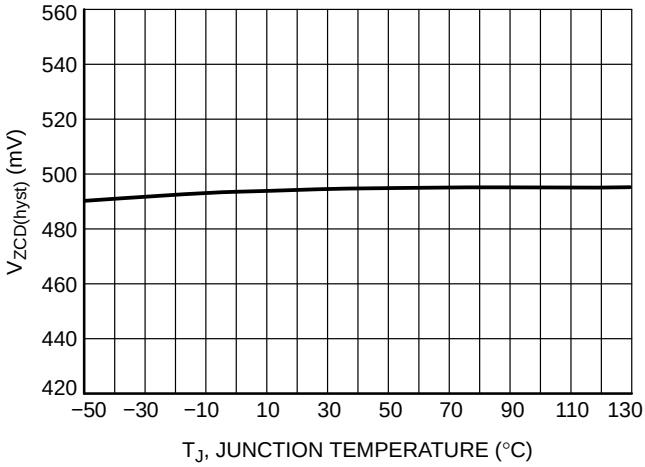


Figure 31. Hysteresis of the Zero Current Detection Comparator vs. Temperature

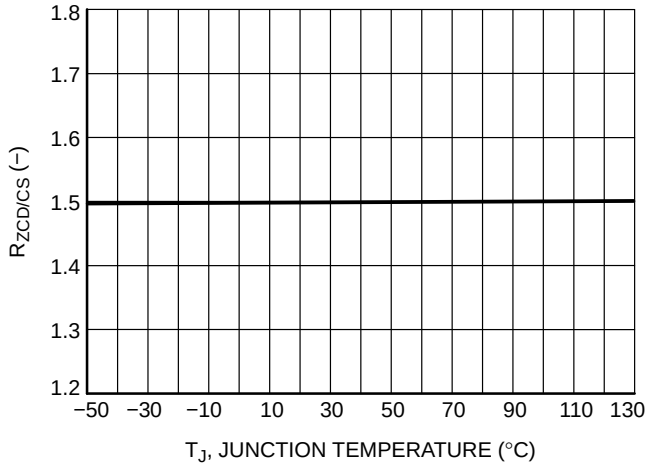


Figure 32. $V_{ZCD(th)}$ over $V_{CS(th)}$ Ratio vs. Temperature

TYPICAL CHARACTERISTICS

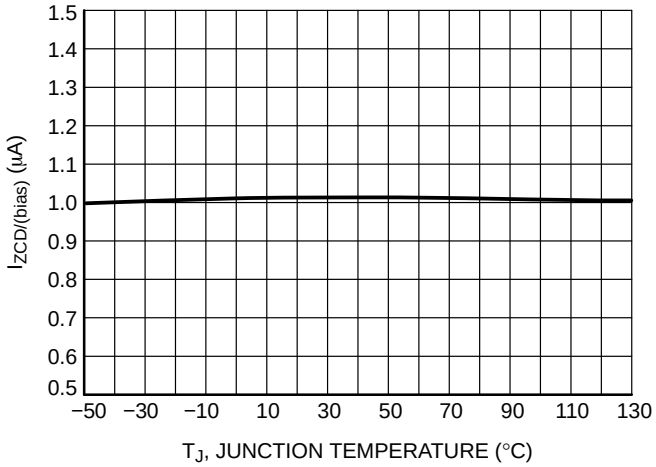


Figure 33. CS/ZCD Pin Bias Current @ $V_{CS/ZCD}$ = 0.75 V vs. Temperature

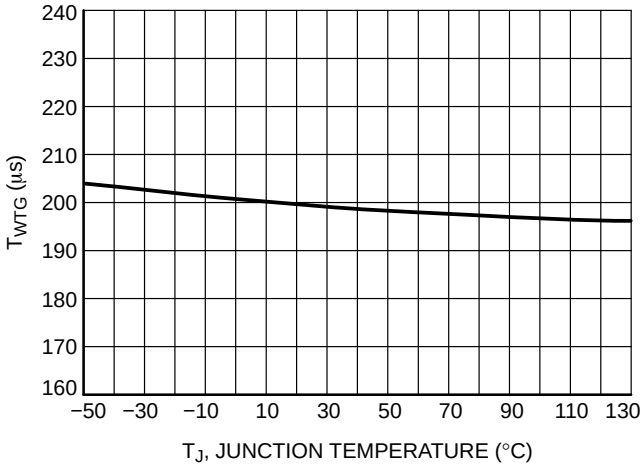


Figure 34. Watchdog Timer vs. Temperature

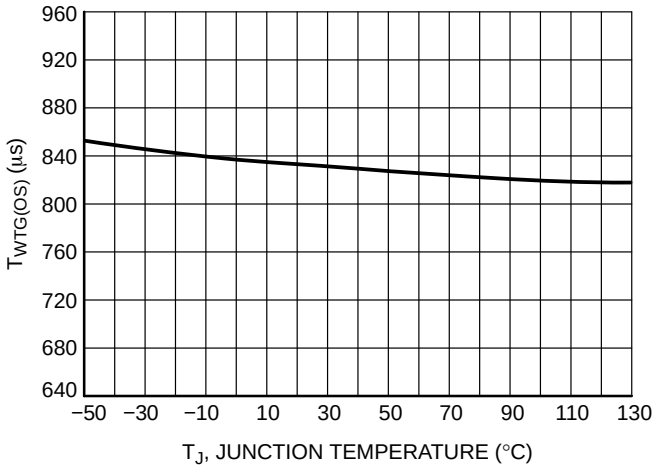


Figure 35. Watchdog Timer in "Overstress" Situation vs. Temperature

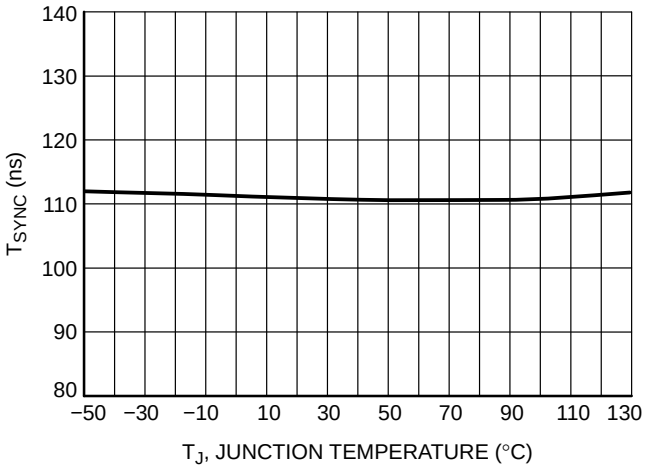


Figure 36. Minimum ZCD Pulse Width for ZCD Detection vs. Temperature

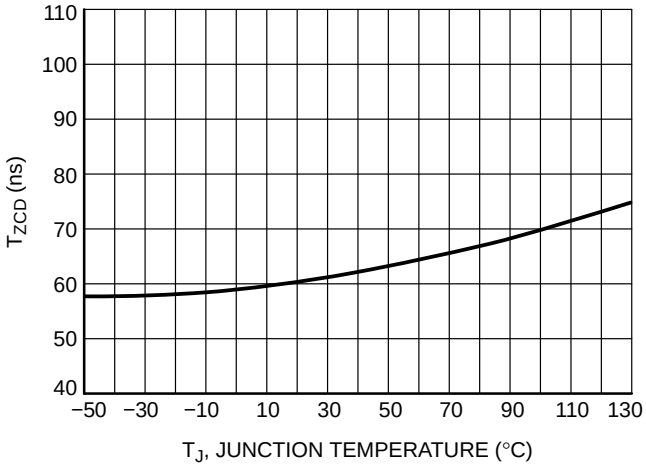


Figure 37. (($V_{CS/ZCD}$ < $V_{ZCD(th)}$) to DRV High) Delay vs. Temperature

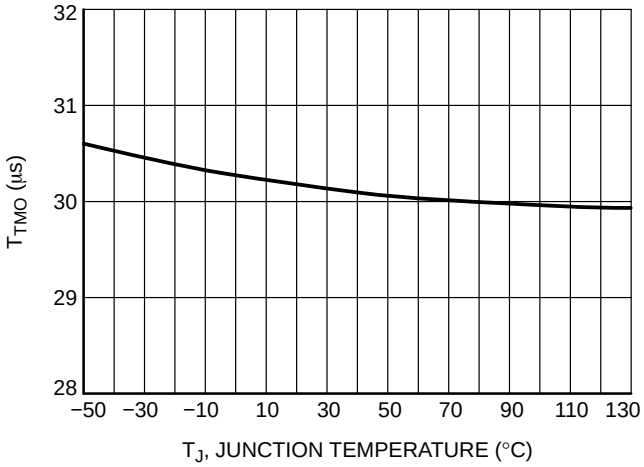


Figure 38. Timeout Timer vs. Temperature

TYPICAL CHARACTERISTICS

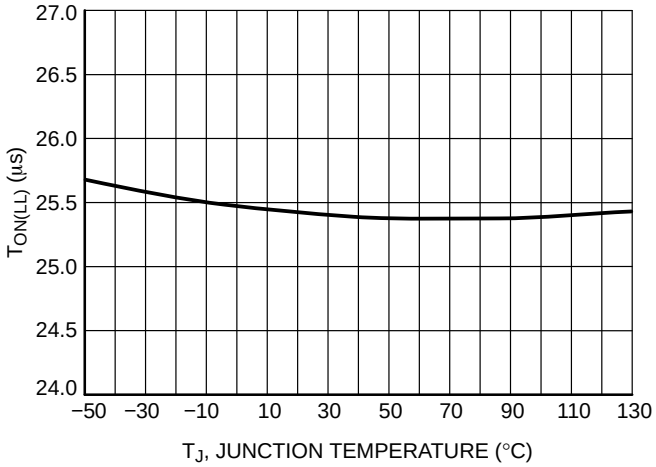


Figure 39. Maximum On Time @ V_{SENSE} = 1.4 V vs. Temperature

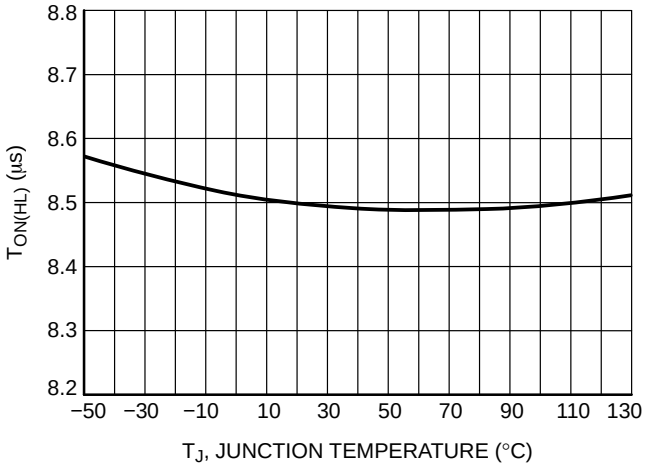


Figure 40. Maximum On Time @ V_{SENSE} = 2.8 V vs. Temperature

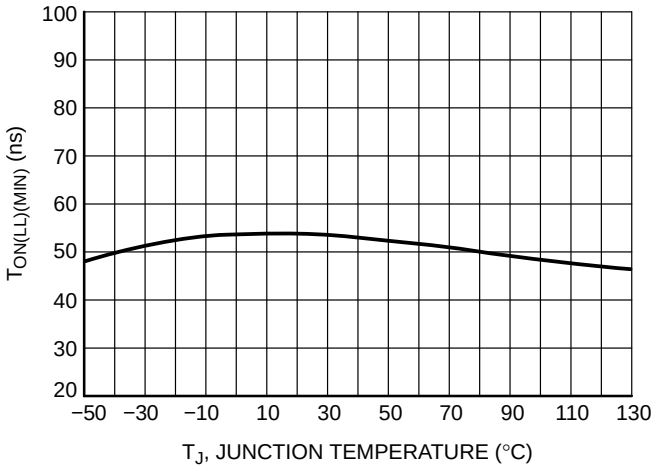


Figure 41. Minimum On Time @ V_{SENSE} = 1.4 V vs. Temperature

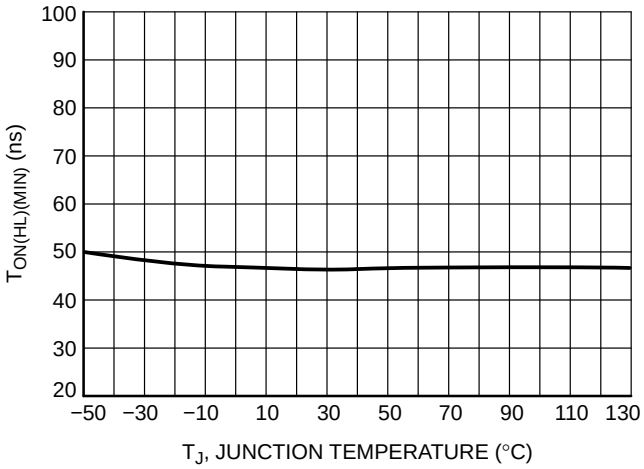


Figure 42. Minimum On Time @ V_{SENSE} = 2.8 V vs. Temperature

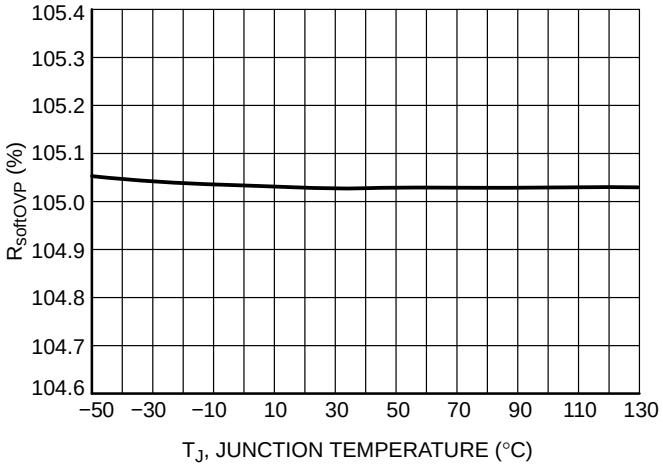


Figure 43. Ratio (Soft OVP Threshold, V_{FB} Rising) over V_{REF} vs. Temperature

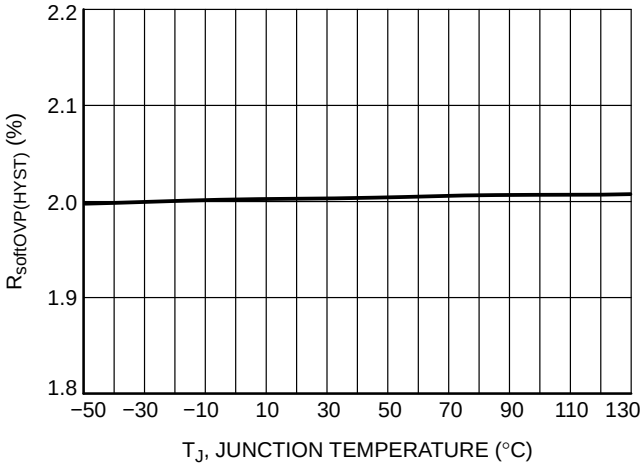


Figure 44. Ratio (Soft OVP Hysteresis) over V_{REF} vs. Temperature

TYPICAL CHARACTERISTICS

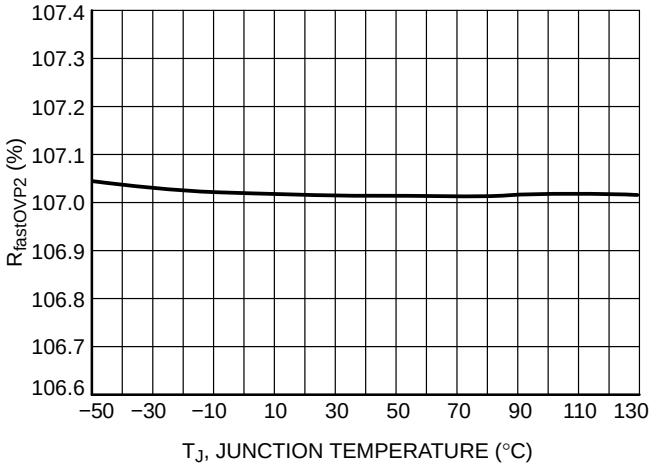


Figure 45. Ratio (Fast OVP Threshold, V_{FB} Rising) over V_{REF} vs. Temperature

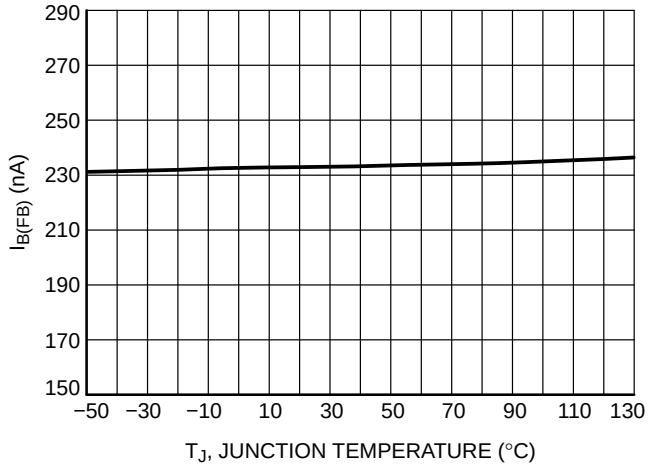


Figure 46. Feedback Pin Bias Current @ V_{FB} = V_{OVP} vs. Temperature

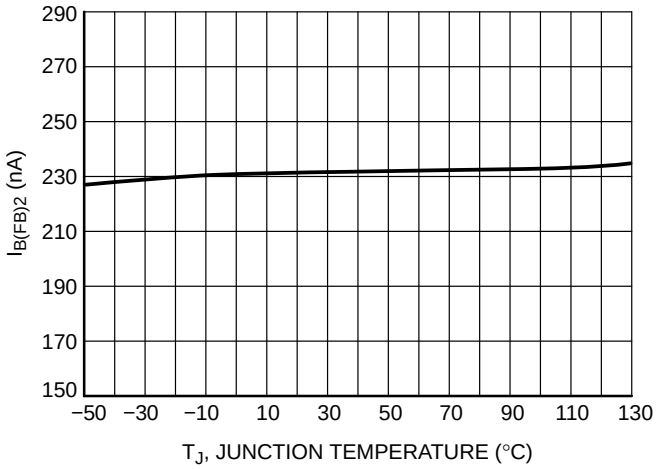


Figure 47. Feedback Pin Bias Current @ V_{FB} = V_{UVP} vs. Temperature

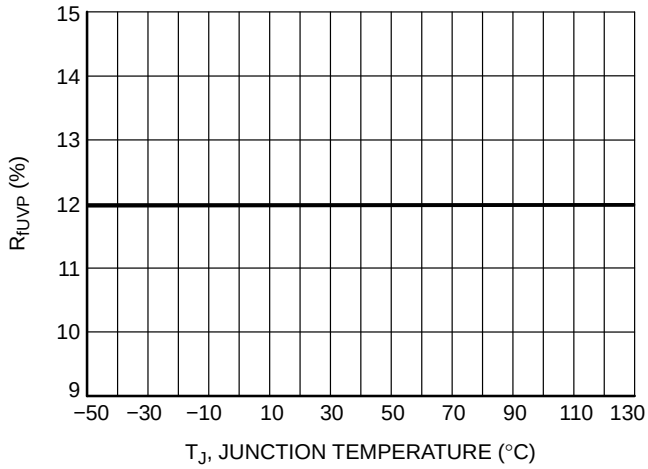


Figure 48. Ratio (UVP Threshold, V_{FB} Rising) over V_{REF} vs. Temperature

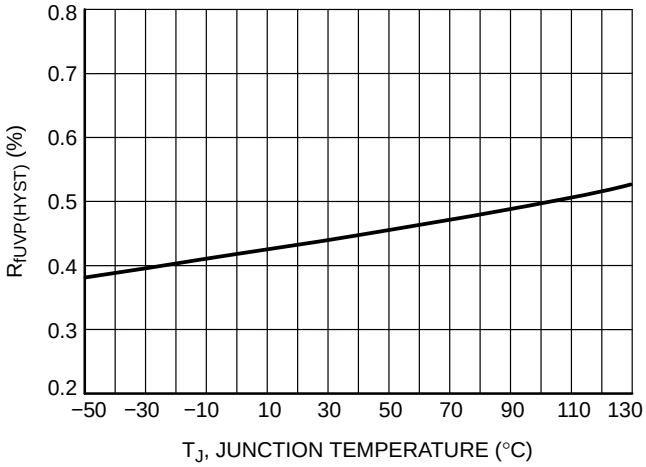


Figure 49. Ratio (UVP Hysteresis) over V_{REF} vs. Temperature

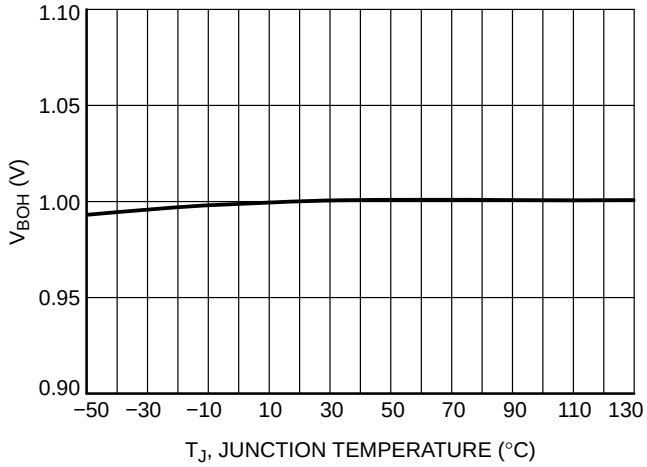


Figure 50. Brown−Out Threshold, V_{SENSE} Rising vs. Temperature

TYPICAL CHARACTERISTICS

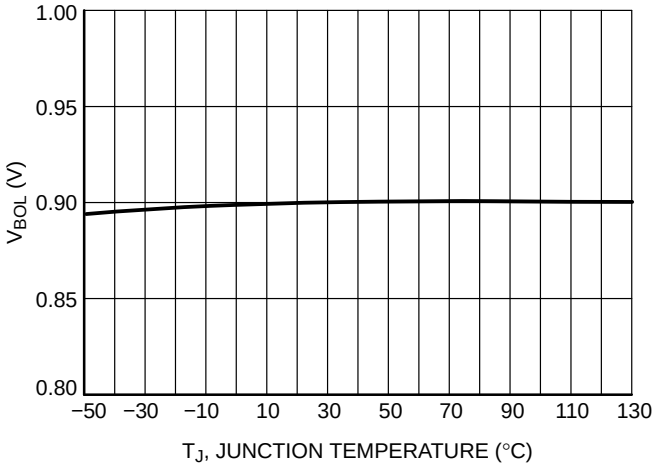


Figure 51. Brown−Out Threshold, V_{SENSE} Falling vs. Temperature

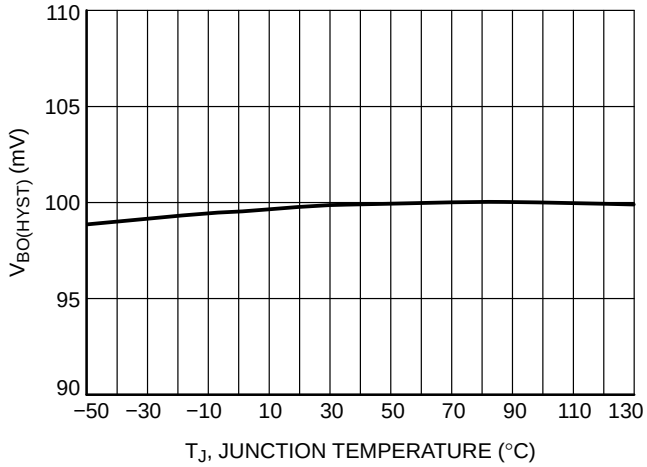


Figure 52. Brown−Out Comparator Hysteresis vs. Temperature

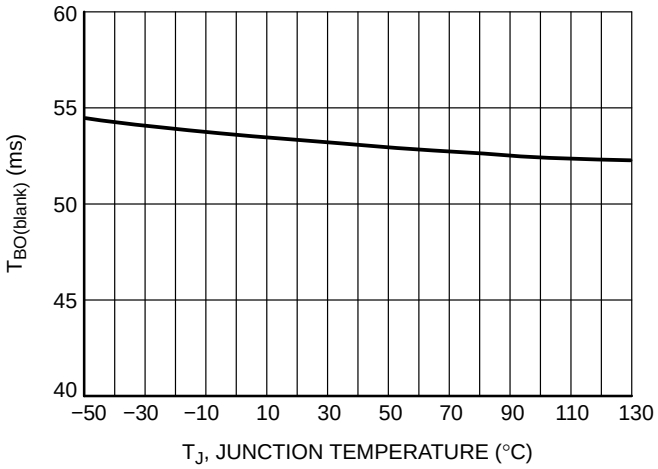


Figure 53. Brown−Out Blanking Time vs. Temperature

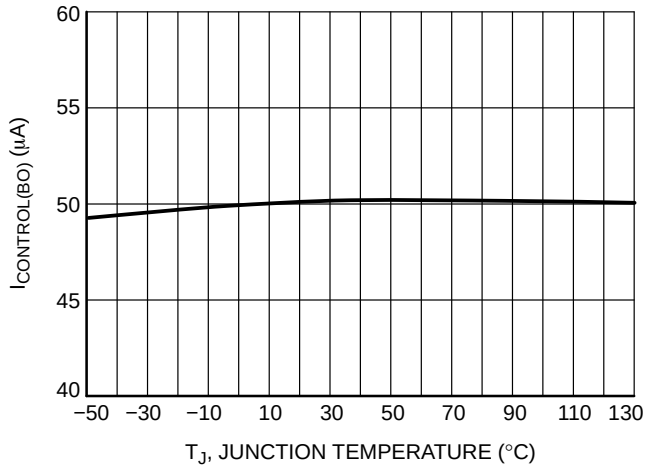


Figure 54. $V_{CONTROL}$ Pin Sink Current when a Brown−Out Situation is Detected vs. Temperature

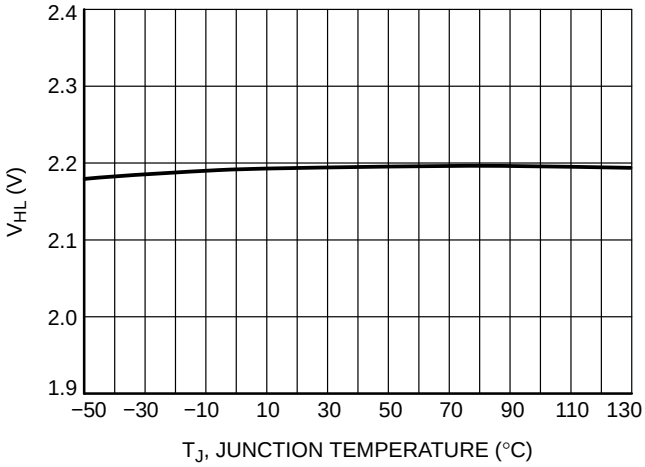


Figure 55. Comparator Threshold for Line Range Detection, V_{SENSE} Rising vs. Temperature

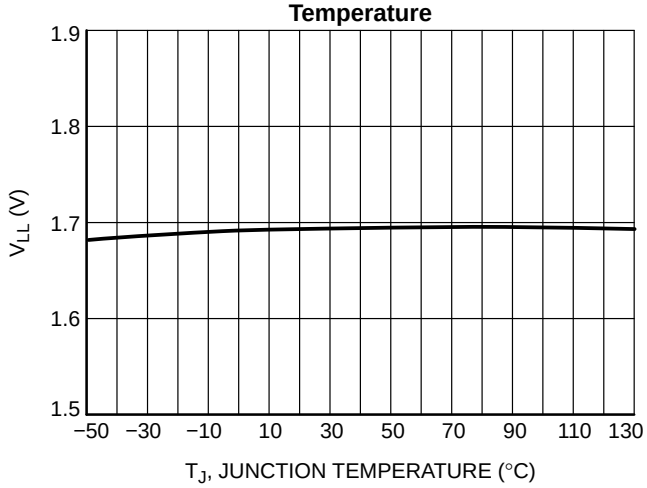


Figure 56. Comparator Threshold for Line Range Detection, V_{SENSE} Falling vs. Temperature

TYPICAL CHARACTERISTICS

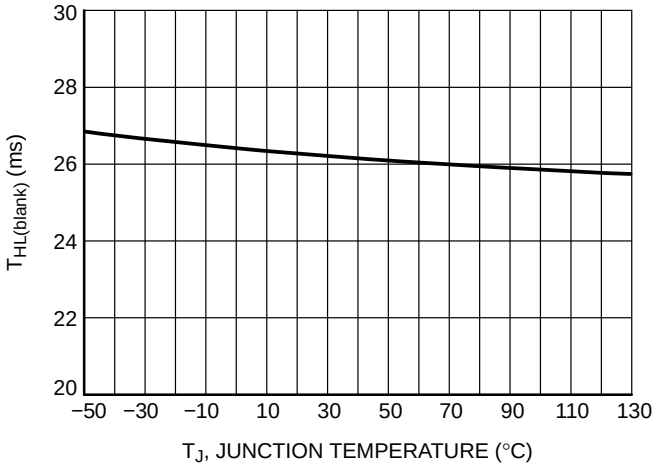


Figure 57. Blanking Time for Line Range Detection vs. Temperature

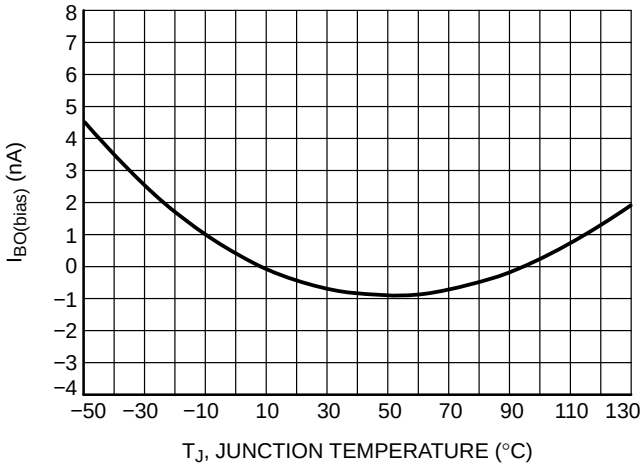


Figure 58. Brown−Out Pin Bias Current, (V_{SENSE} = V_{BOH}) vs. Temperature

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1611 is designed to optimize the efficiency of your PFC stage throughout the load range. In addition, it incorporates protection features for rugged operation. More generally, the NCP1611 is ideal in systems where cost−effectiveness, reliability, low stand−by power and high efficiency are key requirements:

- Current Controlled Frequency Fold−back: the NCP1611 is designed to drive PFC boost stages in so−called Current Controlled Frequency Fold−back (CCFF). In this mode, the circuit classically operates in Critical conduction Mode (CrM) when the inductor current exceeds a programmable value. When the current is below this preset level, the NCP1611 linearly reduces the frequency down to about 20 kHz when the current is zero. CCFF maximizes the efficiency at both nominal and light load. In particular, stand−by losses are reduced to a minimum. Similarly to FCCrM controllers, an internal circuitry allows near−unity power factor even when the switching frequency is reduced.
- Skip Mode: to further optimize the efficiency, the circuit skips cycles near the line zero crossing when the current is very low. This is to avoid circuit operation when the power transfer is particularly inefficient at the cost of current distortion. When superior power factor is required, this function can be inhibited by offsetting the “FFcontrol” pin by 0.75 V.
- Low Start−up Current and large V_{CC} range (B version): The start−up consumption of the circuit is minimized to allow the use of high−impedance start−up resistors to pre−charge the V_{CC} capacitor. Also, the minimum value of the UVLO hysteresis is 6 V to avoid the need for large V_{CC} capacitors and help shorten the start−up time without the need for too dissipative start−up elements. The A version is preferred in applications where the circuit is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start−up level (11.25 V) is set low enough so that the circuit can be powered from a 12−V rail. After start−up, the high V_{CC} maximum rating allows a large operating range from 9.5 V up to 35 V.
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer): since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start−up) may cause excessive over or under−shoot. This circuit limits possible deviations from the regulation level as follows:
  - The NCP1611 linearly decays the power delivery to zero when the output voltage exceeds 105% of its desired level (soft OVP). If this soft OVP is too smooth and the output continues to rise, the circuit immediately interrupts the power delivery when the output voltage is 107% above its desired level.
  - The NCP1611 dramatically speeds−up the regulation loop when the output voltage goes below 95.5% of its regulation level. In A version, this function is enabled only after the PFC stage has started−up to allow normal soft−start operation to occur.
- Safety Protections: the NCP1611 permanently monitors the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over−stress making the PFC stage extremely robust and reliable. In addition to the OVP protection, these methods of protection are provided:

- Maximum Current Limit: the circuit senses the MOSFET current and turns off the power switch if the set current limit is exceeded. In addition, the circuit enters a low duty−cycle operation mode when the current reaches 150% of the current limit as a result of the inductor saturation or a short of the bypass diode.
- Under−Voltage Protection: this circuit turns off when it detects that the output voltage is below 12% of the voltage reference (typically). This feature protects the PFC stage if the ac line is too low or if there is a failure in the feedback network (e.g., bad connection).
- Brown−Out Detection: the circuit detects low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.
- Thermal Shutdown: an internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).

- Output Stage Totem Pole: the NCP1611 incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

NCP1611 Operation Modes

As mentioned, the NCP1611 PFC controller implements a Current Controlled Frequency Fold−back (CCFF) where:

- The circuit operates in classical Critical conduction Mode (CrM) when the inductor current exceeds a programmable value.
- When the current is below this preset level, the NCP1611 linearly reduces the operating frequency down to about 20 kHz when the current is zero.

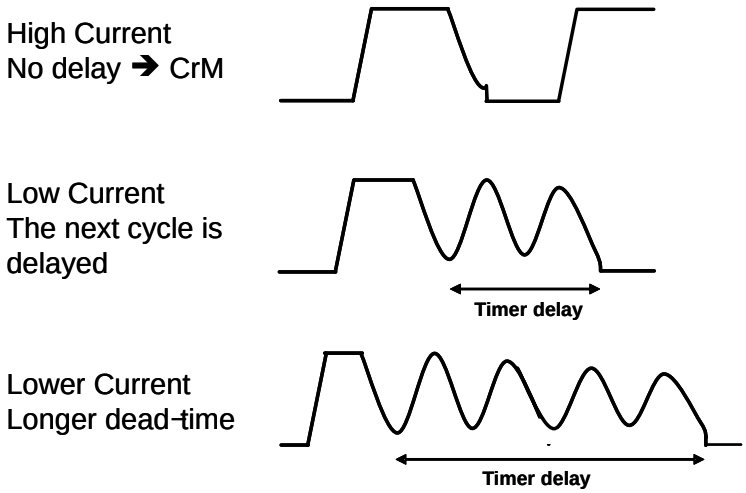
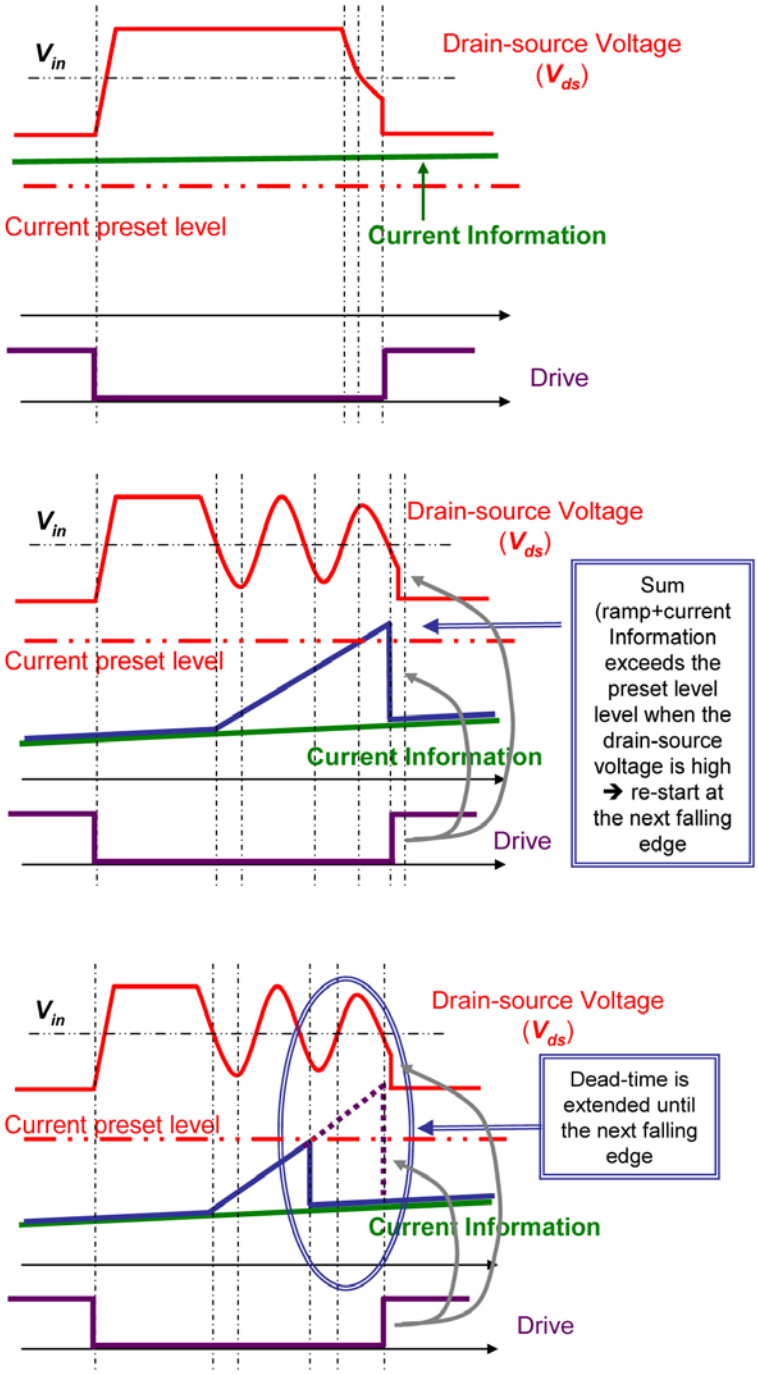


Figure 59. CCFF Operation

As illustrated in Figure 59, under high load conditions, the boost stage is operating in CrM but as the load is reduced, the controller enters controlled frequency discontinuous operation.

Figure 60 details the operation. A voltage representative of the input current (“current information”) is generated. If this signal is higher than a 2.5 V internal reference (named “Dead−Time Ramp Threshold” in Figure 60), there is no dead−time and the circuit operates in CrM. If the current information is lower than the 2.5 V threshold, a dead−time is inserted that lasts for the time necessary for the internal ramp to reach 2.5 V from the current information floor. Hence, the lower the current information is, the longer the dead−time. When the current information is 0.75 V, the dead−time is approximately 45 μs.

To further reduce the losses, the MOSFET turns on is stretched until its drain−source voltage is at its valley. As illustrated in Figure 60, the ramp is synchronized to the drain−source ringing. If the ramp exceeds the 2.5 V threshold while the drain−source voltage is below V_{in}, the ramp is extended until it oscillates above V_{in} so that the drive will turn on at the next valley.



Top: CrM operation when the current information exceeds the preset level during the demagnetization phase
Middle: the circuit re−starts at the next valley if the sum (ramp + current information) exceeds the preset level during the dead−time, while the drain−source voltage is high
Bottom: the sum (ramp + current information) exceeds the preset level while during the dead−time, the drain−source voltage is low. The circuit skips the current valley and re−starts at the following one.

Figure 60. Dead−Time Generation

Current Information Generation

The "FFcontrol" pin sources a current that is representative of the input current. In practice, I_{pin3} is built by multiplying the internal control signal (V_{REGUL}, i.e., the internal signal that controls the on−time) by the sense voltage (pin 2) that is proportional to the input voltage. The multiplier gain (K_m of Figure 61) is three times less in high−line conditions (that is when the "LLine" signal from the brown−out block is in low state) so that I_{pin3} provides a voltage representative of the input current across resistor R_{FF} placed between pin 3 and ground. Pin 3 voltage is the current information.

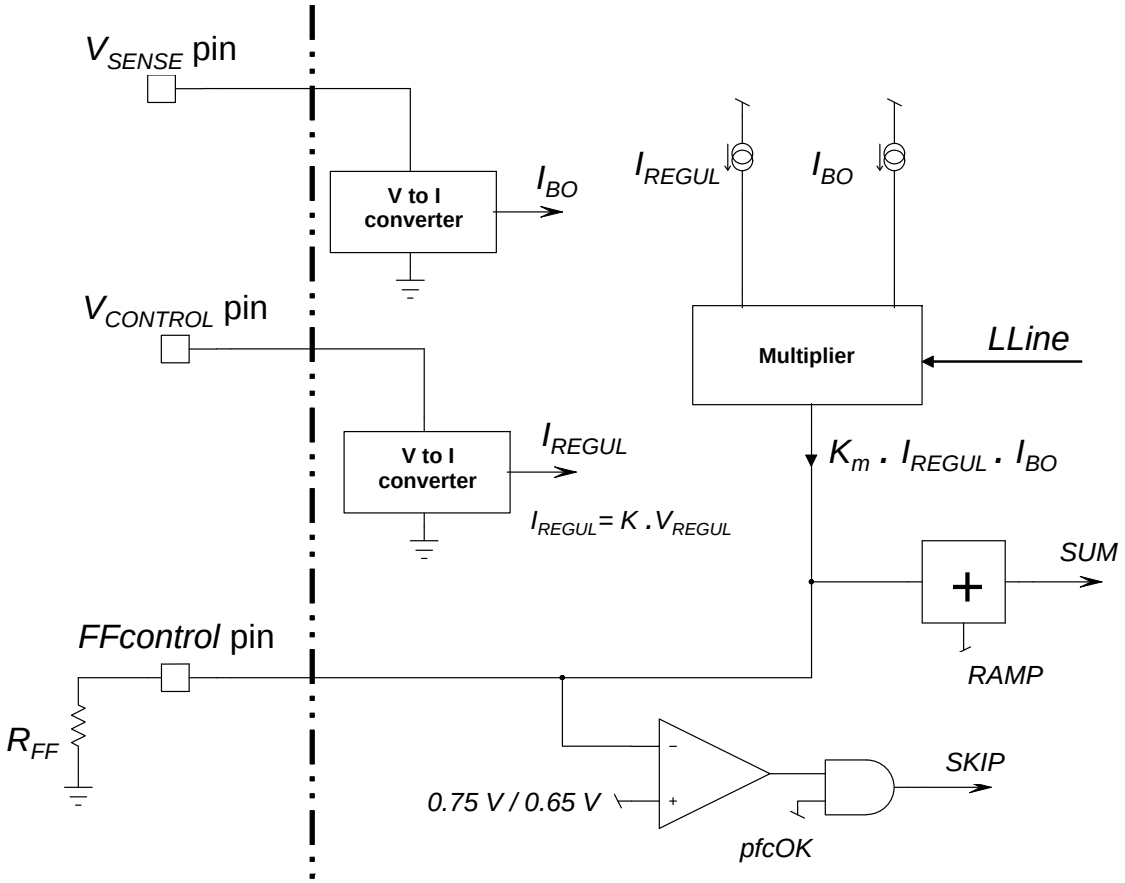


Figure 61. Generation of the Current Information

Skip Mode

As illustrated in Figure 61, the circuit also skips cycles near the line zero crossing where the current is very low. A comparator monitors the pin 3 voltage (“*FFcontrol*” voltage) and inhibits the drive when V_{pin3} is lower than a 0.65 V internal reference. Switching resumes when V_{pin3} exceeds 0.75 V (0.1 V hysteresis). This inhibits circuit operation when the power transfer is particularly inefficient at the expense of slightly increased current distortion. When superior power factor is needed, this function can be inhibited offsetting the “FFcontrol” pin by 0.75 V. The skip mode capability is disabled whenever the PFC stage is not in nominal operation (as dictated by the “pfcOK” signal − see block diagram and “pfcOK Internal Signal” Section).

The circuit does not abruptly interrupt the switching when V_{pin3} goes below 0.65 V. Instead, the signal V_{TON} that controls the on−time is gradually decreased by grounding the V_{REGUL} signal applied to the V_{TON} processing block (see Figure 9). Doing so, the on−time smoothly decays to zero in three to four switching periods typically. Figure 62 shows the practical implementation.

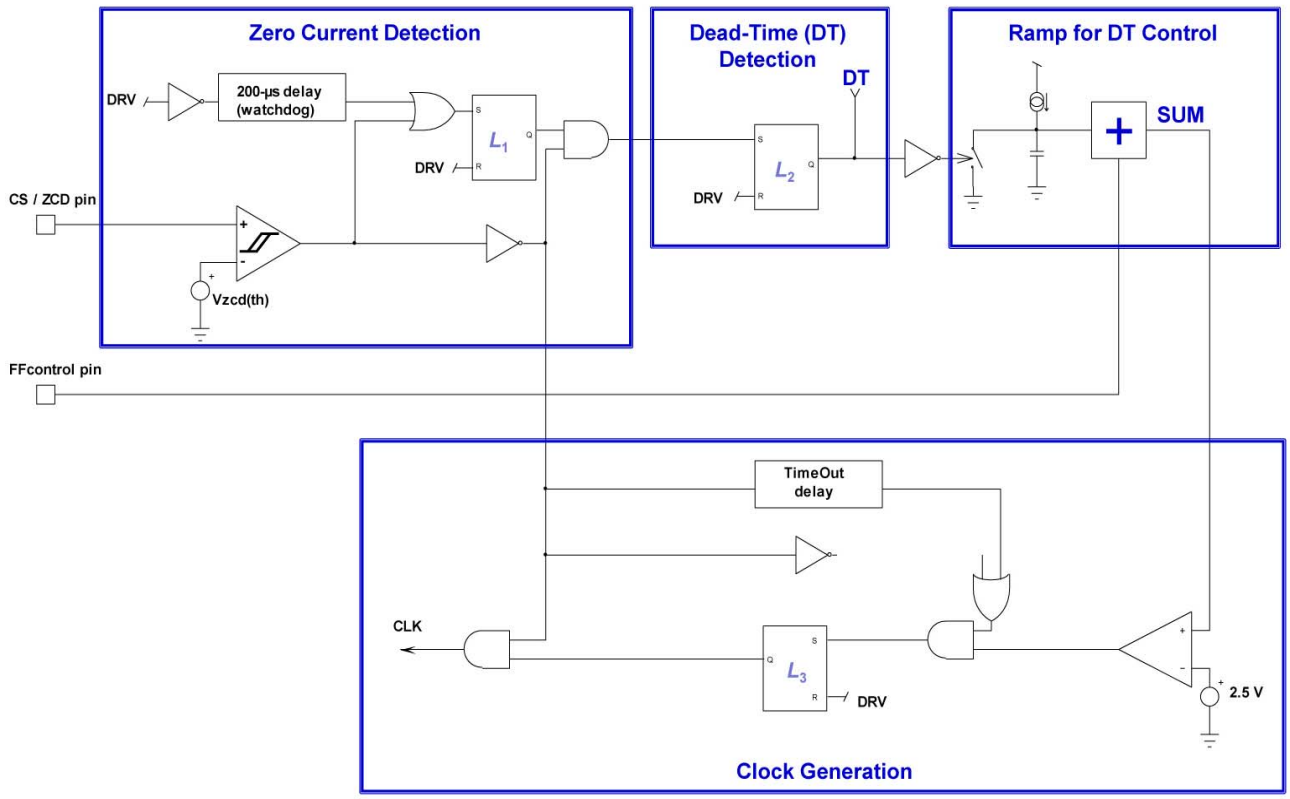


Figure 62. CCFF Practical Implementation

CCFF maximizes the efficiency at both nominal and light load. In particular, the stand−by losses are reduced to a minimum. Also, this method avoids that the system stalls between valleys. Instead, the circuit acts so that the PFC stage transitions from the n valley to (n + 1) valley or vice versa from the n valley to (n − 1) cleanly as illustrated by Figure 63.

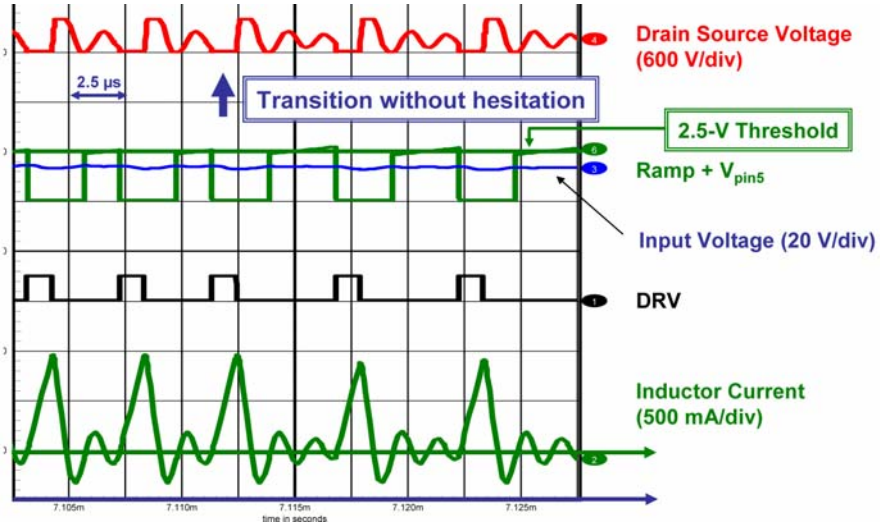


Figure 63. Clean Transition Without Hesitation Between Valleys

NCP1611 On−time Modulation

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is (V_{IN}/L) where L is the coil inductance. At the end of the on−time (t_1), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is (t_2).

In some cases, the system enters then the dead−time (t_3) that lasts until the next clock is generated.

One can show that the ac line current is given by:

$$I_{in} = V_{in}\left[\frac{t_1(t_1 + t_2)}{2TL}\right] \quad \text{(eq. 1)}$$

Where $T = (t_1 + t_2 + t_3)$ is the switching period and V_{in} is the ac line rectified voltage.

In light of this equation, we immediately note that I_{in} is proportional to V_{in} if $[t_1 (t_1 + t_2) / T]$ is a constant.

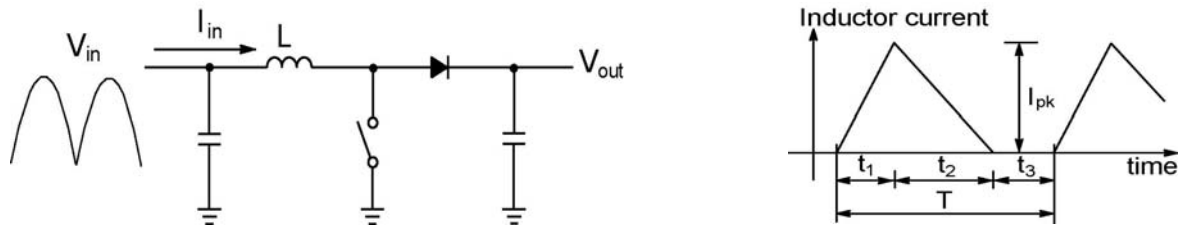


Figure 64. PFC Boost Converter (left) and Inductor Current in DCM (right)

The NCP1611 operates in voltage mode. As portrayed by Figure 8, the MOSFET on−time t_1 is controlled by the signal V_{ton} generated by the regulation block and an internal ramp as follows:

$$t_1 = \frac{C_{ramp} \cdot V_{ton}}{I_{ch}} \quad \text{(eq. 2)}$$

The charge current is constant at a given input voltage (as mentioned, it is 3 times higher at high line compared to its value at low line). C_{ramp} is an internal capacitor.

The output of the regulation block ($V_{CONTROL}$) is linearly transformed into a signal (V_{REGUL}) varying between 0 and 1 V. (V_{REGUL}) is the voltage that is injected into the PWM section to modulate the MOSFET duty−cycle. The NCP1611 includes some circuitry that processes (V_{REGUL}) to form the signal (V_{ton}) that is used in the PWM section (see Figure 9). (V_{ton}) is modulated in response to the dead−time sensed during the precedent current cycles, that is, for a proper shaping of the ac line current. This modulation leads to:

$$V_{ton} = \frac{T \cdot V_{REGUL}}{t_1 + t_2} \quad \text{(eq. 3)}$$

or

$$V_{ton} \cdot \frac{t_1 + t_2}{T} = V_{REGUL}$$

Given the low regulation bandwidth of the PFC systems, ($V_{CONTROL}$) and then (V_{REGUL}) are slow varying signals. Hence, the ($V_{ton} \bullet (t_1 + t_2) / T$) term is substantially constant. Provided that in addition, (t_1) is proportional to (V_{ton}), Equation 1 leads to: ($I_{in} = k \bullet V_{in}$), where k is a constant. More exactly:

$$I_{in} = k \cdot V_{in}$$

$$\text{where : } k = \text{constant} = \left[\frac{1}{2L} \cdot \frac{V_{REGUL}}{(V_{REGUL})_{max}} \cdot t_{on,max}\right]$$

Where $t_{on,max}$ is the maximum on−time obtained when V_{REGUL} is at its $(V_{REGUL})_{max}$ maximum level. The parametric table shows that $t_{on,max}$ is equal to 25 μs ($T_{ON(LL)}$) at low line and to 8.3 μs ($T_{ON(HL)}$) at high line (when pin2 happens to exceed 2.2 V with a pace higher than 40 Hz – see BO 25 ms blanking time).

The input current is then proportional to the input voltage. Hence, the ac line current is properly shaped.

One can note that this analysis is also valid in the CrM case. This condition is just a particular case of this functioning where (t_3=0), which leads to (t_1+t_2=T) and (V_{TON}=V_{REGUL}). That is why the NCP1611 automatically adapts to the conditions and transitions from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

Hence, we can re−write the above equation as follows:

$$I_{in} = \frac{V_{in} \cdot T_{ON(LL)}}{2 \cdot L} \cdot \frac{V_{REGUL}}{(V_{REGUL})max}$$

at low line.

$$I_{in} = \frac{V_{in} \cdot T_{ON(HL)}}{2 \cdot L} \cdot \frac{V_{REGUL}}{(V_{REGUL})max}$$

at high line.

From these equations, we can deduce the expression of the average input power:

$$P_{in,avg} = \frac{(V_{in,rms})^2 \cdot V_{REGUL} \cdot T_{ON(LL)}}{2 \cdot L \cdot (V_{REGUL})_{max}}$$

at low line

$$P_{in,avg} = \frac{(V_{in,rms})^2 \cdot V_{REGUL} \cdot T_{ON(HL)}}{2 \cdot L \cdot (V_{REGUL})_{max}}$$

at high line

Where $(V_{REGUL})_{max}$ is the 1 V V_{REGUL} maximum value.

Hence, the maximum power that can be delivered by the PFC stage is:

$$\left(P_{in,avg}\right)_{max} = \frac{\left(V_{in,rms}\right)^2 \cdot T_{ON(LL)}}{2 \cdot L}$$

at low line

$$\left(P_{in,avg}\right)_{max} = \frac{\left(V_{in,rms}\right)^2 \cdot T_{ON(HL)}}{2 \cdot L}$$

at high line

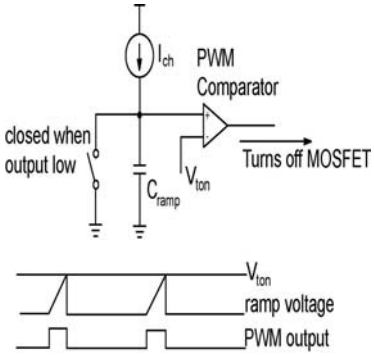


Figure 65. PWM circuit and timing diagram.

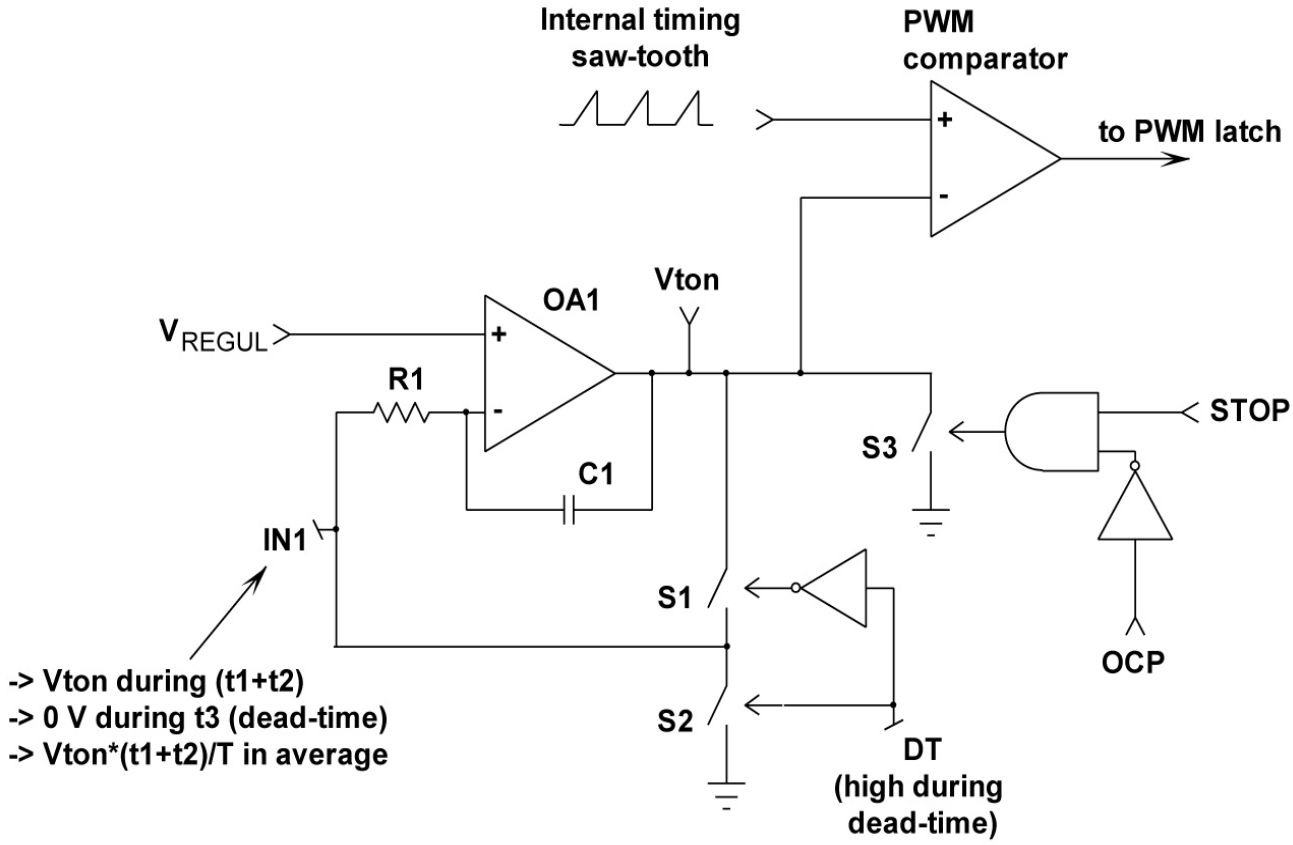


Figure 66. V_{TON} Processing Circuit. The integrator OA1 amplifies the error between V_{REGUL} and IN1 so that on average, (V_{TON} * (t_1+t_2)/T) equates V_{REGUL}.

Remark:

The "V_{ton} processing circuit" is "informed" when a condition possibly leading to a long interruption of the drive activity (functions generating the STOP signal that disables the drive – see block diagram − except OCP, i.e., OVP, OverStress, SKIP, staticOVP and OFF). Otherwise, such situations would be viewed as a normal dead−time phase and V_{ton} would inappropriately over−dimension V_{ton} to compensate it. Instead, as illustrated in Figure 66, the V_{ton} signal is grounded leading to a short soft−start when the circuit recovers.

Regulation Block and Output Voltage Control

A trans−conductance error amplifier (OTA) with access to the inverting input and output is provided. It features a typical trans−conductance gain of 200 μS and a maximum capability of ±20 μA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (pin 8). Bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. However, it is high enough so that the pin remains in low state if the pin is not connected.

The output of the error amplifier is brought to pin 1 for external loop compensation. Typically a type 2 network is applied between pin1 and ground, to set the regulation bandwidth below about 20 Hz and to provide a decent phase boost.

The swing of the error amplifier output is limited within an accurate range:

- It is forced above a voltage drop (V_F) by some circuitry.
- It is clamped not to exceed 4.0 V + the same V_F voltage drop.

Hence, V_{pin1} features a 4 V voltage swing. V_{pin1} is then offset down by (V_F) and scaled down by a resistors divider before it connects to the "V_{TON} processing block" and the PWM section. Finally, the output of the regulation block is a signal ("V_{REGUL}" of the block diagram) that varies between 0 and a top value corresponding to the maximum on−time.

The V_F value is 0.5 V typically.

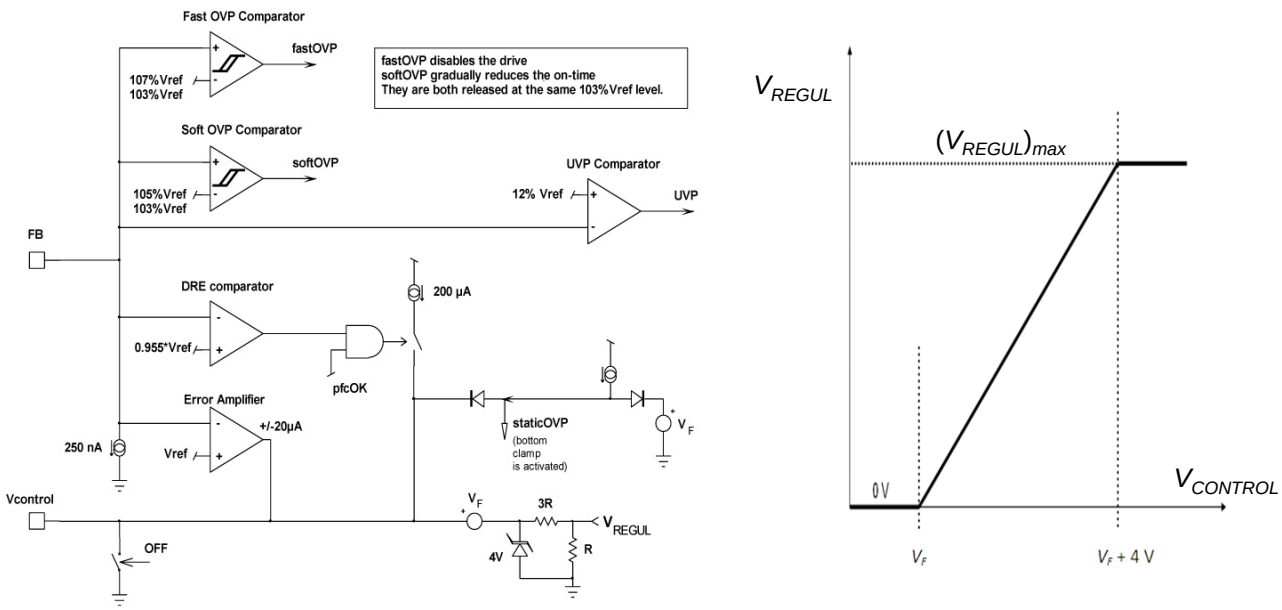


Figure 67. a) Regulation Block Figure (left), b) Correspondence Between $V_{CONTROL}$ and V_{REGUL} (right)

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or under−shoot. Over−shoot is limited by the Over−Voltage Protection connected to pin 8.

The NCP1611 embeds a "***dynamic response enhancer***" circuitry (DRE) that contains under−shoots. An internal comparator monitors the feed−back (V_{pin8}) and when V_{pin8} is lower than 95.5% of its nominal value, it connects a 200 µA current source to speed−up the charge of the compensation network. Effectively this appears as a 10x increase in the loop gain.

In A version, DRE is disabled during the start−up sequence until the PFC stage has stabilized (that is when the "pfcOK" signal of the block diagram, is high). The resulting slow and gradual charge of the pin1 voltage ($V_{CONTROL}$) softens the soft start−up sequence. In B version, DRE is enabled during start−up to speed−up this phase and allow for the use of smaller V_{CC} capacitors.

The circuit also detects overshoot and immediately reduces the power delivery when the output voltage exceeds 105% of its desired level. The NCP1611 does not abruptly interrupt the switching. Instead, the signal V_{TON} that controls the on−time is gradually decreased by grounding the V_{REGUL} signal applied to the V_{TON} processing block (see Figure 66). Doing so, the on−time smoothly decays to zero in four to five switching periods typically. If the output voltage still increases, a second comparator immediately disables the driver if the output voltage exceeds 107% of its desired level.

The error amplifier OTA and the OVP, UVP and DRE comparators share the same input information. Based on the typical value of their parameters and if ($V_{out,nom}$) is the output voltage nominal value (e.g., 390 V), we can deduce:

- Output Regulation Level: $V_{out,nom}$
- Output UVP Level: $V_{out,uvp}$ = 12% x $V_{out,nom}$
- Output DRE Level: $V_{out,dre}$ = 95.5% x $V_{out,nom}$
- Output Soft OVP Level: $V_{out,sovp}$ = 105% x $V_{out,nom}$
- Output Fast OVP level: $V_{out,fovp}$ = 107% x $V_{out,nom}$

Current Sense and Zero Current Detection

The NCP1611 is designed to monitor the current flowing through the power switch. A current sense resistor (R_{sense}) is inserted between the MOSFET source and ground to generate a positive voltage proportional to the MOSFET current (V_{CS}). The V_{CS} voltage is compared to a 500 mV internally reference. When V_{CS} exceeds this threshold, the

OCP signal turns high to reset the PWM latch and forces the driver low. A 200 ns blanking time prevents the OCP comparator from tripping because of the switching spikes that occur when the MOSFET turns on.

The CS pin is also designed to receive a signal from an auxiliary winding for Zero Current Detection. As illustrated in Figure 68, an internal ZCD comparator monitors the pin4 voltage and if this voltage exceeds 750 mV, a demagnetization phase is detected (signal ZCD is high). The auxiliary winding voltage is applied thought a diode to prevent this signal from distorting the current sense information during the on−time. Thus, the OCP protection is not impacted by the ZCD sensing circuitry. This comparator incorporates a 500 mV hysteresis and is able to detect ZCD pulses longer than 200 ns. When pin4 voltage drops below the lower ZCD threshold, the driver can turn high within 200 ns.

It may happen that the MOSFET turns on while a huge current flows through the inductor. As an example such a situation can occur at start−up when large in−rush currents charge the bulk capacitor to the line peak voltage. Traditionally, a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current. If this diode is accidently shorted, the MOSFET will also see a high current when it turns on. In both cases, the current can be large enough to trigger the ZCD comparator. An AND gate detects that this event occurs while the drive signal is high. In this case, the “OverStress” signal goes high and disables the driver for an 800 µs delay. This long delay leads to a very low duty−ratio operation in case of “OverStress” fault in order to limit the risk of overheating.

When no signal is received that triggers the ZCD comparator during the off−time, an internal 200−µs watchdog timer initiates the next drive pulse. At the end of this delay, the circuit senses the CS/ZCD pin impedance to detect a possible grounding of this pin and prevent operation. The CS/ZCD external components must be selected to avoid false fault detection. 3.9 kΩ is the recommended minimum impedance to be applied to the CS/ZCD pin when considering the NCP1611 parameters tolerance over the −40°C to 125°C temperature range. **Practically, R_{cs} must be higher than 3.9 kΩ in the application of Figure 68.**

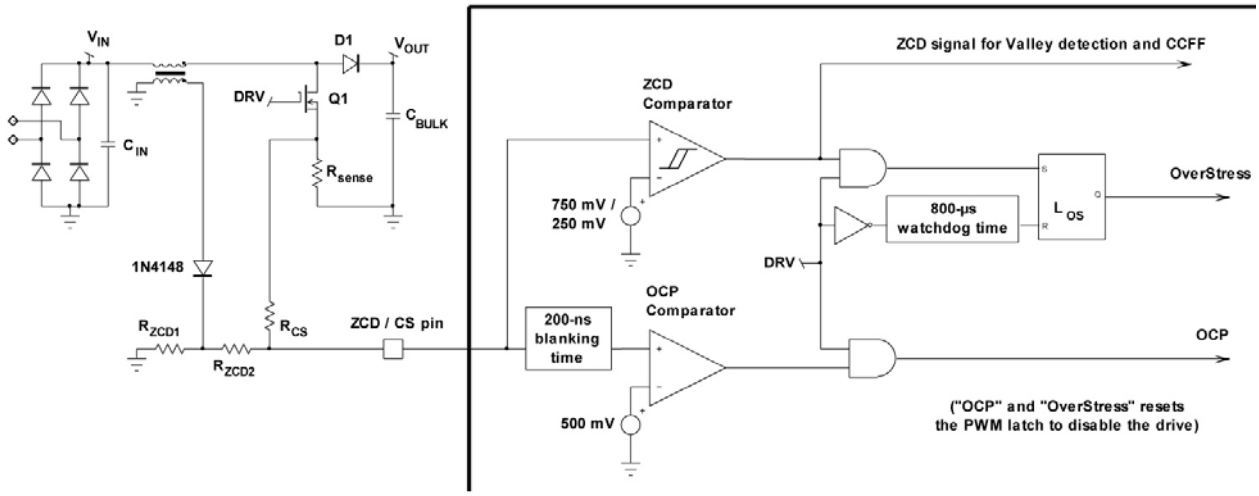


Figure 68. Current Sense and Zero Current Detection Blocks

Brown−Out Detection

The V_{SENSE} pin (pin2) receives a portion of the instantaneous input voltage (V_{in}). As V_{in} is a rectified sinusoid, the monitored signal varies between zero or a small voltage and a peak value.

For the brown−out block, we need to ensure that the line magnitude is high enough for operation. This is done as follows:

- The V_{SENSE} pin voltage is compared to a 1 V reference.
- If V_{pin2} exceeds 1 V, the input voltage is considered sufficient
- If V_{pin2} remains below 0.9 V for 50 ms, the circuit detects a brown−out situation (100 mV hysteresis).

By default, when the circuit starts operation, the circuit is in a fault state (“BO_NOK” high) until V_{pin2} exceeds 1 V.

When “BO_NOK” is high, the drive is not disabled. Instead, a 50 µA current source is applied to pin 1 to gradually reduce $V_{CONTROL}$. As a result, the circuit only stops pulsing when the staticOVP function is activated (that is when $V_{CONTROL}$ reaches the skip detection threshold). At that moment, the circuit turns off (see Figure 2). This method limits any risk of false triggering. The input of the PFC stage has some impedance that leads to some sag of the input voltage when the input current is large. If the PFC stage suddenly stops while a high current is drawn from the mains, the abrupt decay of the current may make the input voltage rise and the circuit detect a correct line level. Instead, the

gradual decrease of $V_{CONTROL}$ avoids a line current discontinuity and limits the risk of false triggering.

Pin2 is also used to sense the line for feed−forward. A similar method is used:

- The V_{SENSE} pin voltage is compared to a 2.2 V reference.
- If V_{pin2} exceeds 2.2 V, the circuit detects a high−line condition and the loop gain is divided by three (the internal PWM ramp slope is three times steeper)
- Once this occurs, if V_{pin2} remains below 1.7 V for 25 ms, the circuit detects a low−line situation (500 mV hysteresis).

At startup, the circuit is in low−line state (“LLine” high”) until V_{pin2} exceeds 2.2 V.

The line range detection circuit allows more optimal loop gain control for universal (wide input mains) applications.

As portrayed in Figure 69, the pin 2 voltage is also utilized to generate the current information required for the frequency fold−back function.

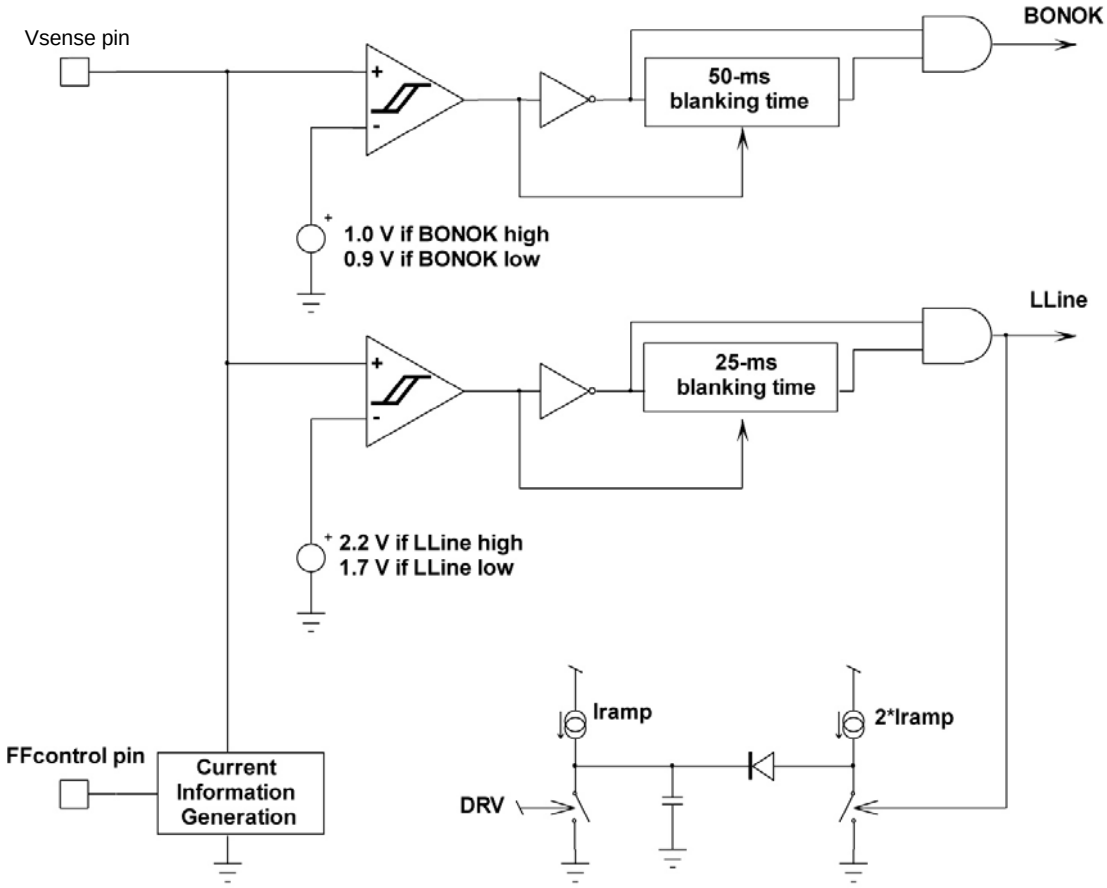


Figure 69. Input Line Sense Monitoring

Thermal Shutdown (TSD)

An internal thermal circuitry disables the circuit gate drive and keeps the power switch off when the junction temperature exceeds 150°C. The output stage is then enabled once the temperature drops below about 100°C (50°C hysteresis).

Output Drive Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. The gate drive is kept in a sinking mode whenever the Under−Voltage Lockout is active or more generally whenever the circuit is off (i.e., when the “Fault Latch” of the block diagram is high). Its high current capability (−500 mA/+800 mA) allows it to effectively drive high gate charge power MOSFET. As the circuit exhibits a large V_{CC} range (up to 35 V), the drive pin voltage is clamped not to provide the MOSFET gate with more than 14 V.

Reference Section

The circuit features an accurate internal 2.5 V reference voltage (V_{REF}) optimized to be ±2.4% accurate over the temperature range.

OFF Mode

As previously mentioned, the circuit turns off when one of the following faults is detected:

- Incorrect feeding of the circuit ("UVLO" high when $V_{CC} < V_{CC(off)}$, $V_{CC(off)}$ equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown.
- Under−Voltage Protection.
- Brown−Out Fault and static OVP (see block diagram)

Generally speaking, the circuit turns off when the conditions are not proper for desired operation. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized.

More specifically, when the circuit is in OFF state:

- The drive output is kept low
- All the blocks are off except:
  - The UVLO circuitry that keeps monitoring the V_{CC} voltage and controlling the start−up current source accordingly.
  - The TSD (thermal shutdown)
  - The Under−Voltage Protection ("UVP").
  - The brown−out circuitry
- $V_{CONTROL}$ is grounded so that when the fault is removed, the device starts−up under the soft start mode (B Version).
- The internal "pfcOK" signal is grounded.
- The output of the "V_{TON} processing block" is grounded

Failure detection

When manufacturing a power supply, elements can be accidentally shorted or improperly soldered. Such failures can also happen to occur later on because of the components fatigue or excessive stress, soldering defaults or external interactions. In particular, adjacent pins of controllers can be shorted, a pin can be grounded or badly connected. Such open/short situations are generally required not to cause fire, smoke nor big noise. The NCP1611 integrates functions that ease meet this requirement. Among them, we can list:

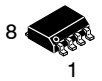
- Floating feedback pin
  A 250 nA sink current source pulls down the voltage on the feedback pin if it is floating so that the UVP protection trips and prevents the circuit from operating. This current source is small (450 nA maximum) so that its impact on the bulk voltage regulation level remains negligible with typical feedback resistor dividers.
- Fault of the GND connection
  If the GND pin is properly connected, the supply current drawn from the positive terminal of the V_{CC} capacitor, flows out of the GND pin to return to the negative terminal of the V_{CC} capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non connection of the GND pin can hence be detected by detecting that one of this ESD diode is conducting. Practically, the CS/ZCD ESD diode is monitored. If such a fault is detected for 200 μs, the circuit stops operating.
- Detection the CS/ZCD pin improper connection
  The CS/ZCD pin sources a 1 μA current to pull up the pin voltage and hence disable the part when the pin is floating. If the CS/ZCD pin is grounded, the circuit cannot monitor the ZCD signal and the 200 μs watchdog timer is activated. When the watchdog time has elapsed, the circuit sources a 250 μA current source to pull−up the CS/ZCD pin voltage. No drive pulse is initiated until the CS/ZCD pin voltage exceeds the ZCD 0.75 V threshold. Hence, if the pin is grounded, the circuit stops operating. Circuit proper operation requires the pin impedance to be 3.9 kΩ or more, the tolerance of the NCP1611 impedance testing function being considered over the −40°C to 125°C temperature range.
- Boost or bypass diode short
  The NCP1611 addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty−cycle operation until the fault is gone.

Refer to application note AND9064 available at http://www.onsemi.com/pub_link/Collateral/AND9064−D.PDF for more details.

ORDERING INFORMATION

Device	Circuit Version	Package	Shipping†
NCP1611ADR2G	NCP1611A	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1611BDR2G	NCP1611B		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

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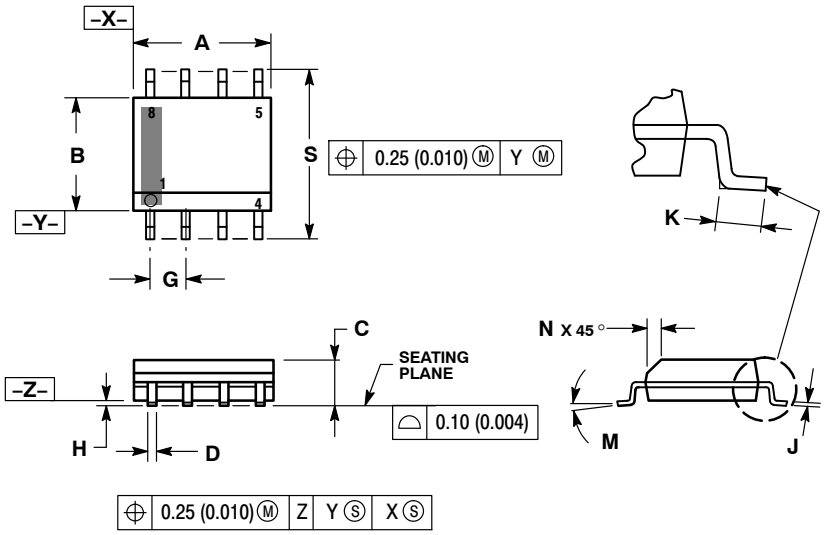
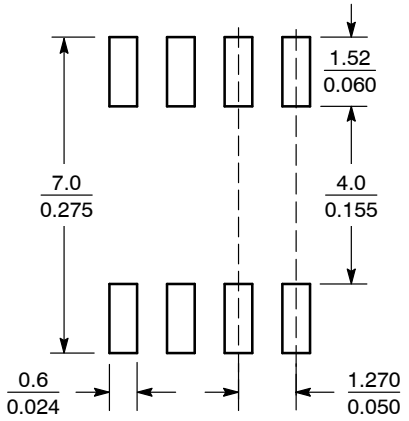


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

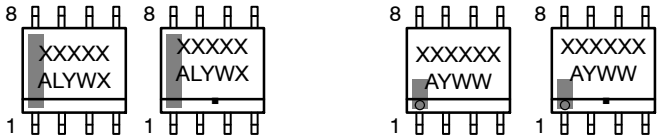
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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