NCP3418, NCP3418A

Dual Bootstrapped 12 V MOSFET Driver with Output Disable

The NCP3418 and NCP3418A are dual MOSFET gate drivers optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. Each of the drivers is capable of driving a 3000 pF load with a 25 ns propagation delay and a 20 ns transition time.

With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal, adaptive nonoverlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate VBST voltages as high as 30 V, with transient voltages as high as 35 V. Both gate outputs can be driven low by applying a low logic level to the Output Disable (OD) pin. An Undervoltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection. The NCP3418A is identical to the NCP3418 except that there is no internal charge pump diode.

The NCP3418 is pin−to−pin compatible with Analog Devices ADP3418 with the following advantages:

Features

- Faster Rise and Fall Times
- Internal Charge Pump Diode Reduces Cost and Parts Count
- Thermal Shutdown for System Protection
- Integrated OVP
- Internal Pulldown Resistor Suppresses Transient Turn On of Either MOSFET
- Anti Cross−Conduction Protection Circuitry
- Floating Top Driver Accommodates Boost Voltages of up to 30 V
- One Input Signal Controls Both the Upper and Lower Gate Outputs
- Output Disable Control Turns Off Both MOSFETs
- Complies with VRM 10.x Specifications
- Undervoltage Lockout
- Thermally Enhanced Package Available
- Pb−Free Packages are Available

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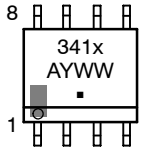
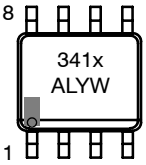
MARKING DIAGRAMS

SO−8
D SUFFIX
CASE 751

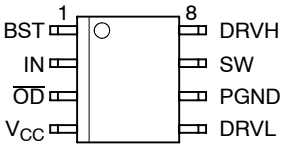


SO−8 EP
PD SUFFIX
CASE 751AC



341x	= Device Code x = 8 or 8A
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW, W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ORDERING INFORMATION

Device	Package	Shipping†
NCP3418D	SO−8	98 Units / Rail
NCP3418DR2	SO−8	2500 / Tape & Reel
NCP3418DR2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCP3418ADR2	SO−8	2500 / Tape & Reel
NCP3418ADR2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCP3418PDR2	SO−8 EP	2500 / Tape & Reel
NCP3418APDR2	SO−8 EP	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

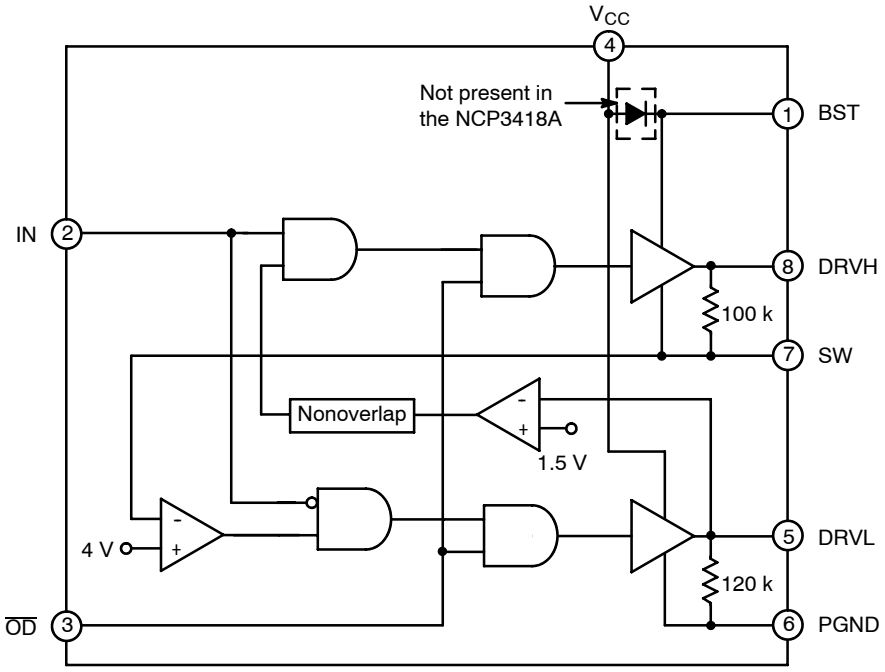


Figure 1. NCP3418/A Block Diagram

PIN DESCRIPTION

Pin	Symbol	Description
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and SW pins holds this bootstrap voltage for the high−side MOSFET as it is switched. The recommended capacitor value is between 100 nF and 1.0 μF. An external diode will be needed with the NCP3418A.
2	IN	Logic−Level Input. This pin has primary control of the drive outputs.
3	$\overline{OD}$	Output Disable. When low, normal operation is disabled forcing DRVH and DRVL low.
4	V_{CC}	Input Supply. A 1.0 μF ceramic capacitor should be connected from this pin to PGND.
5	DRVL	Output drive for the lower MOSFET.
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	SW	Switch Node. Connect to the source of the upper MOSFET.
8	DRVH	Output drive for the upper MOSFET.

MAXIMUM RATINGS

Rating		Value	Unit
Operating Ambient Temperature, T_A		0 to 85	°C
Operating Junction Temperature, T_J (Note 1)		0 to 150	°C
Package Thermal Resistance: SO−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$ (2−Layer Board)		 45 123	 °C/W °C/W
Package Thermal Resistance: SO−8 EP Junction−to−Ambient, $R_{\theta JA}$ (Note 2)		 50	 °C/W
Storage Temperature Range, T_S		−65 to 150	°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only)	Standard (Note 3) Lead Free (Note 4)	240 peak 260 peak	°C
JEDEC Moisture Sensitivity Level	SO−8 (240 peak profile) SO−8 (260 peak profile) SO−8 EP (240 peak profile) SO−8 EP (260 peak profile)	1 1 1 3	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Internally limited by thermal shutdown, 150°C min.
2. Rating applies when soldered to an appropriate thermal area on the PCB.
3. 60 − 180 seconds minimum above 183°C.
4. 60 − 180 seconds minimum above 237°C.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
V_{CC}	Main Supply Voltage Input	15 V	−0.3 V
BST	Bootstrap Supply Voltage Input	30 V wrt/PGND 35 V $\leq$ 50 ns wrt/PGND, 15 V wrt/SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	30 V	−1.0 V DC −10 V< 200 ns
DRVH	High−Side Driver Output	BST + 0.3 V 35 V $\leq$ 50 ns wrt/PGND, 15 V wrt/SW	−0.3 V wrt/SW
DRVL	Low−Side Driver Output	V_{CC} + 0.3 V	−0.3 V DC −2.0 V < 200 ns
IN	DRVH and DRVL Control Input	V_{CC} + 0.3 V	−0.3 V
$\overline{OD}$	Output Disable	V_{CC} + 0.3 V	−0.3 V
PGND	Ground	0 V	0 V

NOTE: All voltages are with respect to PGND except where noted.

NCP3418−SPECIFICATIONS (Note 5) (V_{CC} = 12 V, T_A = 0°C to +85°C, T_J = 0°C to +125°C unless otherwise noted.).

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range	−	V_{CC}	4.6	−	13.2	V
Supply Current	BST = 12 V, IN = 0 V	I_{SYS}	−	2.0	6.0	mA
$\overline{OD}$ INPUT						
Input Voltage High	−	−	2.0	−	−	V
Input Voltage Low	−	−	−	−	0.8	V
Input Current	−	−	−1.0	−	+1.0	μA
Propagation Delay Time (Note 6)	See Figure 2	$t_{pdl\overline{OD}}$ t_{pdhOD}	− −	40 40	60 60	ns ns
PWM INPUT						
Input Voltage High	−	−	2.0	−	−	V
Input Voltage Low	−	−	−	−	0.8	V
Input Current	−	−	−1.0	−	+1.0	μA
HIGH−SIDE DRIVER						
Output Resistance, Sourcing Current	V_{BST} − V_{SW} = 12 V (Note 8)	−	−	1.8	3.0	Ω
Output Resistance, Sinking Current	V_{BST} − V_{SW} = 12 V (Note 8)	−	−	1.0	2.5	Ω
Transition Times (Note 6)	V_{BST} − V_{SW} = 12 V, C_{LOAD} = 3.0 nF, See Figure 3	t_{rDRVH} t_{fDRVH}	− −	18 10	25 15	ns ns
Propagation Delay (Notes 6 & 7)	V_{BST} − V_{SW} = 12 V	$t_{pdhDRVH}$ $t_{pdlDRVH}$	− −	30 25	60 45	ns ns
LOW−SIDE DRIVER						
Output Resistance, Sourcing Current	−	V_{CC} = 12 V (Note 8)	−	1.8	3.0	Ω
Output Resistance, Sinking Current	−	V_{CC} − V_{SW} = 12 V (Note 8)	−	1.0	2.5	Ω
Transition Times	t_{rDRVL} t_{fDRVL}	C_{LOAD} = 3.0 nF, See Figure 3	− −	16 11	25 15	ns ns
Propagation Delay	$t_{pdhDRVL}$ $t_{pdlDRVL}$	See Figure 3	− −	30 20	60 30	ns ns
UNDERVOLTAGE LOCKOUT						
UVLO	−	−	3.9	4.3	4.6	V
Hysteresis	(Note 8)	−		0.5		V
THERMAL SHUTDOWN						
Over Temperature Protection	(Note 8)	−	150	170		°C
Hysteresis	(Note 8)			20		°C

5. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).
6. AC specifications are guaranteed by characterization, but not production tested.
7. For propagation delays, "t_{pdh}" refers to the specified signal going high; "t_{pdl}" refers to it going low.
8. GBD: Guaranteed by design; not tested in production. Specifications subject to change without notice.

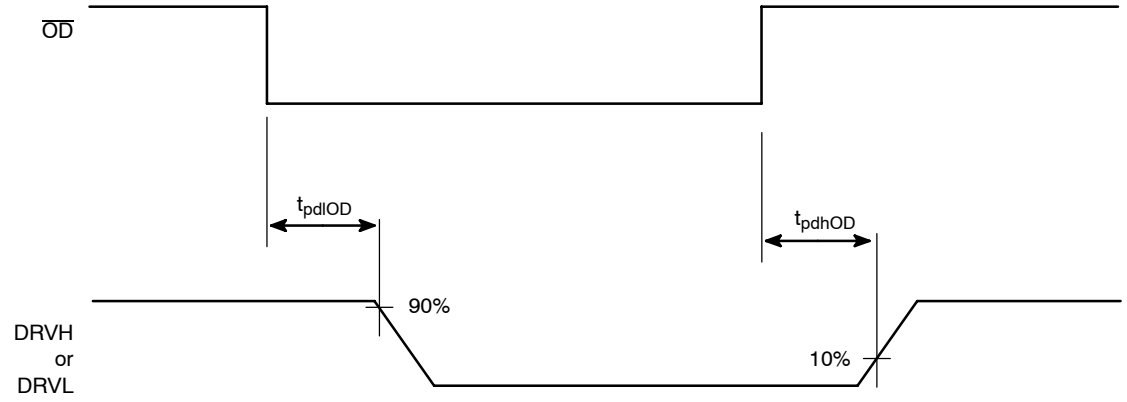


Figure 2. Output Disable Timing Diagram

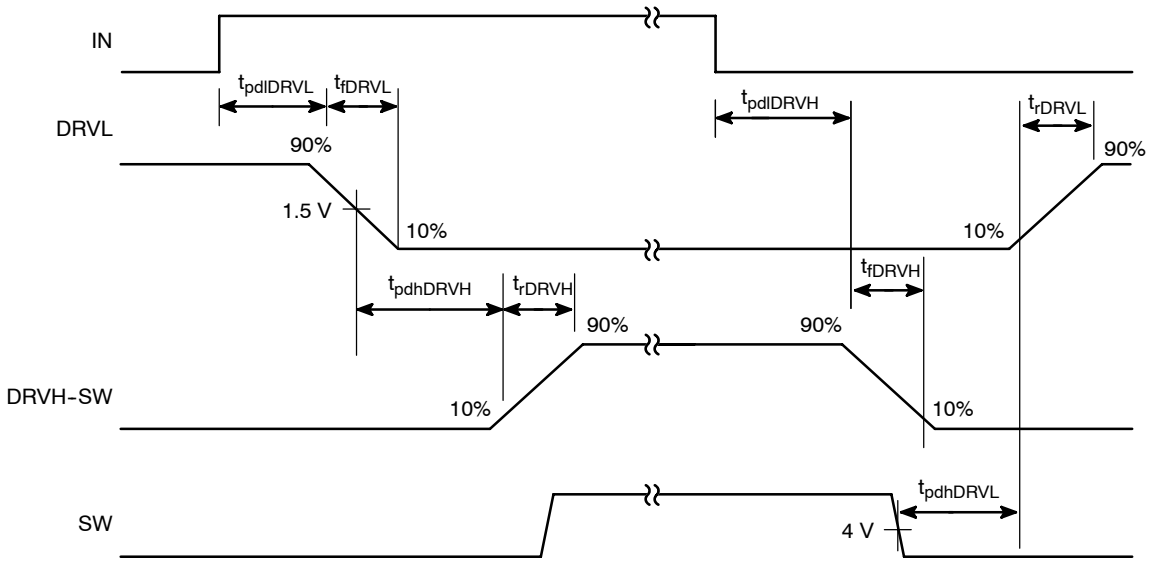


Figure 3. Nonoverlap Timing Diagram (timing is referenced to the 90% and 10% points unless otherwise noted)

APPLICATIONS INFORMATION

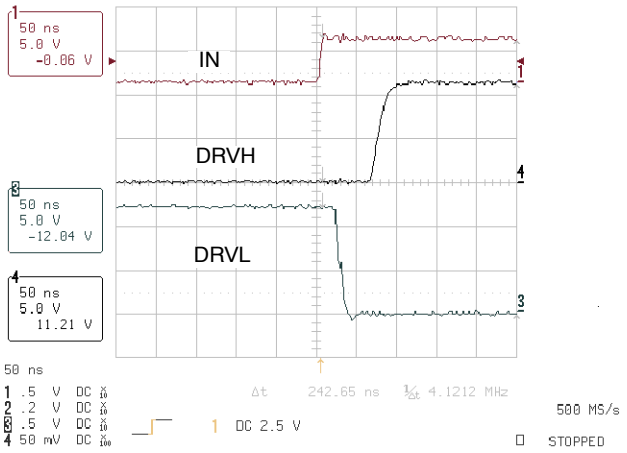


Figure 4. DRVH Rise and DRVL Fall Times

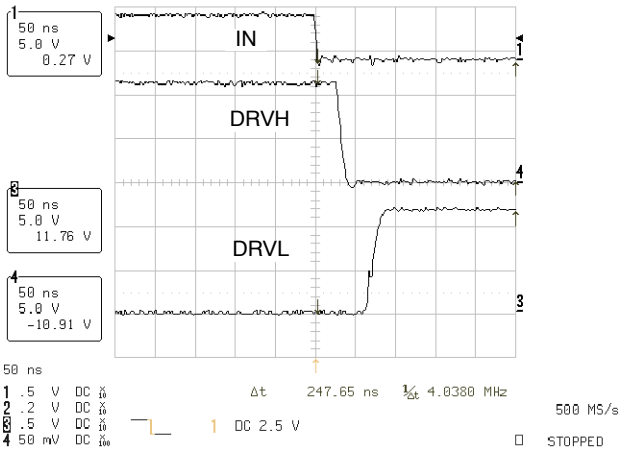


Figure 5. DRVH Fall and DRVL Rise Times

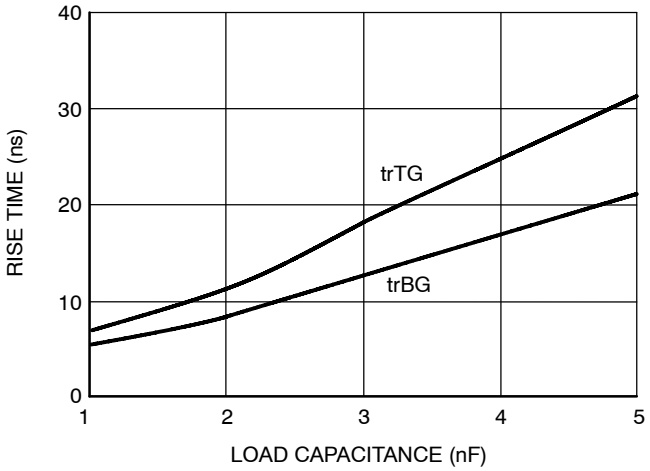


Figure 6. Rise Time vs. Load Capacitance

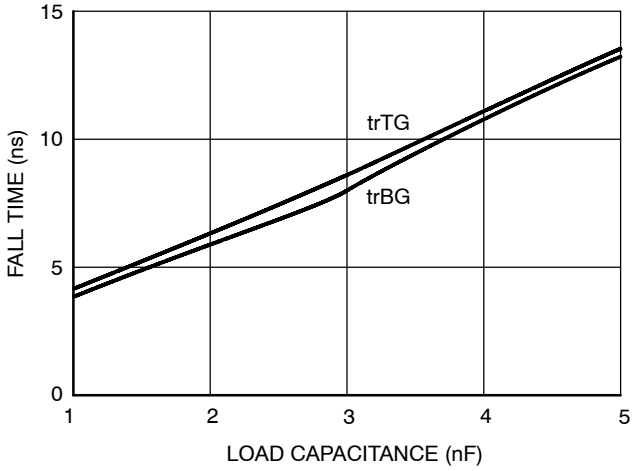


Figure 7. Fall Time vs. Load Capacitance

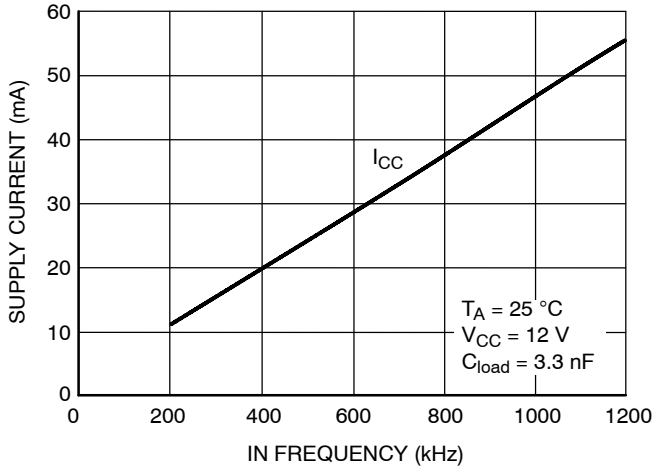


Figure 8. V_{CC} Supply Current vs. IN Frequency

APPLICATIONS INFORMATION

Theory of Operation

The NCP3418 and NCP3418A are single phase MOSFET drivers optimized for driving two N−channel MOSFETs in a synchronous buck converter topology. The NCP3418 features an internal diode, while the NCP3418A requires an external BST diode for the floating top gate driver. A single PWM input signal is all that is required to properly drive the high−side and the low−side MOSFETs. Each driver is capable of driving a 3.3 nF load at frequencies up to 500 kHz.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to the V_{CC} supply and PGND.

When the NCP3418 is enabled, the low−side driver's output is 180° out of phase with the PWM input. When the device is disabled, the low−side gate is held low.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The bias voltage for the high side driver is developed by a bootstrap circuit referenced to SW. The bootstrap capacitor should be connected between the BST and SW pins.

The bootstrap circuit comprises an internal or external diode, D1 (in which the anode is connected to V_{CC}), and an external bootstrap capacitor, C_{BST}. When the NCP3418 is starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to V_{CC} through D1. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET by pulling charge out of C_{BST}. As the high−side MOSFET turns on, the SW pin will rise to V_{IN}, forcing the BST pin to V_{IN} + V_{CC}, which is enough gate−to−source voltage to hold the MOSFET on. To complete the cycle, the high−side MOSFET is switched off by pulling the gate down to the voltage at the SW pin. When low−side MOSFET turns on, the SW pin is held at ground. This allows the bootstrap capacitor to charge up to V_{CC} again.

The high−side driver's output is in phase with the PWM input. When the device is disabled, the high side gate is held low.

Safety Timer and Overlap Protection Circuit

The overlap protection circuit prevents both the high−side MOSFET and the low−side MOSFET from being on at the same time, and minimizes the associated off times. This will reduce power losses in the switching elements. The overlap protection circuit accomplishes this by controlling the delay from turning off the high−side MOSFET to turning on the low−side MOSFET.

To prevent cross conduction during the high−side MOSFET's turn−off and the low−side MOSFET's turn−on, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, DRVH will go low after a propagation delay ($t_{pdlDRVH}$), turning the high−side MOSFET off. However, before the low−side MOSFET can turn on, the overlap protection circuit waits for the voltage at the SW pin to fall below 4.0 V. Once SW falls below the 4.0 V threshold, DRVL will go high after a propagation delay ($t_{pdhDRVL}$), turning the low−side MOSFET on. However, if SW does not fall below 4.0 V in 300 ns, the safety timer circuit will override the normal control scheme and drive DRVL high. This will help insure that if the high−side MOSFET fails to turn off it will not produce an over−voltage at the output.

Similarly, to prevent cross conduction during the low−side MOSFET's turn−off and the high−side MOSFET's turn−on, the overlap circuit monitors the voltage at the gate of the low−side MOSFET through the DRVL pin. When the PWM signal goes high, DRVL will go low after a propagation delay ($t_{pdlDRVL}$), turning the low−side MOSFET off. However, before the high−side MOSFET can turn on, the overlap protection circuit waits for the voltage at DRVL to drop below 1.5 V. Once this has occurred, DRVH will go high after a propagation delay ($t_{pdhDRVH}$), turning the high−side MOSFET on.

Application Information

Supply Capacitor Selection

For the supply input (V_{CC}) of the NCP3418, a local bypass capacitor is recommended to reduce noise and supply peak currents during operation. Use a 1.0 to 4.7 μF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Keep the ceramic capacitor as close as possible to the V_{CC} and PGND pins.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal (or an external) diode. Selection of these components can be done after the high−side MOSFET has been chosen.

The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}} \qquad \text{(eq. 1)}$$

where Q_{GATE} is the total gate charge of the high−side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high−side MOSFET drive. For example, a NTD60N03 has a total gate charge of about 30 nC. For an allowed droop of 300 mV, the required bootstrap capacitance is 100 nF. A good quality ceramic capacitor should be used.

If an external Schottky diode will be used for bootstrap, it must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on SW. The average forward current can be estimated by:

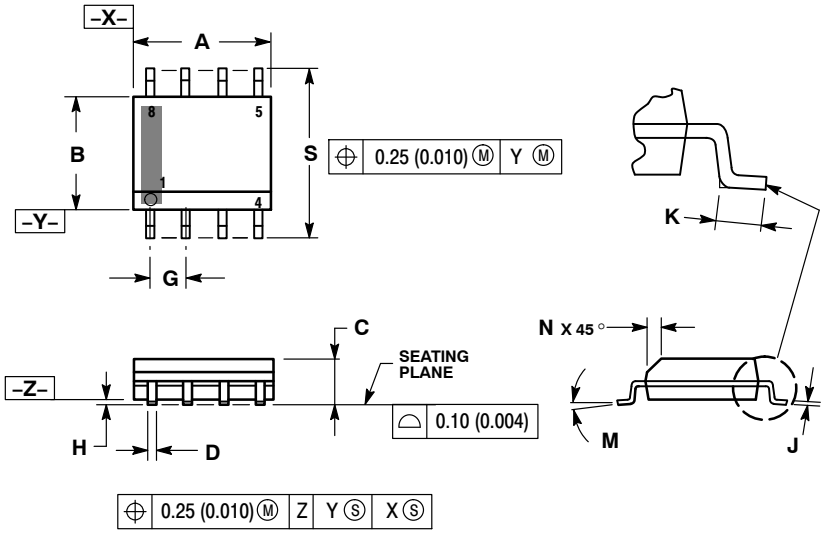
$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \qquad \text{(eq. 2)}$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in−circuit, since this is dependent on the source impedance of the 12 V supply and the ESR of C_{BST}.

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

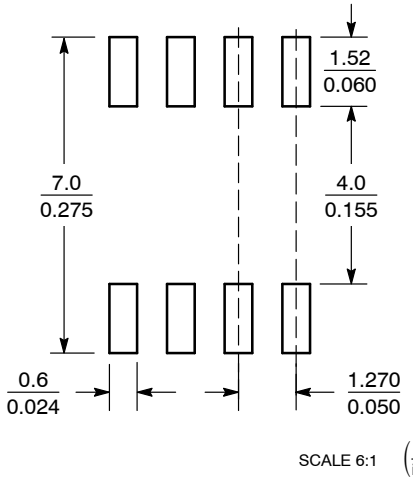
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

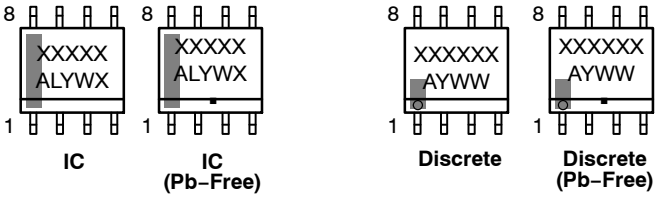
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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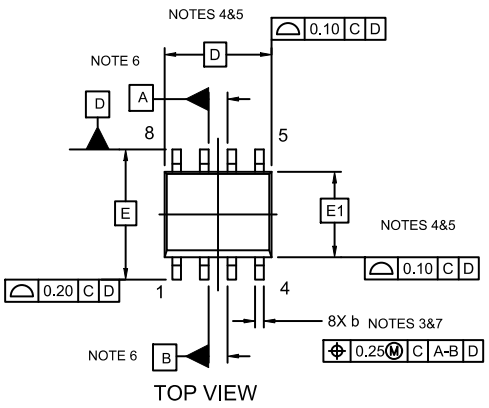
SCALE 1:1

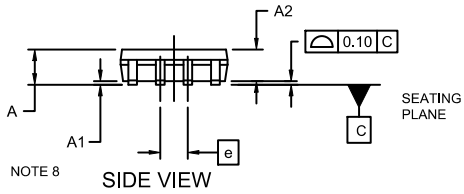
SOIC−8 EP
CASE 751AC
ISSUE E

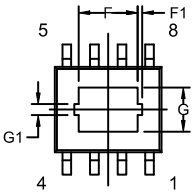
DATE 05 OCT 2022

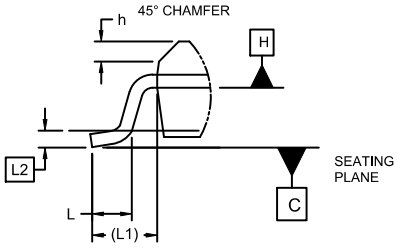
NOTES:

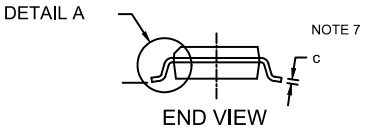
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

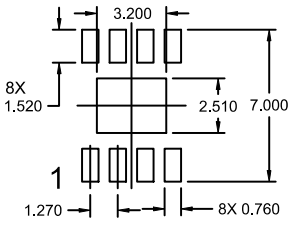








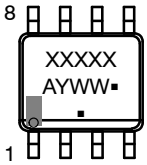




DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1		0.20 REF	
G	1.55	2.03	2.51
G1		0.46 REF	
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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