3 Amp V_{TT} Termination Source / Sink Regulator for DDR, DDR-2, DDR-3, DDR-4

NCP51510, NCV51510

The NCP51510 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low−noise systems where space is a key consideration. The NCP51510 maintains a fast transient response and only requires a minimum V_{TT} load capacitance of 10 μF for output stability. The NCP51510 supports remote sensing and all power requirements for DDR V_{TT} bus termination. The NCP51510 can also be used in low−power chipsets and graphics processor cores that require dynamically adjustable output voltages. The NCP51510 is available in the thermally−efficient DFN10 Exposed Pad package, and is rated both Green and Pb−Free.

Features

- Generate DDR Memory Termination Voltage (V_{TT})
- For DDR, DDR−2, DDR−3 and DDR−4 Source / Sink Currents
- Supports Loads Up to ±3 A (Typ), Output is Over−Current Protected
- Integrated MOSFETs with Thermal Shutdown Protection
- Fast Load−Transient Response
- P_{GOOD} Output Pin to Monitor Status of V_{TT} Output Regulation
- $\overline{SS}$ Input Pin for Suspend Shutdown mode
- V_{RI} Input Reference for Flexible Voltage Tracking
- V_{TTS} Input for Remote Sensing (Kelvin Connection)
- Built−in Soft−Start, Under Voltage Lockout
- Small, Low−Profile 10−pin, 3 x 3 mm DFN Package
- NCV51510MWTAG − Wettable Flank Option for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- This is a Pb−Free Device

Applications

- DDR Memory Termination
- Desktop PC's, Notebooks, and Workstations
- Servers and Networking equipment
- Telecom/Datacom, GSM Base Station
- Graphics Processor Core Supplies
- Set Top Boxes, LCD−TV/PDP−TV, Copier/Printers
- Supplies Power for Chipset/RAM as Low as 0.5 V
- Active Source/Sink Bus Termination

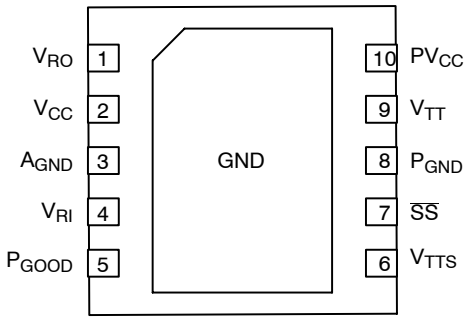
DFN10
CASE 485C

MARKING DIAGRAM

51510	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP51510MNTAG	DFN10 (Pb−Free)	3000 / Tape & Reel
NCV51510MNTAG*	DFN10 (Pb−Free)	3000 / Tape & Reel

DISCONTINUED (Note 1)

NCV51510MWTAG*	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V_{RO}	OUTPUT – Buffered Output of V_{RI} Reference Input pin.
2	V_{CC}	INPUT – Regulator Analog Power Input pin. Connect to the system supply voltage. Bypass V_{CC} to A_{GND} with a 1 μF or greater ceramic capacitor.
3	A_{GND}	Analog Ground
4	V_{RI}	INPUT – External Reference Input for V_{TT} Output (see Figure 1 for typical application)
5	P_{GOOD}	OUTPUT – V_{TT} "Power Good" pin (open drain output)
6	V_{TTS}	INPUT – Remote Sense Input for V_{TT}. The V_{TTS} pin provides accurate remote feedback sensing of the V_{TT} output.
7	$\overline{SS}$	INPUT – Suspend Shutdown Control Input. CMOS compatible. Logic HIGH = enable, logic LOW = shutdown. Connect to VDDQ for normal operation.
8	P_{GND}	Power Ground. Internally connected to Low−side MOSFET
9	V_{TT}	OUTPUT – Regulated Power Output pin
10	PV_{CC}	INPUT – Regulator Power Input pin. Internally connected to High−side MOSFET
–	THERMAL PAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
PV_{CC} to P_{GND}	(Note 2)	–	−0.3 to 4.3	V
V_{CC} to A_{GND}	(Note 2)	V_{CC}	−0.3 to 4.3	
V_{RI}, V_{RO}, $\overline{SS}$, P_{GOOD} to A_{GND}	(Note 2)	–	−0.3 to (V_{CC} + 0.3)	
V_{TT} to P_{GND}	(Note 2)	–	−0.3 to (PV_{CC} + 0.3)	
V_{TTS} to A_{GND}	(Note 2)	V_{TTS}	−0.3 to (PV_{CC} + 0.3)	
P_{GND} to A_{GND}		P_{GND}	−0.3 to +0.3	
Storage Temperature		T_{stg}	−65 to 150	°C
Operating Junction Temperature Range		T_J	−40 to 125	
ESD Capability, Human Body Model	(Note 3)	ESD_{HBM}	2000	V
ESD Capability, Machine Model	(Note 3)	ESD_{MM}	200	V
V_{TT} Output Continuous RMS Current	100 sec	–	±1.6	A
	1 sec		±2.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

DISSIPATION RATINGS

Package	T_A =70°C Power Rate	Derating Factor Above T_A = 70°C
10−Pin DFN	1951 mW	24.4 mW / °C

RECOMMENED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
V_{TT} Output Voltage Range	V_{TT}, V_{TTS}	0.5 to 1.5	V
PV_{CC} Input Voltage Range (Power)	PV_{CC}	1.1 to 3.6	
V_{CC} Input Voltage Range (Analog)	V_{CC}	2.7 to 3.6	
Logic Voltage Range	$\overline{SS}$, P_{GOOD}	0 to V_{CC}	
Operating Ambient Temperature Range	T_A	−40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

PV_{CC} = 1.8 V; V_{CC} = 3.3 V; V_{RI} = V_{TTS} = 1.25 V; $\overline{SS}$ = V_{CC}; (circuit of Figure 1, −40°C ≤ (T_J = T_A) ≤ 125°C; unless otherwise noted. Typical values are at T_A = +25°C

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT						
V_{TT} Output Voltage Range	PV_{CC} > (V_{TT} + $V_{DROPOUT}$)	V_{TT}	0.5		1.5	V
V_{TT} Load Regulation	−1 A ≤ I_{TT} ≤ +1 A	ΔV_{LOAD}	−4		+4	mV
V_{TT} Line−Regulation	1.4 V ≤ PV_{CC} ≤ 3.3 V, I_{OUT} = ±100 mA	ΔV_{LINE}		1		
Feedback−Voltage Error	V_{RI} to V_{TTS}, I_{TT} = ±200 mA; T_A = −40°C to 125°C	V_{TTS}	−17		+17	
V_{TT} Current Slew Rate	C_{OUT} = 100 μF, I_{TT} = 0.1 A to 2 A	I_{TT} di/dt		3		A/μs
V_{TT} Output Power−Supply Rejection Ratio	10 Hz < f < 10 kHz, I_{TT} = 200 mA, C_{OUT} = 100 μF	PSRR		80		dB
V_{TT} Output MOSFET $R_{DS(on)}$	High−side (source) (I_{TT} = +100 mA)	$R_{DS(on)}$		140	250	mΩ
	Low−side (sink) (I_{TT} = −100 mA)			140	250	
V_{TT} Output−to−V_{TTS} Input	Internal Feedback Resistance	R_{FB}		12		kΩ
Discharge MOSFET $R_{DS(on)}$	$\overline{SS}$ = 0 V	R_{DIS}		8		Ω
SUPPLY CURRENT						
Quiescent PV_{CC} Current	No Load	I_{PVCC}		0.4	10	mA
Quiescent V_{CC} Current	V_{RI} > 0.45 V, No Load	I_{CC}		0.7	1.3	
Shutdown PV_{CC} Current	$\overline{SS}$ = 0 V	$I_{PVCC\ SD}$		0.1	10	μA
Shutdown V_{CC} Current	$\overline{SS}$ = 0V, V_{RI} = 0 V	$I_{CC\ SD}$		50	100	
	$\overline{SS}$ = 0V, V_{RI} > 0.45 V			350	600	
REFERENCE						
V_{RI} Input Voltage Range		V_{RI}	0.5		1.5	V
V_{RI} Input−Bias current	T_A = +25°C	I_{RI}	−1		+1	μA
V_{RO} Output Voltage	V_{CC} = 3.3 V, I_{RO} = 0	V_{RO}	V_{RI} −10	V_{RI}	V_{RI} +10	mV
V_{RO} Load Regulation	I_{RO} = ±5 mA	ΔV_{RO}	−20		+20	
SUSPEND SHUTDOWN						
$\overline{SS}$ − Suspend Shutdown Logic Input Threshold	$\overline{SS}$ Logic HI (V_{TT} Output Enabled)	V_{IH}	2.0			V
	$\overline{SS}$ Logic LOW (V_{TT} Suspended)	V_{IL}			0.8	
$\overline{SS}$ − Logic Input Current	$\overline{SS}$ = V_{CC} or 0 V, T_A = +25°C	I_{SS}	−1		+1	μA
FAULT CONDITION − CURRENT LIMIT						
Current−Limit Threshold	T_A = −40°C to +125°C	$I_{TT\ LIMIT}$	1.8	3	4.2	A
Soft−start Current−limit time		T_{SS}		200		μs

ELECTRICAL CHARACTERISTICS

PV_{CC} = 1.8 V; V_{CC} = 3.3 V; V_{RI} = V_{TTS} = 1.25 V; $\overline{SS}$ = V_{CC}; (circuit of Figure 1, −40°C ≤ (T_J = T_A) ≤ 125°C; unless otherwise noted. Typical values are at T_A = +25°C (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
FAULT CONDITION − UNDER−VOLTAGE LOCKOUT						
V_{CC} UVLO Threshold	Wake−up, rising edge	$V_{CC\ UVLO}$	2.50	2.70	2.90	V
	Hysteresis Voltage	−		100		mV
PV_{CC} UVLO Threshold	Wake−up, rising edge	$PV_{CC\ UVLO}$		0.9	1.1	V
	Hysteresis Voltage	−		55		mV
V_{RI} UVLO Voltage	V_{RI}, rising edge	$V_{RI\ UVLO}$		350	450	
	Hysteresis Voltage	−		50		
FAULT CONDITION − THERMAL SHUTDOWN						
Thermal Shutdown Temperature	Thermal Shutdown, rising edge	T_{SD}		165		°C
Thermal Shutdown Hysteresis	Hysteresis Temperature	T_{SH}		15		
FAULT CONDITION − POWER GOOD						
P_{GOOD} Lower trip threshold	With respect to feedback threshold, hysteresis = 12 mV	−	−200	−150	−100	mV
P_{GOOD} Upper trip threshold		−	100	150	200	
P_{GOOD} Output Low Voltage	I_{SINK} = 4 mA (P_{GOOD} MOSFET = On)	−			300	
P_{GOOD} start−up delay	Start−up rising edge, V_{TTS} within ±100 mV of the feedback threshold	−	1	2	3.5	ms
P_{GOOD} Propagation Delay	V_{TTS} forced 25 mV beyond P_{GOOD} trip threshold	T_{PGOOD}	5	10	35	μs
P_{GOOD} Leakage Current	V_{TTS} = V_{RI} (P_{GOOD} Hi−impedance), P_{GOOD} = V_{CC} + 0.3 V, T_A = +25°C	I_{PGOOD}			1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

General*

The NCP51510 is a source/sink tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51510 integrates a high−performance, low−dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing input (V_{TTS}) should be connected to the positive terminal of the output capacitors as a separate trace from the high current path of the V_{TT} output.

Generation of Internal Voltage Reference

The V_{TT} output voltage is regulated to (and tracks with) the voltage on the V_{RI} Reference input. When the V_{RI} input is configured for standard DDR termination applications, the V_{RI} Reference input can be set by an external equivalent ratio voltage divider connected to the memory supply bus (V_{DDQ}). The NCP51510 supports V_{TT} voltages from 0.5 V to 1.5 V.

Generation of Internal Voltage Reference (cont)

When the V_{RO} output is configured for DDR termination applications, it provides a separate V_{TT} output reference voltage for the memory application. The V_{RO} Reference Output pin is a buffered version of the V_{RI} Reference Input, and is capable of sourcing and sinking a load of ±5 mA. The V_{RO} output becomes active when the V_{RI} input > 0.45 V and the V_{CC} power rail is above the UVLO threshold. The V_{RO} Reference Output is independent of the $\overline{SS}$ pin (Suspend Shutdown) state.

Fault Detection and Shutdown Function

When the $\overline{SS}$ “Suspend Shutdown” input pin is driven high, the NCP51510 regulator begins normal operation, with the Soft Start circuit gradually increasing output current during the first 200 μs in order to reduce the input surge currents at startup, with full current available after the 200 μs Soft−Start circuitry has timed out.

When the $\overline{SS}$ input is driven low, the V_{TT} output is discharged to P_{GND} through an internal 8 Ω MOSFET. The V_{RO} output remains on when the $\overline{SS}$ input is driven low. The NCP51510 provides an open−drain P_{GOOD} “Power Good” output that goes high when the V_{TTS} Sense input is within ±150 mV of the V_{RI} Reference Input. The P_{GOOD} output de−asserts within 10 μs after the V_{TTS} Sense input exceeds the size of the P_{GOOD} window. During initial V_{TT} startup, P_{GOOD} asserts high 2 ms after the V_{TTS} Sense input enters P_{GOOD} window. Because the P_{GOOD} output is open−drain, an external pull−up resistor is required (100 kΩ*) between P_{GOOD} and a stable active supply voltage rail.

Thermal Shutdown with Hysteresis

If the NCP51510 is to operate in elevated temperatures for long durations, care should be taken to ensure that the maximum operating junction temperature is not exceeded. To guarantee safe operation, the NCP51510 provides on−chip thermal shutdown protection. When the chip junction temperature exceeds 165°C*, the part will shutdown. When the junction temperature falls back, to 150°C*, the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold, the V_{TT} output is shut off, discharged by the 8 Ω internal discharge MOSFET.

Output Capacitor

Output stability is guaranteed for V_{TT} output capacitance C_{OUT} from 10 μF to 220 μF. The ESR of C_{OUT} between 2 mΩ and 50 mΩ is required to maintain stability. Use the formula below to calculate the application’s transient response:

$$\Delta I_{TT(pp)} \times ESR = \Delta V_{TT(pp)}$$

Where:
$\Delta I_{TT(pp)}$ is the maximum peak−to−peak load current delta and $\Delta V_{TT(pp)}$ is the allowable peak−to−peak voltage tolerance.

*Typical values are used with the application description text. Please refer to the Electrical Specifications Table for a more detailed list of MIN, MAX and TYPICAL values.

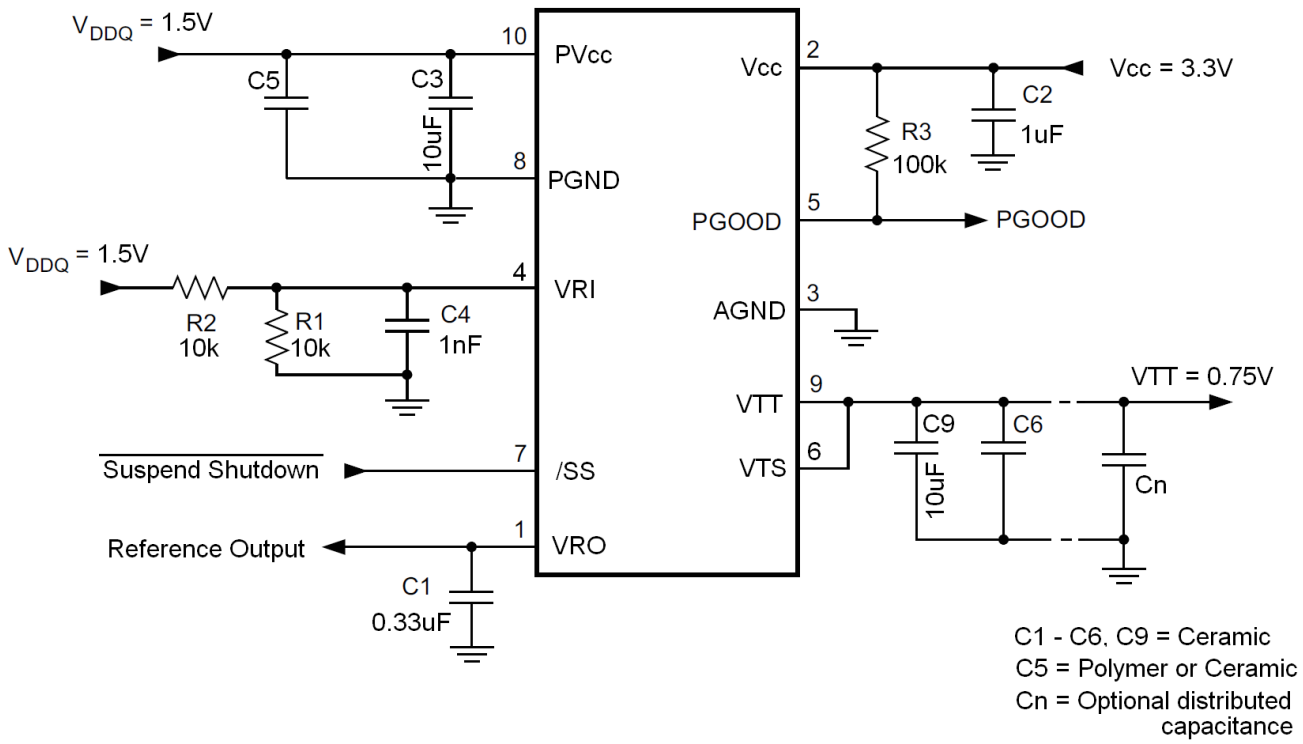
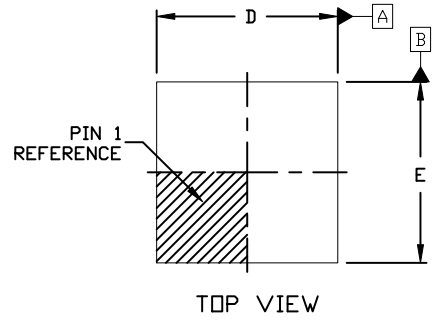


Figure 1. Standard Application Schematic for NCP51510

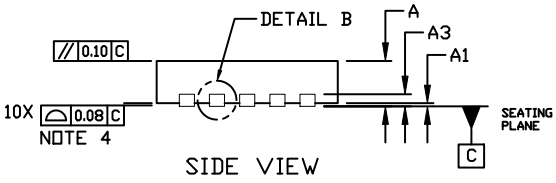
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

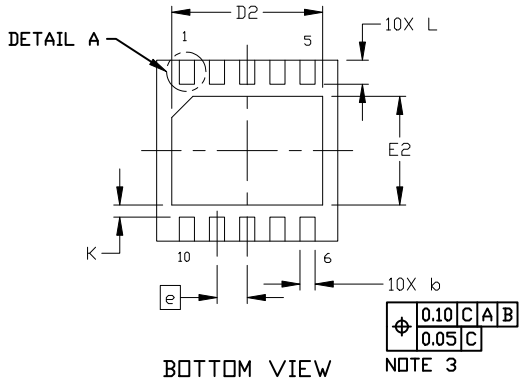
SCALE 2:1



TOP VIEW

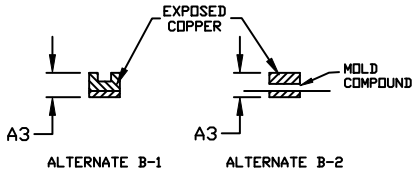


SIDE VIEW

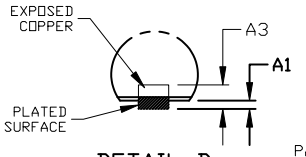


BOTTOM VIEW

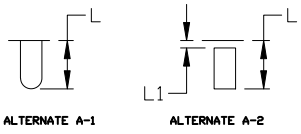
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

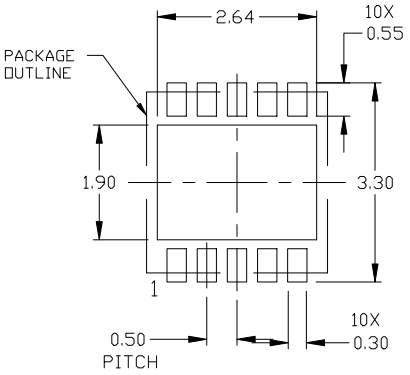


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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