Linear Regulator - Wide Input Voltage Range, Ultra-Low Iq, High PSRR, Adjustable Output Voltage
5 mA

NCP786L

ON Semiconductor®

www.onsemi.com

The NCP786L is high−performance linear regulator, offering a very wide operating input voltage range of up to 450 V DC, with an output current of up to 5 mA. Ideal for high input voltage applications such as industrial and home metering, home appliances. The NCP786L family offers ±5% initial accuracy, extremely high−power supply rejection ratio and ultra−low quiescent current. The NCP786L family is optimized for high−voltage line and load transients, making them ideal for harsh environment applications. The output voltage can be set by resistor divider in range from 1.27 V up to 15 V. SOT−223 Pb−free package with high allowable power dissipation keep small footprint at space sensitive applications.

Features

- Wide Input Voltage Range:
  DC: Up to 450 V
  AC: 85 V to 260 V (half−wave rectifier and 2.2 μF capacitor)
- 5 mA Guaranteed Output Current
- Ultra Low Quiescent Current: Typ. 10 μA ($V_{OUT} \le 15$ V)
- ±5% Accuracy Over Full Load, Line and Temperature Variations
- Ultra−high PSRR: 70 dB at 60 Hz, 90 dB at 100 kHz
- Stable with Ceramic Output Capacitor 2.2 μF MLCC
- Thermal Shutdown and Current Limit Protection
- Available in Thermally Enhanced SOT−223 Package
- This is a Pb−Free Device

Typical Applications

- Industrial Applications, Home Appliances
- Home Metering / Network Application
- Off−line Power Supplies

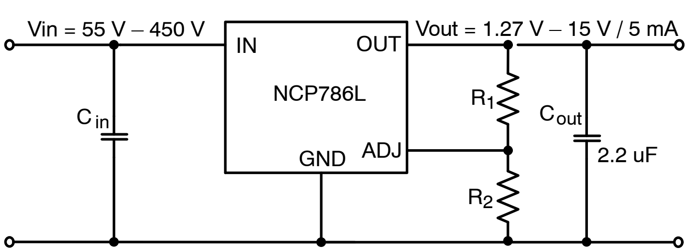
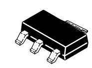
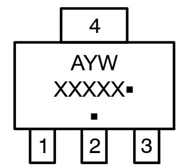


Figure 1. Typical Applications

MARKING DIAGRAM



SOT−223
S SUFFIX
CASE 318E



(Top View)

A	= Assembly Location
Y	= Year
W	= Work Week
XXXXX	= Specific Device Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

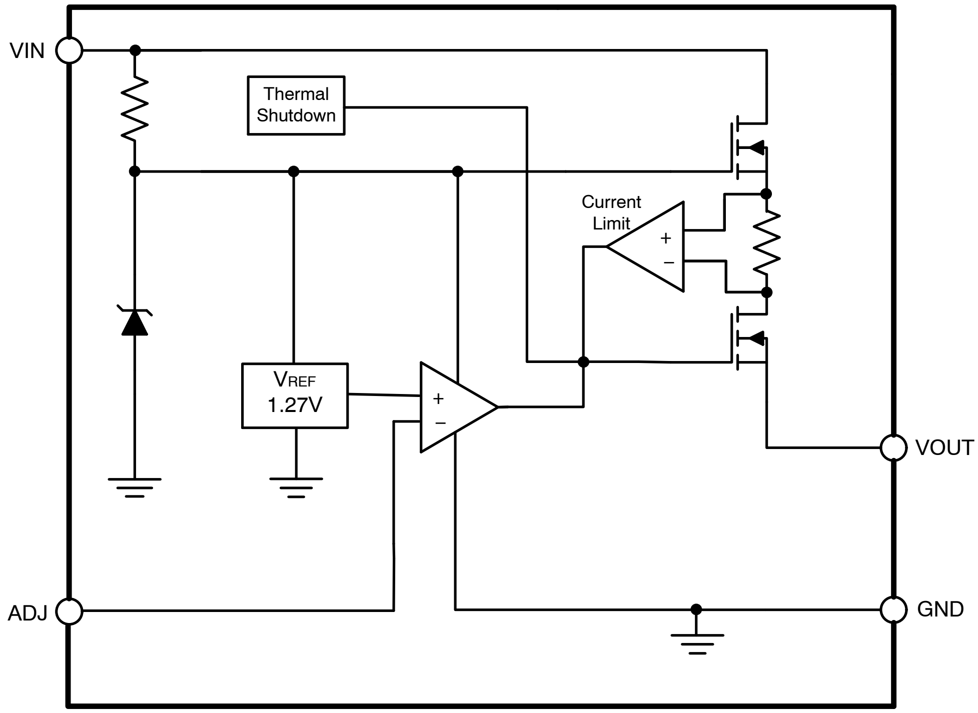


Figure 2. Simplified Internal Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. (SOT−223)	Pin Name	Description
1	VIN	Supply Voltage Input. Connect 1 μF or 2.2 μF capacitor from VIN to GND.
2	ADJ	ADJ pin for output voltage setting via resistors divider.
3	VOUT	Regulator Output. Connect 2.2 μF or higher MLCC capacitor from VOUT to GND.
4 (Tab)	GND	Ground connection.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 700	V
Output Voltage	V_{OUT}	−0.3 to 18	V
Enable Pin Voltage	V_{EN}	−0.3 to 5.5	V
Maximum Junction Temperature	$T_{J(MAX)}$	125	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (All pins except HV pin no.1) (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Peak 650 V max 1 ms non repeated for 1 s
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch−up Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT−223 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	73	°C/W

Table 4. ELECTRICAL CHARACTERISTICS NCP786L Adj. $-40°C \le T_J \le 85°C$; V_{IN} = 340 V; I_{OUT} = 100 μA, C_{IN} = 2.2 μF, C_{OUT} = 10 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 3)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage DC			V_{IN}	55		450	V
Maximum output voltage	$-40°C \le T_J \le 85°C$, Iout = 100 μA, 55 V ≤ Vin ≤ 450 V		Voutmax		15		V
Reference Voltage Accuracy	T_J = 25°C, Iout = 100 μA, 55 V ≤ Vin ≤ 450 V		V_{REF}	−3%	1.275	+3%	V
	$-40°C \le T_J \le 85°C$, Iout = 100 μA, 55 V ≤ Vin ≤ 450 V		V_{REF}	−5%	1.275	+5%	V
Line Regulation	V_{IN} = 55 V to 450 V, Iout = 100 μA		Reg_{LINE}	−0.5	0.1	+0.5	%
Load Regulation	0.1 mA ≤ I_{OUT} ≤ 5 mA, Vin = 55 V		Reg_{LOAD}	−1.0	0.66	+1.0	%
Maximum Output Current	55 V ≤ Vin ≤ 450 V, (Note 4)		I_{OUT}	6			mA
Quiescent Current	I_{OUT} = 0, 55 V ≤ Vin ≤ 450 V		I_{GND}		10	15	μA
Ground current	55 V ≤ Vin ≤ 450 V, (Note 4) 0 < I_{OUT} ≤ 5 mA					25	μA
ADJ Pin current					150		nA
Power Supply Rejection Ratio	Vin = 340 VDC +1 Vpp modulation, Iout = 100 μA	f = 1 kHz	PSRR		65		dB
Noise (Note 5)	f = 10 Hz to 100 kHz Vin = 340 VDC, Iout = 1 mA, V_{OUT} = 1.27 V, C_{OUT} = 2.2 μF		V_{NOISE}		146		μVrms
Thermal Shutdown Temperature (Note 5)	Temperature increasing from T_J = +25°C		T_{SD}		145		°C
Thermal Shutdown Hysteresis (Note 5)	Temperature falling from T_{SD}		T_{SDH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
4. Respect to Safe Operating Area
5. Guaranteed by design

TYPICAL CHARACTERISTICS

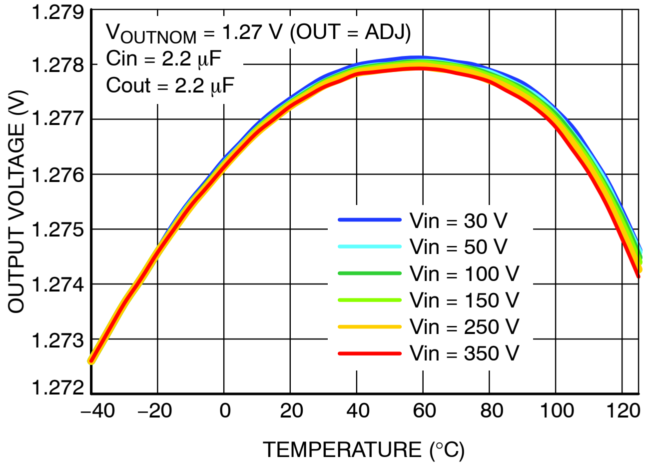


Figure 3. Output Voltage vs. Temperature

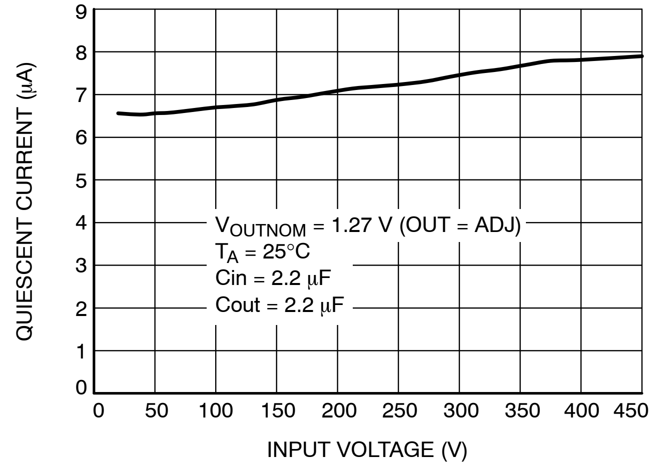


Figure 4. Quiescent Current vs. Input Voltage

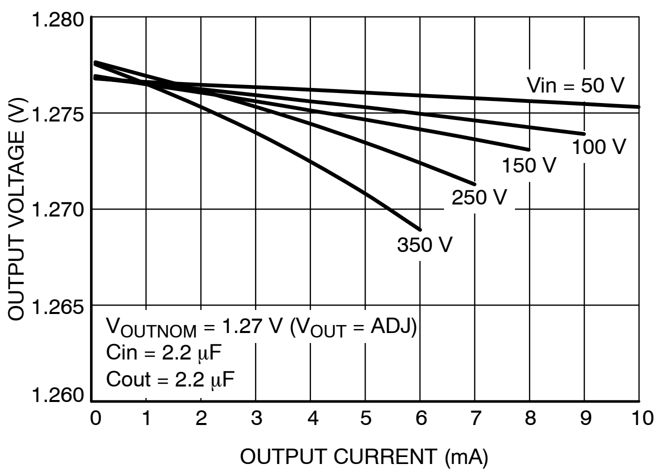


Figure 5. Output Voltage vs. Output Current

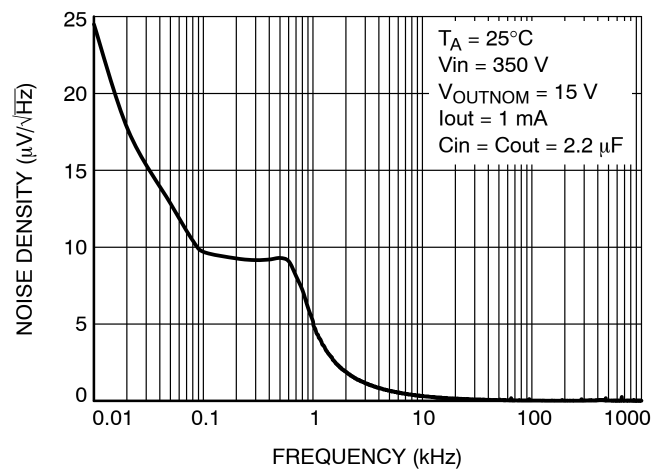


Figure 6. Output Voltage Noise Density vs. Frequency

APPLICATION INFORMATION

The typical application circuit for the NCP786L device is shown below.

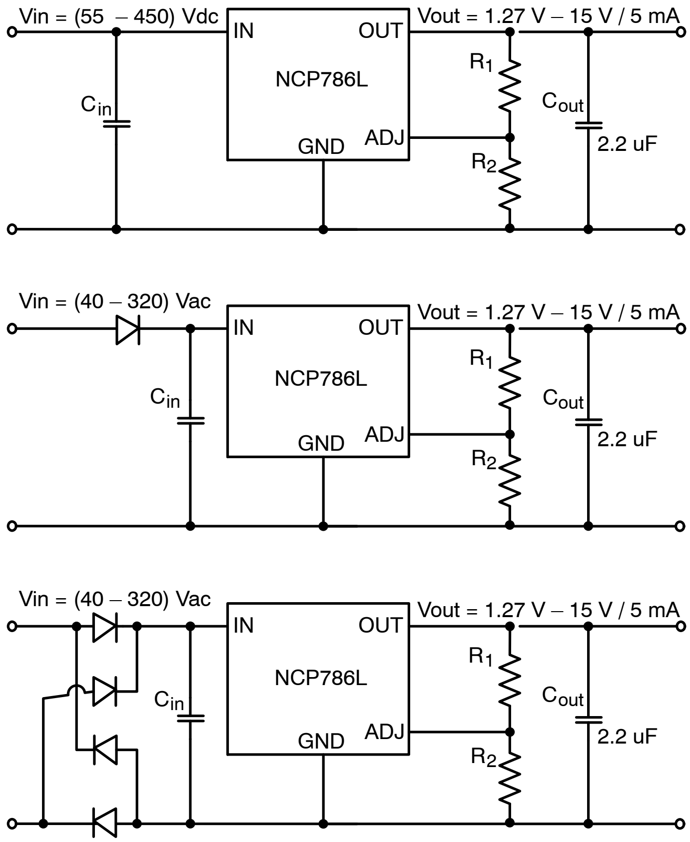


Figure 7. Typical Application Schematic

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or electrolytic is recommended and should be connected close to the input pin of NCP786L. Higher value 2.2 μF is necessary to keep the input voltage above the required minimum input voltage at full load for AC voltage as low as 85 V with half wave rectifier. The capacitor 1 μF could be acceptable for DC input voltage from 55 V up to 450 V or AC input voltage 235 V ±20%. There must be assured minimum Input Voltage more than 55 V at input pin of NCP786L regulator in order to keep stable desired output voltage with guaranteed parameters at AC supply.

Output Decoupling (C2)

The NCP786L Regulator does not require any specific Equivalent Series Resistance (ESR). Thus capacitors exhibiting ESRs ranging from a few mΩ up to 0.5 Ω can be used safely. The minimum decoupling value is 2.2 μF. The regulator accepts ceramic chip capacitors as well as tantalum devices or low ESR electrolytic capacitors. Larger values improve noise rejection and especially load transient response.

Layout Recommendations

Please be sure that the V_{IN} and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up a noise or to cause the malfunction of regulator by induced parasitic signal.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP786L increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design layout and used package. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature rise for the part. This is stating that when the NCP786L has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

Output Voltage

The output voltage can be set by using a resistor divider as shown in Figure 1 with a range of 1.27 to 15 V. The appropriate resistor divider can be found by solving the equation below.

$$V_{OUT} = 1.27 \times \left(1 + \frac{R1}{R2}\right) + \left(I_{ADJ} \times R1\right) \quad \text{(eq. 1)}$$

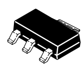
The recommended current through the resistor divider is from 1 μA to 3 μA in order to keep negligible ADJ pin consumption. In this case we can simplify the Equation 1 to:

$$V_{OUT} = 1.27 \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 2)}$$

ORDERING INFORMATION:

Part Number	Output Voltage	Case	Package	Marking	Shipping†
NCP786LSTADJT3G	ADJ	318E	SOT223−4	RRA	1000 / Tape & Reel

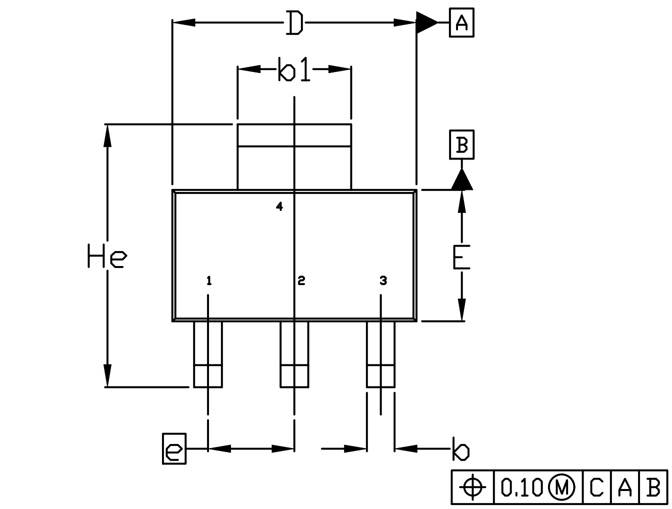
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

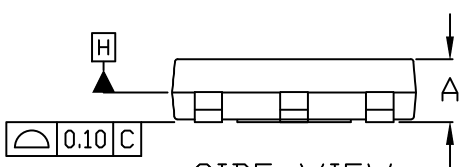
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

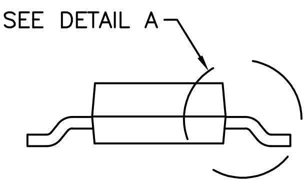


TOP VIEW

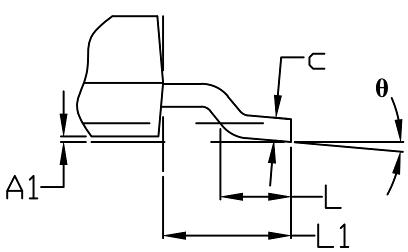
NOTE 5



SIDE VIEW



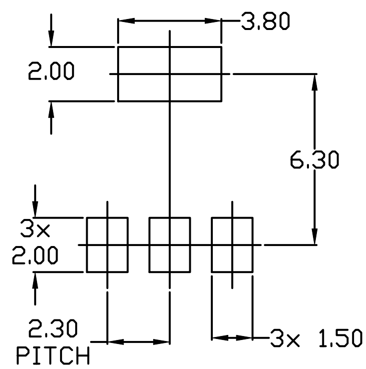
FRONT VIEW



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

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DESCRIPTION:	SOT−223 (TO−261)	PAGE 1 OF 2

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

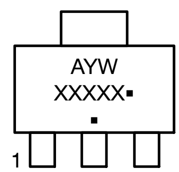
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC
MARKING DIAGRAM*



A	= Assembly Location
Y	= Year
W	= Work Week
XXXXX	= Specific Device Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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