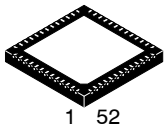
8 + 1 Phase Output Controller with SVID Interface for Computer CPU Applications

NCP81560



QFN52 6x6, 0.4P
CASE 485BE

The NCP81560 is a dual rail, eight plus one phase buck solution optimized for Intel's IMVP9.1 CPUs. The multi−phase rail control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing. This provides an ultra−fast initial response to dynamic load events and reduced system cost. The NCP81560 has an ultra−low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

Features

- Vin Range 4.5 V to 21 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable Vboot
- High Impedance Differential Output Voltage Amplifier
- Dual VID Table Support to Be Compatible with IMVP9.1
- Support High Current Extensions
- Dynamic Reference Injection
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Adjustable Switching Frequency Range
- Digitally Stabilized Switching Frequency
- UltraSonic Operation
- Supports Acoustic Noise Mitigation Function
- Support for VCCIN_AUX IMON Input
- Meets Intel's IMVP9.1 Specifications
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- This is a Pb−Free Device

Typical Applications

- Computers

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81560MNTXG	QFN52 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

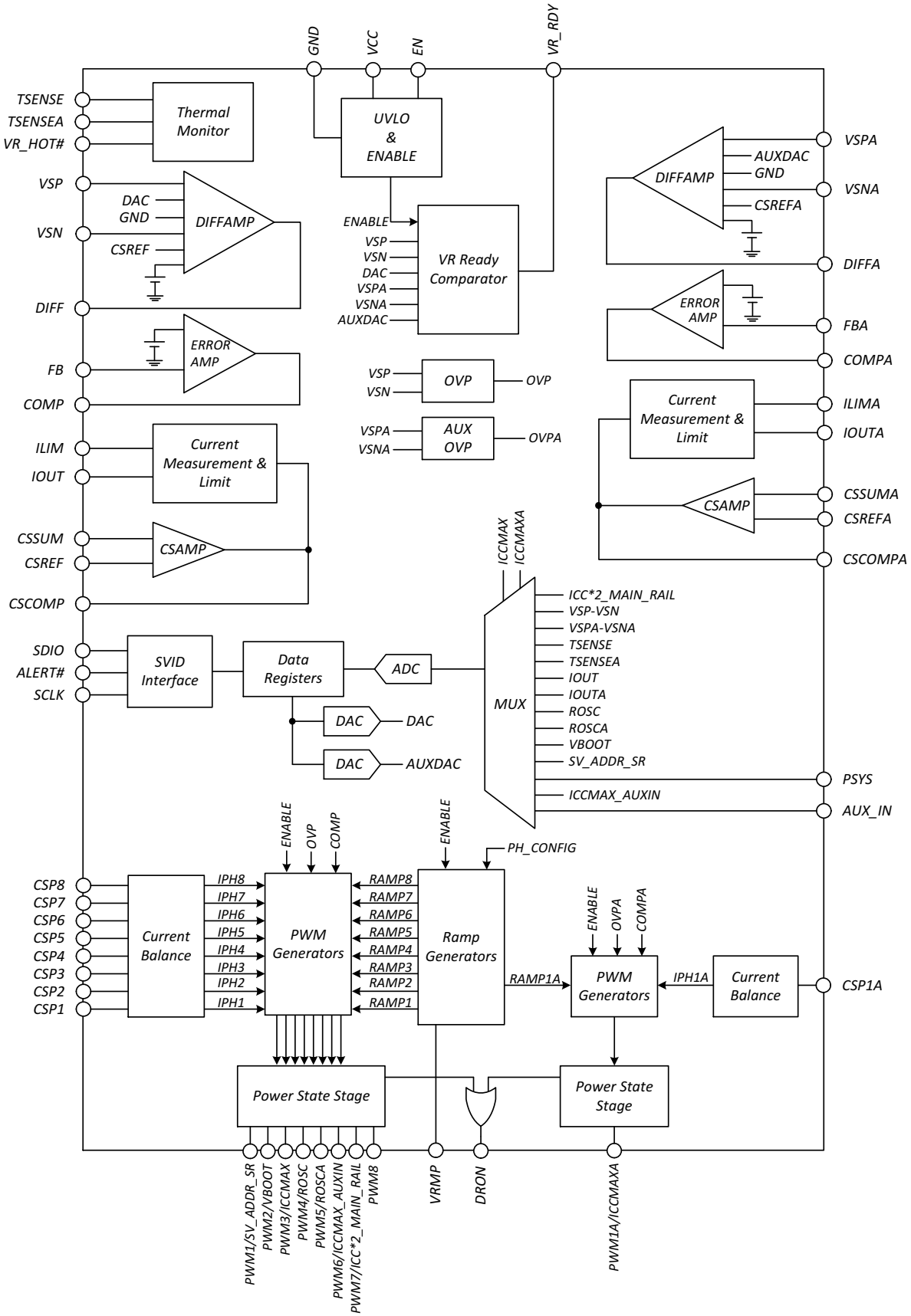


Figure 1. Internal Block Diagram

APPLICATIONS INFORMATION

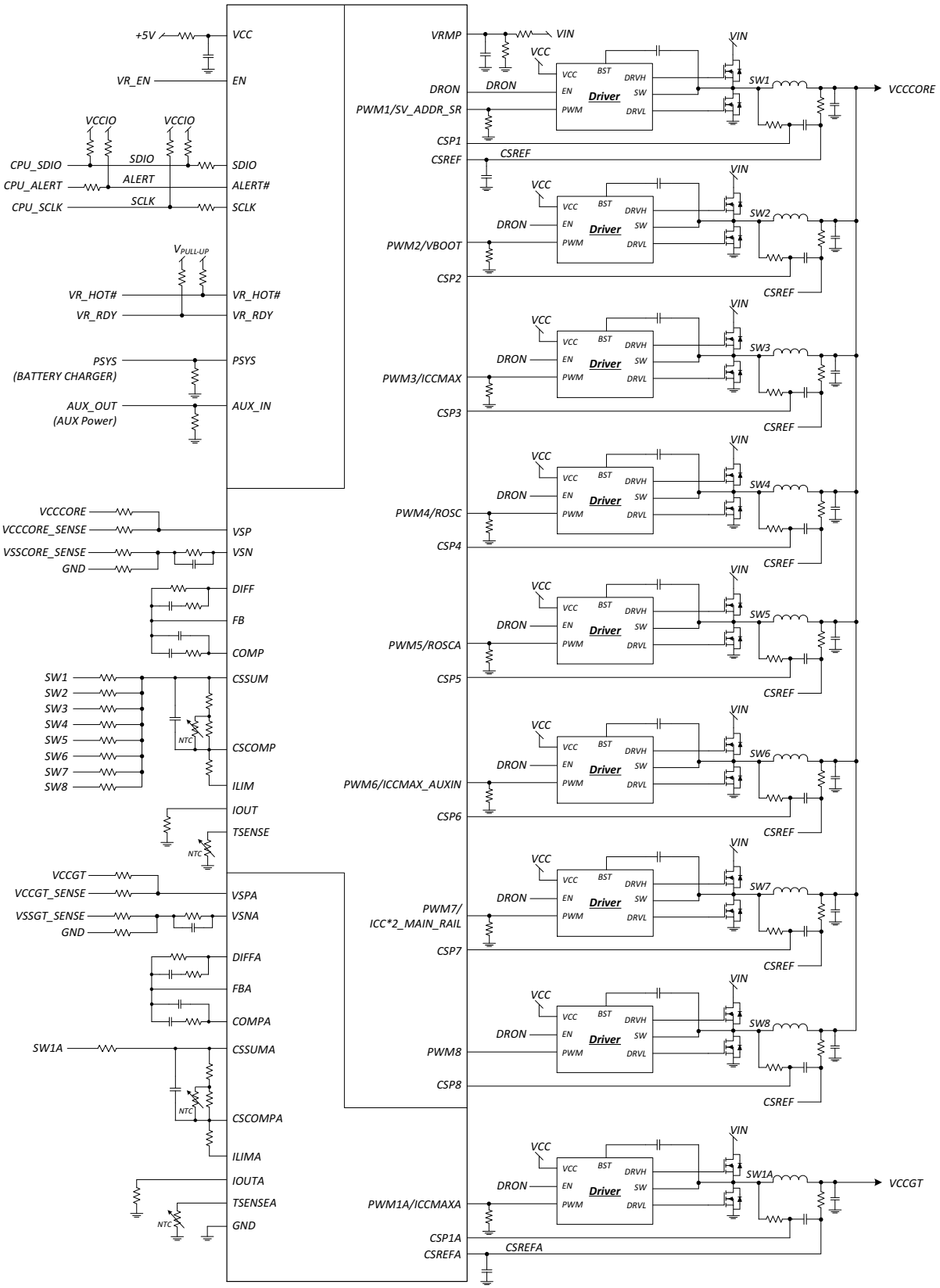


Figure 2. Typical Application Circuit

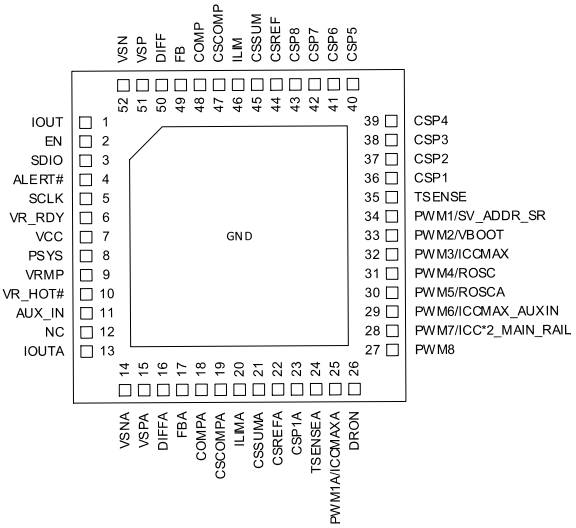


Figure 3. Pinout

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	IOUT	Total output current monitor for regulator 1
2	EN	Enable. High enables both rails
3	SDIO	Serial VID data interface
4	ALERT#	Serial VID ALERT#
5	SCLK	Serial VID clock
6	VR_RDY	VR_RDY indicates both rails are ready to accept SVID commands
7	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
8	PSYS	System power signal input. A resistor to ground scales this signal.
9	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes
10	VR_HOT#	OD output. Indicates high VR temperature or per channel OCP.
11	AUX_IN	AUX IMON Input on 0x0Dh SVID domain. A resistor to ground scales this signal.
12	NC	Reserved.
13	IOUTA	Total output current monitor for regulator 2
14	VSNA	Differential output voltage negative sense for regulator 2
15	VSPA	Differential output voltage positive sense for regulator 2
16	DIFFA	Output of the regulator 2's differential remote sense amplifier
17	FBA	Error amplifier voltage feedback for regulator 2
18	COMPA	Output of the error amplifier and the inverting inputs of the PWM comparators for regulator 2
19	CSCOMPA	Output of total−current−sense amplifier for regulator 2
20	ILIMA	Over−current threshold setting − programmed with a resistor to CSCOMPA for regulator 2
21	CSSUMA	Inverting input of total−current−sense amplifier for regulator 2
22	CSREFA	Total−current−sense amplifier reference voltage input for regulator 2
23	CSP1A	Non−inverting input to current−balance amplifier for Phase 1 of regulator 2
24	TSENSEA	Temperature sense input for regulator 2
25	PWM1A / ICCMAXA	PWM1 output for regulator 2. Pulldown on this pin programs ICCMAX for regulator 2 during startup

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
26	DRON	External FET driver enable for discrete driver or **onsemi** DrMOS
27	PWM8	PWM8 output for regulator 1
28	PWM7 / ICC*2_MAIN_RAIL	PWM7 output for regulator 1 / Pulldown on this pin programs ICCMAX on main rail from 255 to 511A
29	PWM6 / ICCMAX_AUXIN	PWM6 output for regulator 1 / Pulldown resistor on this pin programs ICCMAX for the AUX_IN monitoring rail
30	PWM5 / ROSCA	PWM5 output for regulator 1 / Pulldown on this pin programs RoscA value for regulator 2
31	PWM4 / ROSC	PWM4 output for regulator 1 / Pulldown on this pin programs Rosc value for regulator 1
32	PWM3 / ICCMAX	PWM3 output for regulator 1 / Pulldown on this pin programs ICCMAX for regulator 1 during startup
33	PWM2 / VBOOT	PWM2 output for regulator 1 / Pin−program for eight−phase and one−phase Vboot.
34	PWM1 / SV_ADDR_SR	PWM1 output for regulator 1 / Pulldown on this pin configures SVID address and slew rate and Intel Proprietary Current Protection Feature.
35	TSENSE	Temperature sense input for regulator 1
36	CSP1	Differential current sense positive for Phase 1 of regulator 1
37	CSP2	Differential current sense positive for Phase 2 of regulator 1
38	CSP3	Differential current sense positive for Phase 3 of regulator 1
39	CSP4	Differential current sense positive for Phase 4 of regulator 1
40	CSP5	Differential current sense positive for Phase 5 of regulator 1
41	CSP6	Differential current sense positive for Phase 6 of regulator 1
42	CSP7	Differential current sense positive for Phase 7 of regulator 1
43	CSP8	Differential current sense positive for Phase 8 of regulator 1
44	CSREF	Total−current−sense amplifier reference voltage input for regulator 1
45	CSSUM	Inverting input of total−current−sense amplifier for regulator 1
46	ILIM	Over−current threshold setting − programmed with a resistor to CSCOMP for regulator 1
47	CSCOMP	Output of total−current−sense amplifier for regulator 1
48	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for regulator 1
49	FB	Error amplifier voltage feedback for regulator 1
50	DIFF	Output of the regulator 1’s differential remote sense amplifier
51	VSP	Differential output voltage sense positive for regulator 1
52	VSN	Differential output voltage sense negative for regulator 1
	Flag	GND

1. “Regulator 1” is referred to as “Main” rail throughout the datasheet, “Main” is the primary rail with the highest phase count.
2. “Regulator 2” is referred to as “A” rail throughout the datasheet.

Table 2. MAXIMUM RATINGS (Note 3)

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP, COMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP, CSCOMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWMX	VCC + 0.3 V	−0.3 V	–	1 mA
VSN, VSNA	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
DIFF, DIFFA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	2 mA	–
VCC	6.0 V	−0.3 V	–	–
VRMP	VCC + 0.3 V	−0.3 V	–	–
SCLK, SDIO	3.6 V	−0.3 V	–	–
All Other Pins	VCC + 0.3 V	−0.3 V	–	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All signals referenced to GND unless noted otherwise

Table 3. ESD CAPABILITY

Description	Symbol	Typ	Unit
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 4)	ESD_{CDM}	750	V

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charge Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latch−up Current Maximum Rating: ≤200 mA per JEDEC standard: JESD78.

Table 4. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Max	Unit
VCC Voltage Range	VCC	4.75	5.25	V
Operating Junction Temperature Range (Note 2)	TJ	−40	125	°C
Operating Ambient Temperature Range	TA	−40	100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. JEDEC JESD 51−7 with 0 LFM.

Table 5. THERMAL CHARACTERISTICS

Description	Symbol	Value	Unit
Thermal Characteristic QFN Package	R_{JA}	68	°C/W
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	
Soldering Temperature		260	°C
Junction−to−Ambient, Thermal Resistance (Note 6)	θ_{JA}	30	°C/W
Junction−to−Case (Top), Thermal Resistance (Note 6)	$\theta_{JC(TOP)}$	18	°C/W
Junction−to−Board Heat Spreader, Thermal Resistance (Note 6)	θ_{JB}	1.0	°C/W
Junction−to−Case (Top), Measurement Reference (Note 6)	Ψ_{J-CT}	1.1	°C/W

6. JEDEC JESD 51−7 with 0 LFM

Table 6. ELECTRICAL CHARACTERISTICS (−40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Voltage Range		4.75	–	5.25	V
Quiescent Current (PS0, 1)	PS0	–	29	–	mA
	PS1	–	25	–	mA
	PS2	–	21	–	mA
	PS3	–	14	–	mA
	PS4	–	–	79	μA
	Enable low	–	–	64	μA
UVLO Threshold	VCC Rising	–	–	4.5	V
	VCC Falling	4.1	–	–	V
	VCC UVLO Hysteresis	–	100	–	mV
VRMP					
VIN Supply Range	VRMP range prior to external voltage divider resistor network with 1/12 ratio	4.5	–	21	V
UVLO Threshold	VRMP Rising	–	–	0.355	V
	VRMP Falling	0.250	–	–	V
UVLO Hysteresis		–	100	–	mV
ENABLE INPUT					
Upper Threshold	Activation Level	0.8	–	–	V
Lower Threshold	Deactivation Level	–	–	0.3	V
PHASE DETECTION					
CSP Pin Threshold Voltage		VCC − 0.4	–	–	V
Phase Detect Timer		–	1.5	–	ms
IMVP9.1 DAC (Protocol 0Eh)					
System Voltage Accuracy	0.25 < DAC < 0.495 V (at 25°C only)	−10	–	10	mV
	0.5 < DAC < 0.745 V (at 25°C only)	−8	–	8	mV
	0.75 < DAC < 1.52 V (at 25°C only)	−0.5	–	0.5	%
DAC SLEW RATE					
Soft Start Slew Rate		–	1/4 fast	–	mV/μs
Slew Rate Slow		–	1/4 fast	–	mV/μs
Slew Rate Fast	Resistor Selectable (See Table 9)	–	>10	–	mV/μs
DRON					
Output High Voltage	Sourcing 500 μA	3	–	–	V
Output Low Voltage	Sinking 500 μA	–	–	0.1	V
TSENSE					
TSENSE Bias Current		115.5	120	124.5	μA
Alert#	Assert Threshold	–	556	–	mV
	De−Assert Threshold	–	595	–	mV
VR_HOT	Assert Threshold	–	517	–	mV
	De−Assert Threshold	–	556	–	mV

Table 6. ELECTRICAL CHARACTERISTICS (−40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
VR_RDY OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = −4 mA	–	0.1	0.3	V
VR_RDY Rise Time	1 kΩ pull−up to 3.3 V CTOT = 45 pF	–	110	150	ns
VR_RDY Fall Time		–	20	150	ns
VR_RDY Output Voltage High		0.8	–	3.3	V
SVID (SDIO and SCLK)					
SVID Voltage Low Level	VIL, (V_{CC} = 5 V, T_A = 25°C)	–	–	0.45	V
SVID Voltage High Level	VIH, (V_{CC} = 5 V, T_A = 25°C)	0.65	–	–	V
SDIO Output Low Voltage	VOL	–	–	0.3	V
SVID Clock to Data Delay (Note 7)	TCO	–	–	12	ns
SVID Setup Time (Note 7)		7	–	–	ns
SVID Hold Time (Note 7)		14	–	–	ns
SVID Pull Down Resistance		–	4	–	Ω
Pad and Pin Capacitance	V_{CC} = 5 V, T_A = 25°C	–	5	–	pF
ALERT#					
VOL (Output Low)		–	–	0.3	V
OVP AND UVP					
Absolute Over Voltage Threshold	10 mV DAC step During Soft Start − CSREF Rising	3.3	3.44	3.6	V
	5 mV DAC step During Soft Start − CSREF Rising	2.4	2.5	2.65	V
Over Voltage Threshold Above DAC	VSP−VSN−VID Rising	350	400	475	mV
Over Voltage Delay	VSP−VSN Rising to PWM Low		50		ns
Under Voltage Threshold Below DAC−DROOP (VUVM)	VSP−VSN−VID Falling	−440	−400	−360	mV
Under Voltage Delay		–	5	–	μs
PWM OUTPUT					
Output High Voltage	Sourcing 500 μA	Vcc − 0.2	–	–	V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA	–	–	0.7	V
DIFFERENTIAL AMPLIFIER					
Input Bias Current	VSP = 1.3 V	200	–	500	nA
−3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ	–	22.5	–	MHz
Closed Loop DC Gain	VSP − VSN = 0.5 V to 1.3 V	–	1	–	V/V
ERROR AMPLIFIER					
Input Bias Current	Input = 1.3 V	−400	–	400	nA
DC Gain	CL = 20 pF, RL = 10 kΩ	–	80	–	dB
−3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ	–	20	–	MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 1.5 V to 2.5 V, CL = 20 pF, RL = 10 kΩ	–	5	–	V/μs
OVER−CURRENT PROTECTION (ILIM)					
ILim Threshold Current (Delayed OCP shutdown)	PS0	8.5	10	11.5	μA
	PS1, PS2, PS3	–	10/N*	–	μA

Table 6. ELECTRICAL CHARACTERISTICS (−40°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
ILim Threshold Current (Immediate OCP shutdown)	PS0	13.5	15	16.5	μA
	PS1, PS2, PS3	–	15/N*	–	μA
Shutdown Delay	Immediate	–	1.3	–	μs
	Delayed	–	50	–	μs
IOUT OUTPUT					
Current Gain	IOUT/ILIM (RLIM = 20 kΩ, RIOUT = 5 kΩ, Vout = 0.8 V, 1.25 V, 1.52 V)	9.5	10	10.5	A/A
PWM GENERATOR					
PWM Minimum Pulse Width		–	40	–	ns
0% Duty Cycle	Comp Voltage for PWM Held Low	–	1.3	–	V
100% Duty Cycle	Comp Voltage for PWM Held High VIN at 4.5 V	–	1.75	–	V
100% Duty Cycle	Comp Voltage for PWM Held High VIN at 21 V	–	3.4	–	V
CURRENT SUMMING AMPLIFIER (CSAMP)					
Offset Voltage		−500	–	500	μV
Input Bias Current	CSSUM = CSREF = 1.0 V	−10	–	10	μA
Open Loop Gain		–	80	–	dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	10	–	MHz
CURRENT BALANCE AMPLIFIER					
Differential Mode Input Voltage Range	CSREF = 1.2 V	−100	–	100	mV
PSYS					
Full Scale Input Voltage		–	2.5	–	V
Disable Threshold		–	VCC − 0.4	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*N is the phase configuration number in PS0.
7. Guaranteed by characterization, not production tested.

Start Up

Following the rise of VCC above the UVLO threshold, externally programmed configuration data is collected, and all PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRON is asserted (high) to activate the external gate drivers. A digital counter steps the DAC up from zero to the target boot voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced. When the controller is disabled, the PWM signals return to Mid−level. The VR_RDY signal is asserted when the controller is ready to accept the first SVID command.

DEVICE CONFIGURATION

Phase and Rail Configuration

During start−up, the number of operational phases of the multiphase rail is determined by the internal circuitry monitoring the CSP inputs. If a reduced phase count is required, the appropriate CSP pins should be externally pulled to VCC with a resistor during startup.

Basic Configuration

The controller has four basic configuration features. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- SVID Address
- Slew Rate
- V_{BOOT}
- Output Voltage Step

SVID address and slew rate options are shown in Table 9.

V_{BOOT} and output voltage step options are shown in Table 10.

Switching Frequency

Switching frequencies between 180 kHz and 1.17 MHz are programmed at startup with pulldown resistors on Rosc and RoscA pin. Switching frequency options are shown in Table 13.

ICCMAX

Resistors to ground on the PWM3/ICCMAX, PWM1A/ICCMAXA and PWM6/ICCMAX_AUXIN pins programs these registers at the time the part is enabled.

On power up a 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is set by the equation below. The resistor value should be no less than 10 kΩ.

$$ICC_{MAX} = \frac{R \cdot 10\ \mu A \cdot 255\ A}{2.5\ V} \quad \text{(eq. 1)}$$

ICCMAX Additional Capability

There is an option to extend the current range of the main rail by scaling the lsb size (see Table 7). See Table 11 for details on how to enable this mode.

Table 7. ICCMAX CAPABILITY SCALING

ICCMAX_ADD$_{50h}$[4:0]		ICC Scaling	Power Scaling
Power [4:2]	Current [1:0]		
010	00	1 A / bit	4 W / bit
011	01	2 A / bit	8 W / bit

Table 8 shows the rail configurations when ICC*2_MAIN_RAIL mode is enabled and disabled.

Table 8. RAIL SETTINGS FOR ICC*2_MAIN_RAIL MODE

		ICC*2_MAIN_RAIL	
		Disabled	Enabled
Main Rail	ICCMAX$_{21h}$ LSB Size	1A	2A
	IOUT$_{15h}$ LSB Size	1A	2A
	POUT$_{18h}$ LSB Size	4 W	8 W
	HIGHPOWER_ICCMAX_ADD$_{50h}$[1:0]	00	01
	HIGHPOWER_ICCMAX_ADD$_{50h}$[4:2]	010	011
	Loadline Weighting	43.75%	87.50%
A Rail	ICCMAX$_{21h}$ LSB Size	1A	
	IOUT$_{15h}$ LSB Size	1A	
	POUT$_{18h}$ LSB Size	4 W	
	HIGHPOWER_ICCMAX_ADD$_{50h}$[1:0]	00	
	HIGHPOWER_ICCMAX_ADD$_{50h}$[4:2]	010	
	Loadline Weighting	93.75%	
VCCIN_AUX	ICCMAX$_{21h}$ LSB Size	1A	
	IOUT$_{15h}$ LSB Size	1A	
	POUT$_{18h}$ LSB Size	4 W	
	HIGHPOWER_ICCMAX_ADD$_{50h}$[1:0]	00	
	HIGHPOWER_ICCMAX_ADD$_{50h}$[4:2]	010	

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

CCM/DCM Operation

In PS0, all rails operate in Continuous Conduction Mode (CCM) which uses the dual−edge control methodology. However, if PS0 is configured as one−phase instead of multi−phase, the control methodology changes to RPM operation. RPM has great transient performance in one−phase CCM operation.

The RPM frequency average DC value is targeted to be similar to the PS0 Dual Edge frequency. However, the switching frequency of RPM depends on input voltage, output voltage, load current, inductor value, and output capacitor value. In PS1, all rails operate in one−phase CCM RPM. In PS2 and PS3, all rails operate in either CCM or Discontinuous Conduction Mode (DCM). It depends on load current in order to prevent loss of efficiency from negative inductor current.

Table 9. NCP81560 SVID ADDRESS AND SLEW RATE

Resistor (kΩ)	SR (mV/μs)	Main Rail Address	A Rail Address	Intel Proprietary Current Protection Feature
10	10	00	01	ON
14	30	00	01	ON
18.7	48	00	01	ON
24.3	10	01	00	OFF
30.9	30	01	00	OFF
38.3	48	01	00	OFF
47.5	10	00	02	ON
59	30	00	02	ON
71.5	48	00	02	ON
86.6	10	01	02	OFF
105	30	01	02	OFF
127	48	01	02	OFF

Table 10. V_{BOOT} AND OUTPUT VOLTAGE STEP

Resistor (kΩ)	V_{BOOT} (V) Main Rail	V_{BOOT} (V) A Rail	Output Voltage Step
10	0 V	0 V	Both rail 5 mV/step
14	0 V	1.05 V	
18.7	1.05 V	0 V	
24.3	1.05 V	1.05 V	
30.9	0 V	0 V	Both rail 10 mV/step
38.3	0 V	1.8 V	
47.5	1.8 V	0 V	
59	1.8 V	1.8 V	
71.5	0 V	0 V	Main rail 5 mV/step. A rail 10 mV/step.
86.6	0 V	1.8 V	
105	1.05 V	0 V	
127	1.05 V	1.8 V	
154	0 V	0 V	Main rail 10 mV/step. A rail 5 mV/step.
187	1.8 V	0 V	
221	0 V	1.05 V	
280	1.8 V	1.05 V	

Table 11. POWER STATES

SVID Power State	Typical Operating Mode
PS0	Multiphase rail dual edge
PS1	One−phase CCM RPM
PS2	One−phase DCM RPM
PS3	One−phase DCM RPM
PS4	Standby

PSYS

The PSYS pin is an analog input to the VR controller. PSYS is a system input power monitor that facilitates the monitoring of the total platform system power. For more details about PSYS please contact Intel, Inc.

AUX_IN

The AUX_IMON current monitor input is a means of measuring the VCCIN_AUX platform VR output current using the IMVP9.1 ADC.

Programming Pin

This is a multifunction select pin used to set the operation of multiple features and the combination of these features enabled/disabled. Items programmed on this pin are ICC*2_MAIN_RAIL which allows the user to select if the ICCMAX and IOUT reporting for the main rail is a 1 A or 2 A LSB step size. When off, the resolution is 1 A per LSB. When on, the resolution is set to 2 A per LSB which allows reporting of over 255 A on the main rail only.

The other options include dithering and acoustic noise solution.

Table 12. PIN OF ICC*2_MAIN_RAIL CONFIGURATION

Resistor (kΩ)	ICCMAX*2 Main Rail	Acoustic Noise Solution	Dithering
10	OFF	OFF	OFF
14	OFF	OFF	OFF
18.7	OFF	OFF	ON
24.3	OFF	OFF	ON
30.9	OFF	ON	OFF
38.3	OFF	ON	OFF
47.5	OFF	ON	ON
59	OFF	ON	ON
71.5	ON	OFF	OFF
86.6	ON	OFF	OFF
105	ON	OFF	ON
127	ON	OFF	ON
154	ON	ON	OFF
187	ON	ON	OFF
221	ON	ON	ON
280	ON	ON	ON

Table 13. SWITCHING FREQUENCY

	Switching Frequency (kHz)		
Control by Pin Resistor (kΩ)	1 Phase~6 Phase	7 Phase	8 Phase
10	180	180	180
14	225	215	210
18.7	270	250	240
24.3	315	285	270
30.9	360	320	300
38.3	405	355	330
47.5	450	390	360
59	495	425	390
71.5	540	460	420
86.6	630	495	450
105	720	530	480
127	810	600	510
154	900	700	540
187	990	800	600
221	1080	900	700
280	1170	1000	800

THEORY OF OPERATION

Input Voltage Feed−Forward (VRMP Pin)

Ramp generator circuits are provided for the dual−edge modulator. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled. For multi−phase operation, the dual−edge PWM ramp amplitude is changed according to the following:

$$VRMP_{PP} = 0.1 \times V_{VRMP} \quad \text{(eq. 2)}$$

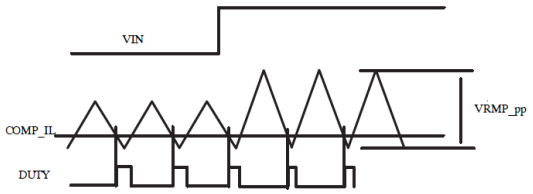


Figure 4. Ramp Feed Forward

An external voltage divider is required on this VRMP pin in order to scale the voltage seen on the VRMP pin the voltage divider on the pin needs to be setup to maintain a ratio of 1/12. Typical resistor values may include 1 MΩ Rup / 90.9 KΩ Rdown or 1.1 MΩ Rup / 100 KΩ Rdown.

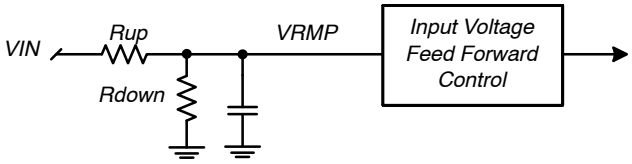


Figure 5. Ramp Feed Forward Circuit

Differential Current Feedback Amplifiers

Each phase of the rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset due to leakage current.

It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance.

The external filter RCSN and CCSN time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \times DCR} \quad \text{(eq. 3)}$$

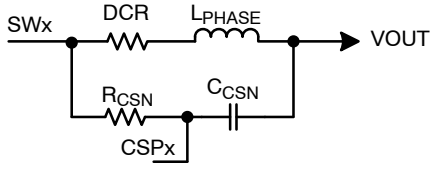


Figure 6. Per Phase Current Sense Network

Total Current Sense Amplifier

The multiphase rail uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The Rref(n) resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The Rph resistors sum currents from the switch nodes to the virtual CSREF potential created at the CSSUM pin by the amplifier. The total current signal is the difference between the CSCOMP and CSREF voltages.

The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. Phase 1 inductor is chosen for the thermistor location so that the temperature of the inductor providing current in the PS1 power mode.

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP} - V_{CSREF} = -\frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times I_{OUT} \quad \text{(eq. 4)}$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline. The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

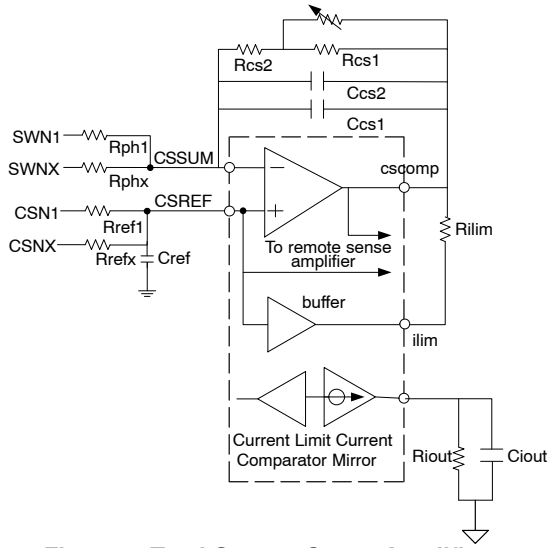


Figure 7. Total Current Sense Amplifier

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$F_Z = \frac{DCR_{25°C}}{2\pi \times L_{Phase}} \quad \text{(eq. 5)}$$

$$F_P = \frac{1}{2\pi \times \left(R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}\right) \times (C_{CS1} + C_{CS2})} \quad \text{(eq. 6)}$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier.

The value of the CREF capacitor (in nF) on the CSREF pin should be:

$$Cref = \frac{0.02 \times Rph}{Rref} \quad \text{(eq. 7)}$$

High Performance Voltage Error Amplifier

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

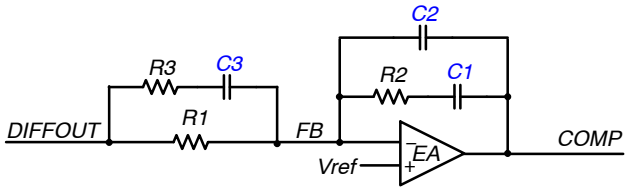


Figure 8. Error Amplifier

Loadline Programming (V_{DROOP})

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

A load line is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. The load line is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

$$V_{DROOP} = \frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times I_{OUT} \quad \text{(eq. 8)}$$

For the main rail, loadline programming is dependent on its programmed ICCMAX value.

$$Loadline = DCR \times \frac{Rcs}{Rph} \times Weighting \quad \text{(eq. 9)}$$

For ICC*2_MAIN_RAIL configuration enabled, weighting = 87.50%.

For ICC*2_MAIN_RAIL configuration disabled, weighting = 43.75%.

For the A rail, load line weighting = 93.75%.

Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - v_{DAC}) + (V_{DROOP} - V_{CSREF}) \quad \text{(eq. 10)}$$

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The multiphase rails generates a replica of the CSREF pin voltage at the ILIM pin, and compares ILIM pin current to ICL and ICLM. The controller latches off if ILIM pin current exceeds ICL for t_OCPDLY, and latches off immediately if ILIM pin current exceeds ICLM. Set the value of the current limit resistor RLIMIT according to the desired current limit Iout LIMIT.

$$R_{LIMIT} = \frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times I_{OUT_{LIM}} \Big/ 10\ \mu \quad \text{(eq. 11)}$$

Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT.

$$R_{IOUT} = \frac{2.5\ V \times R_{LIMIT}}{10 \times \frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times ICCMAX} \quad \text{(eq. 12)}$$

Programming DAC Feed−Forward Filter

The multiphase rail outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a dynamic voltage change up command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during dynamic voltage change to be regulated slightly higher, in order to compensate for the response of the DROOP function to current flowing into the charging output capacitors. In the following equations, C_{OUT} is the total output capacitance of the system.

$$R_{FF} = Cout \times LL \times 453.6 \times 10^{6} \quad \text{(eq. 13)}$$

$$C_{FF} = \frac{LL \times Cout}{R_{FF}} \quad \text{(eq. 14)}$$

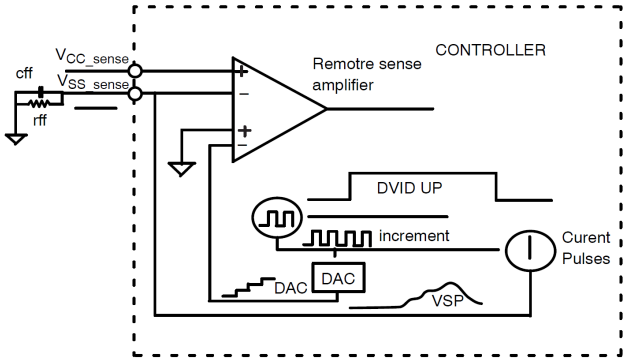


Figure 9. DAC Feed Forward

TSENSE Network

A temperature sense input is provided for each rail. A precision current is sourced from the output of the TSENSE pin to generate a voltage on the temperature sense networks. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. Rcomp1 in the following Figure is optional, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

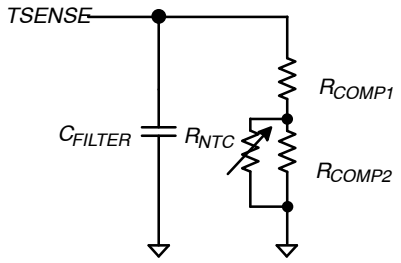


Figure 10. TSENSE Network

PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (IL x DCR x Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output. During steady state PS0 operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

Table 14. PHASE CONFIGURATION

Phase Configuration	Programming Pin in CSPx	Unused Pin
8 + 1	All CSP pins are connected normally	No unused Pin
7 + 1	CSP1 to CSP7 and CSP1A pins connected normally. CSP8 connected to VCC through a 2 kΩ resistor.	Float PWM8.
6 + 1	CSP1 to CSP6 and CSP1A pins connected normally. CSP7 connected to VCC through a 2 kΩ resistor.	Float PWM8 and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only.
5 + 1	CSP1 to CSP5 and CSP1A pins connected normally. CSP6 connected to VCC through a 2 kΩ resistor.	Float PWM8, CSP7, and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only. Use PWM6 for programming ICCMAX_AUXIN only.
4 + 1	CSP1 to CSP4 and CSP1A pins connected normally. CSP5 connected to VCC through a 2 kΩ resistor.	Float PWM8, CSP6, CSP7, and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only. Use PWM6 for programming ICCMAX_AUXIN only. Use PWM5 for programming ROSCA only.
8 + 0	CSP1 to CSP8 pins connected normally. CSP1A connected to VCC through a 2 kΩ resistor.	Float PWM1A.

FAULT PROTECTION

Over Current Protection (OCP)

A programmable total current limit is provided that is decreased when not operating in PS0 mode. This limit is programmed with a resistor between the CSCOMP and ILIM pins. The current from the ILIM pin to this resistor is compared to the ILIM Threshold Currents.

If the fault is not removed, the controller shuts down when the timer expires. If the current into the pin exceeds ICLM, the controller shuts down immediately. To recover from an OCP fault, the EN pin or VCC voltage must be cycled low.

Input Under−voltage Lockouts (UVLO)

The VR monitors the 5 V VCC supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The multiphase rail output voltage is monitored for under voltage at the output of the differential amplifier. If the multiphase− rail output falls more than VUVM2 below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The multiphase phase output voltage is monitored for OVP at the VSP pin. During normal operation, if an output voltage exceeds the DAC voltage by VOVP, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage. At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP threshold as DAC decreases. When the DAC gets to zero, the PWMs will be held low, and the VR will stay in this mode until the VCC voltage or EN is toggled.

Absolute OVP

During start up, the OVP threshold is set to the absolute over voltage threshold. This allows the controller to start up without false triggering OVP.

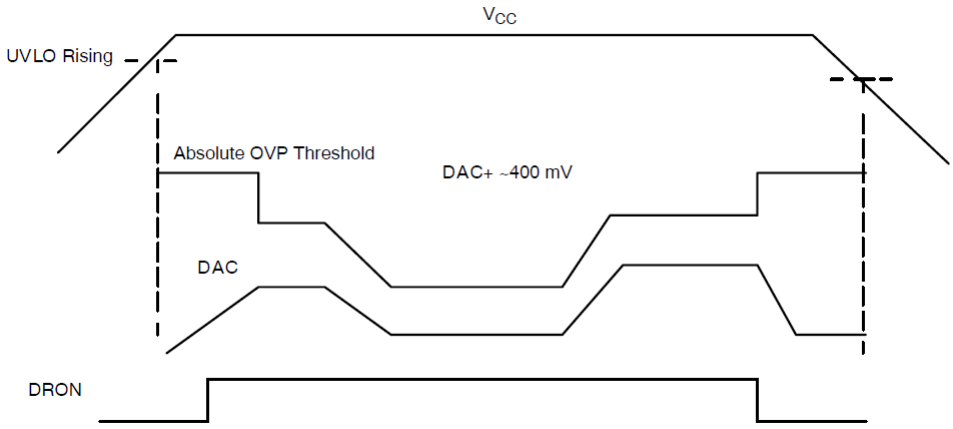


Figure 11. OVP Threshold Behavior

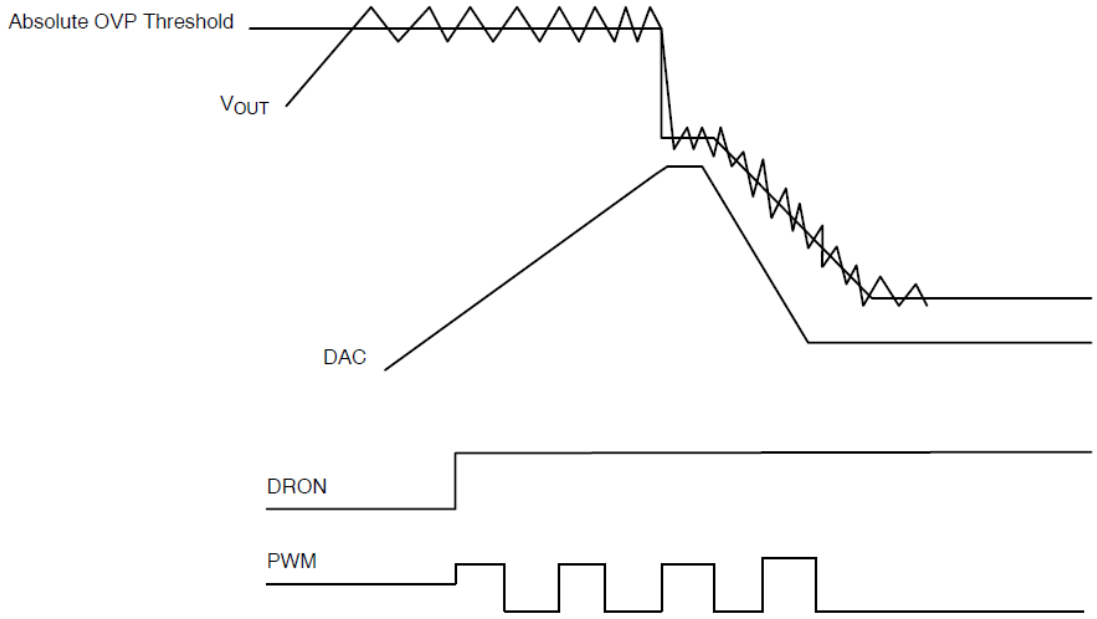


Figure 12. OVP Behavior at Start−up

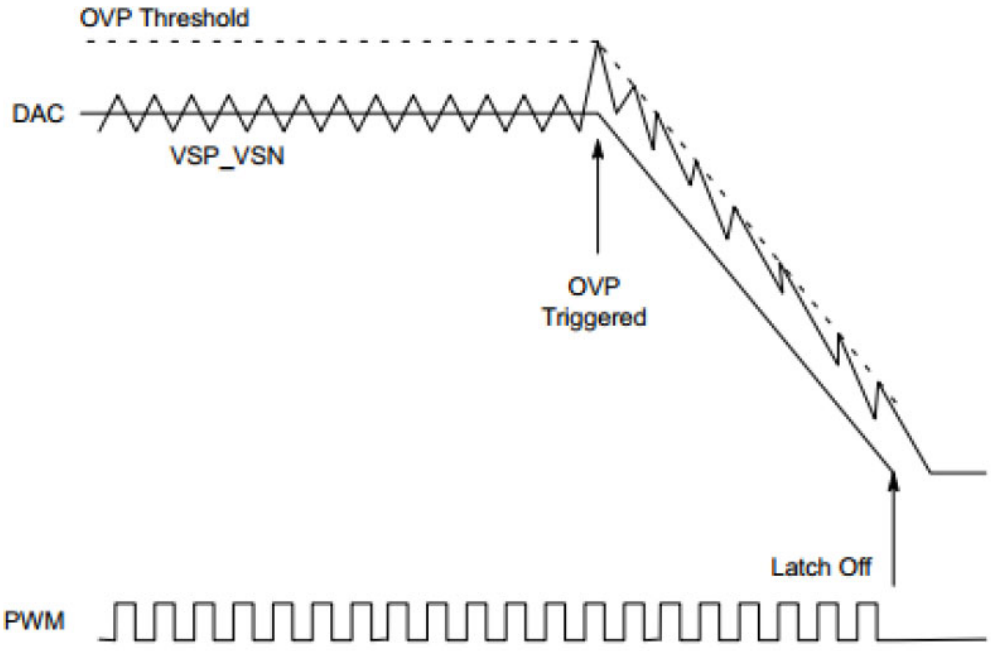


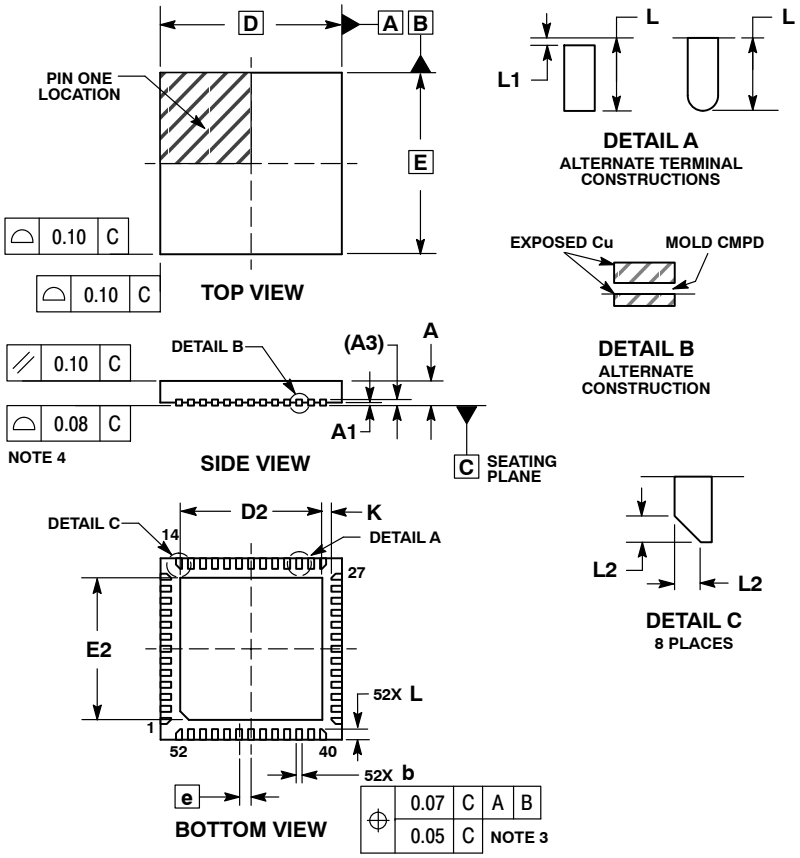
Figure 13. OVP During Normal Operation Mode

Serial VID Interface

For Intel proprietary interface communication details please contact Intel, Inc.

PACKAGE DIMENSIONS

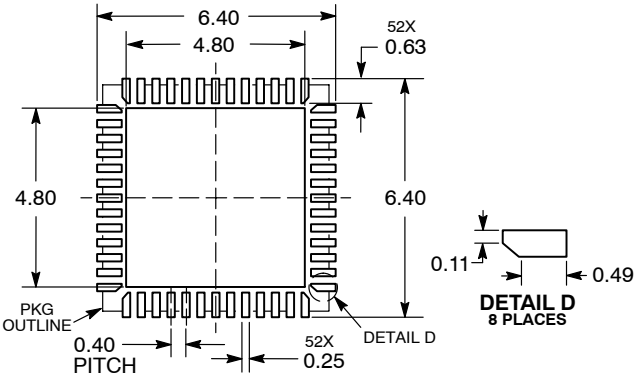
QFN52 6x6, 0.4P
CASE 485BE
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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