NCV1009

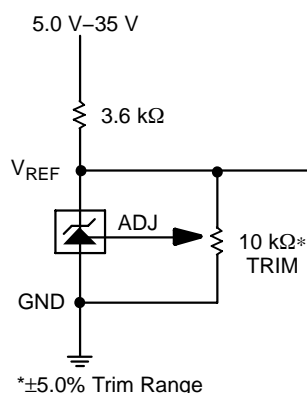# 2.5 Volt Reference

The NCV1009 is a precision trimmed 2.5 V ±5.0 mV shunt regulator diode. The low dynamic impedance and wide operating current range enhances its versatility. The tight reference tolerance is achieved by on−chip trimming which minimizes voltage tolerance and temperature drift.

A third terminal allows the reference voltage to be adjusted ±5.0% to calibrate out system errors. In many applications, the NCV1009Z can be used as a pin−to−pin replacement of the LT1009CZ and the LM136Z−2.5 with the external trim network eliminated.

Features

- 0.2% Initial Tolerance Max.
- Guaranteed Temperature Stability
- Maximum 0.6 Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LT1009 and LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient
- Meets Mil Std 883C ESD Requirements
- Extended Operating Temperature Range for Use in Automotive Applications
- NCV Prefix, for Automotive and Other Applications Requiring Site and Change Control
- Pb−Free Packages are Available

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751

```
8
1009D
ALYW
1
```

TO−92
Z SUFFIX
CASE 29

```
1009Z
ALYWW■
```

A = Assembly Location
L = Wafer Lot
Y = Year
WW, W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

```
      1              8
NC                    NC
NC                    NC
NC                    V_REF
GND                   ADJ. PIN
```

Pin 1. ADJ. PIN
    2. V_REF
    3. GND

```
1 2 3
```

ORDERING INFORMATION

Device	Package	Shipping
NCV1009D	SOIC−8	95 Units/Rail
NCV1009DR2	SOIC−8	2500 Tape & Reel
NCV1009DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
NCV1009Z	TO−92	2000 Units/Rail
NCV1009ZG	TO−92 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

5.0 V−35 V

3.6 kΩ

V_{REF}

ADJ

10 kΩ∗ TRIM

GND

*±5.0% Trim Range

If the external trim resistor is not used, the "ADJ. PIN" should be left floating. The 10k trim potentiometer does not effect the temperature coefficient of the device.
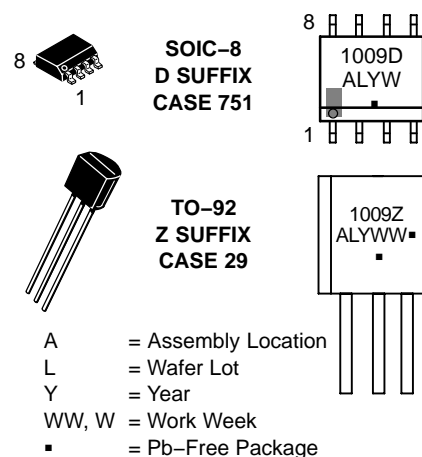
Figure 1. Application Diagram

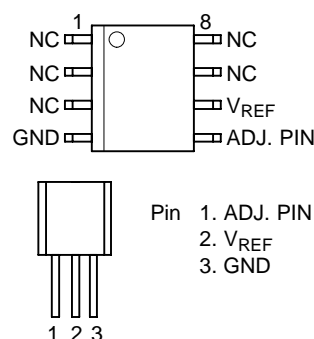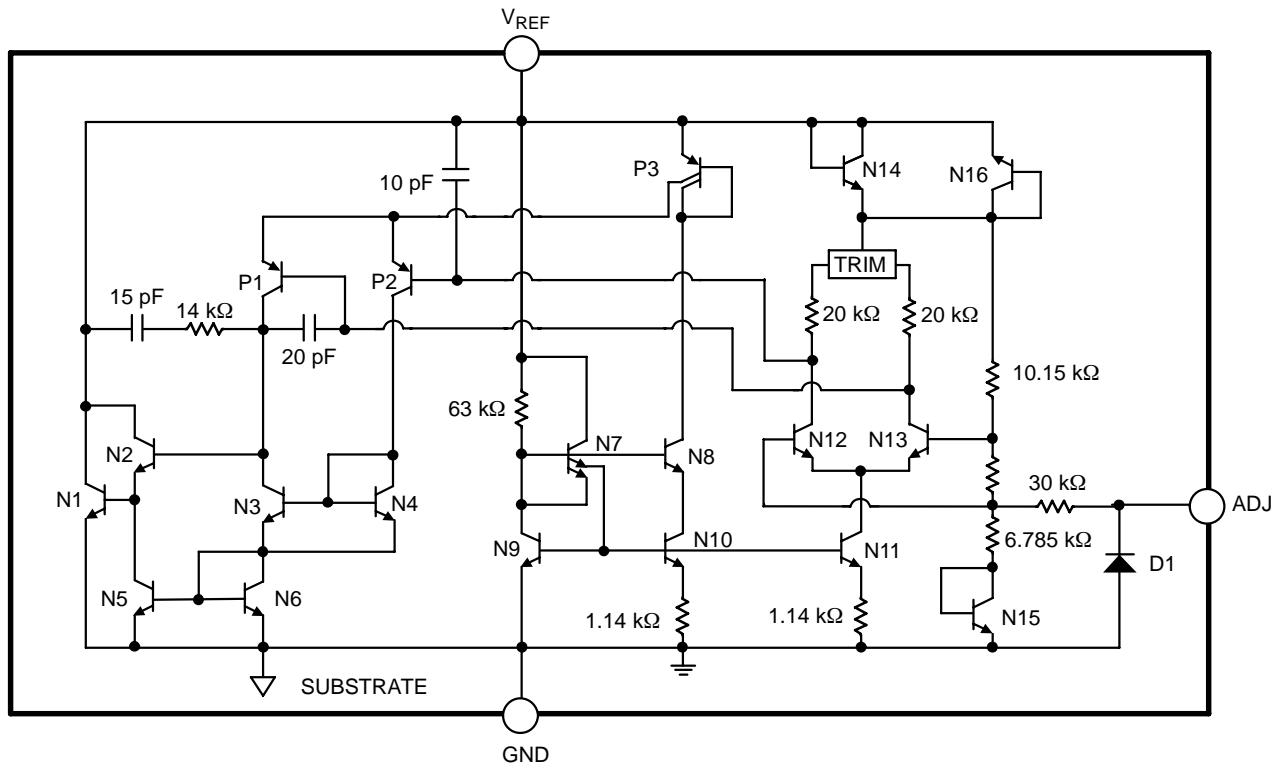**February, 2006 − Rev. 9**

NCV1009

Figure 2. Block Diagram

MAXIMUM RATINGS*

Rating		Value	Unit
Reverse Current		20	mA
Forward		10	mA

Package Thermal Resistance, SOIC−8:
    Junction−to−Case, $R_{\theta JC}$
    Junction−to−Ambient, $R_{\theta JA}$
Package Thermal Resistance, TO−92:
    Junction−to−Case, $R_{\theta JC}$
    Junction−to−Ambient, $R_{\theta JA}$
		45
		165
		
		−
		170
			°C/W
			°C/W
			
			°C/W
			°C/W

Operating Temperature Range		−40 to +125	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Notes 2, 3)	260 peak 240 peak	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
*The maximum package power dissipation must be observed.
1. 10 second maximum
2. 60 second maximum above 183°C.
3. −5°C / +0°C allowable conditions.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 1.0 mA	2.492	2.500	2.508	V
Reverse Breakdown Voltage	−40°C ≤ T_A ≤ 125°C	2.480	2.500	2.508	V
Reverse Breakdown Voltage Change with Current	400 µA ≤ I_R ≤ 10 mA (Note 4)	− −	2.6 3.0	5.0 6.0	mV mV
Reverse Dynamic Impedance	I_R = 1.0 mA (Note 4)	− −	0.2 0.4	1.0 1.4	Ω Ω
Temperature Stability Average Temperature Coefficient	0°C ≤ T_A ≤ 70°C, (Note 5) 0°C ≤ T_A ≤ 70°C, (Note 5)	− −	1.8 15	− −	mV ppm/°C
Long Term Stabilty	T_A = 25°C ±0.1 C, I_R = 1.0 mA	−	20	−	ppm/kHr

4. Denotes the specifications which apply over full operating temperature range.
5. Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

NCV1009
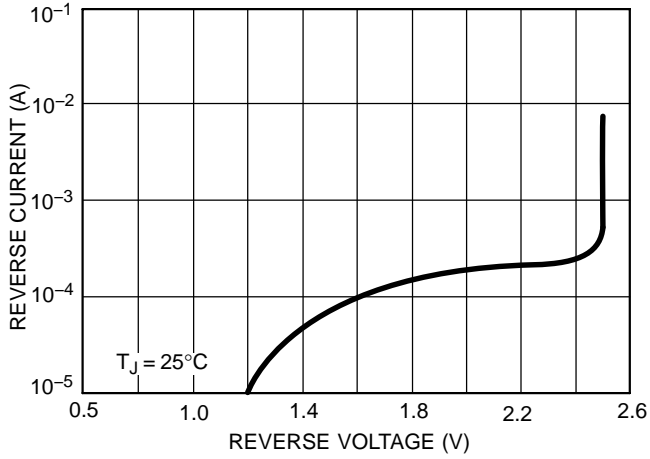
TYPICAL PERFORMANCE CHARACTERISTICS

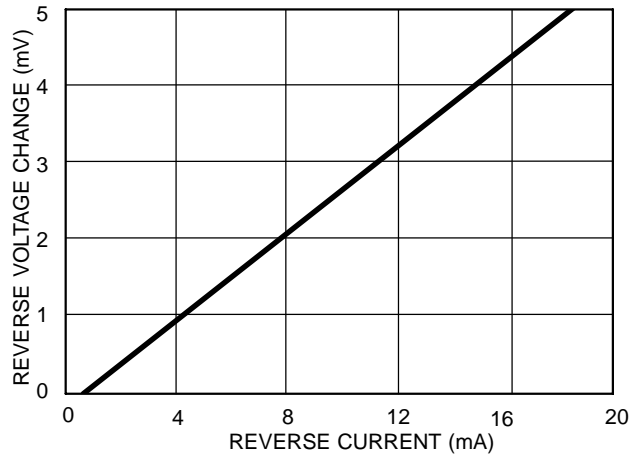**Figure 3. Reverse Current vs. Reverse Voltage**

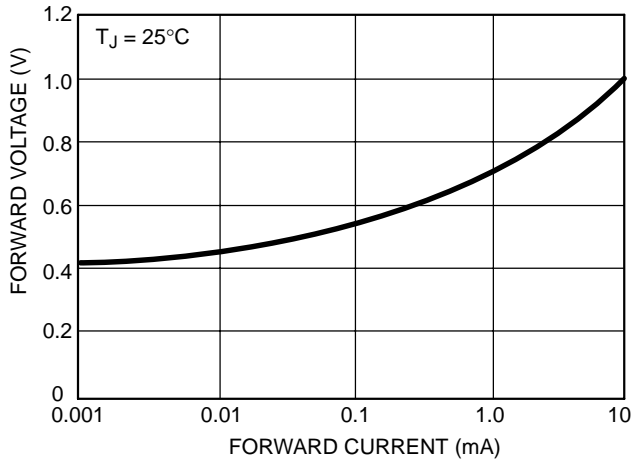**Figure 4. Change in Reverse Voltage vs. Reverse Current**
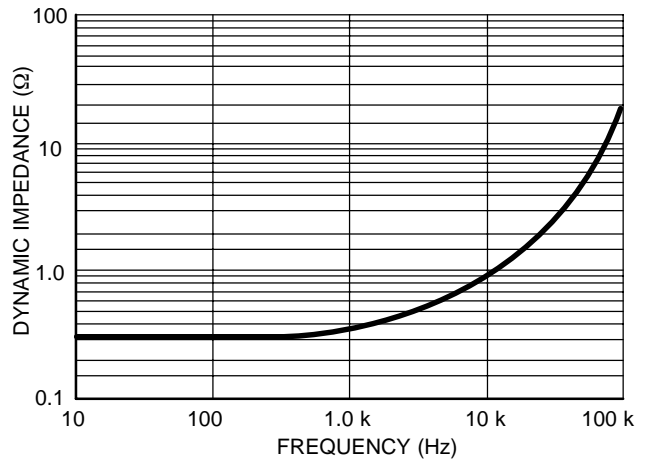

Figure 5. Forward Voltage vs. Forward Current
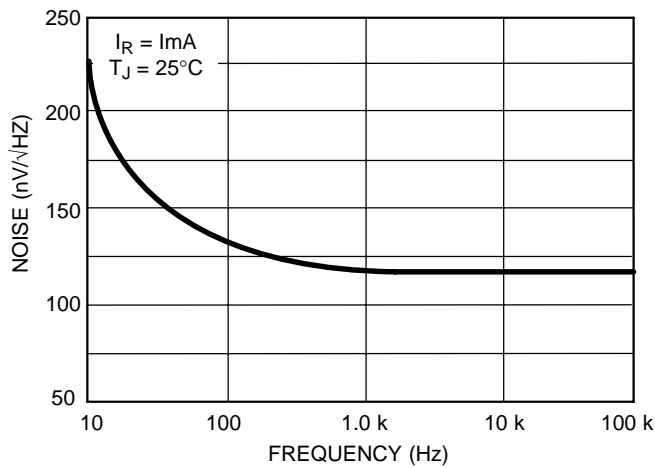

Figure 6. Dynamic Impedance vs. Frequency
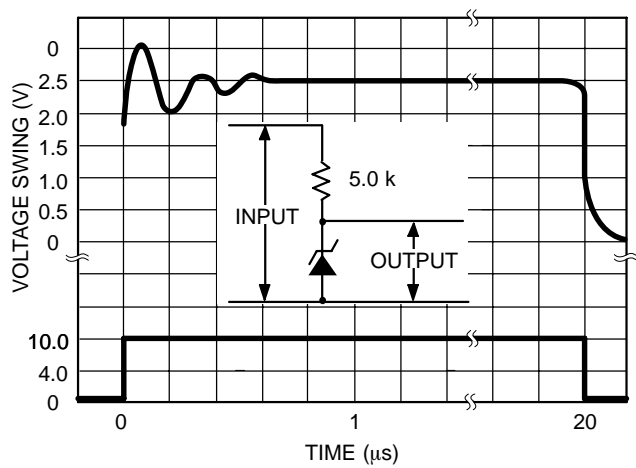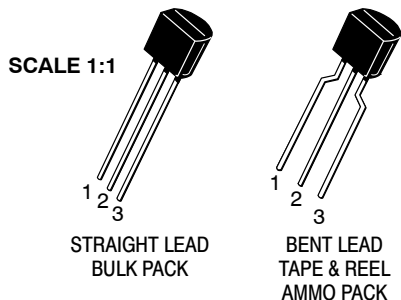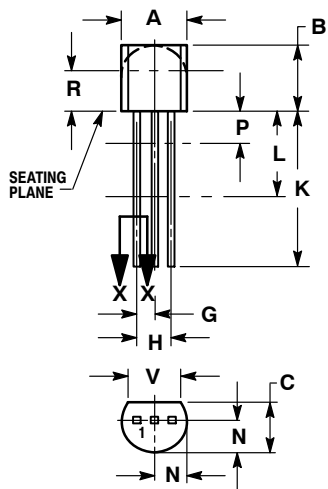

Figure 7. Zener Noise Voltage vs. Frequency

Figure 8. Response Time

** onsemi**
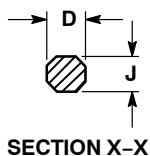
SCALE 1:1

TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

1
2
3
STRAIGHT LEAD
BULK PACK

1
2
3
BENT LEAD
TAPE & REEL
AMMO PACK

STRAIGHT LEAD
BULK PACK

SEATING
PLANE

SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

BENT LEAD
TAPE & REEL
AMMO PACK

SEATING
PLANE

SECTION X−X
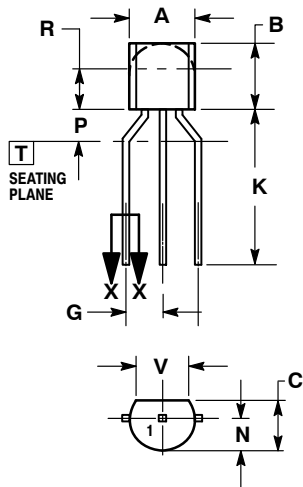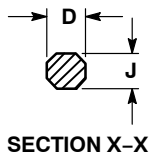
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

STYLE 1:
PIN 1. EMITTER
  2. BASE
  3. COLLECTOR

STYLE 2:
PIN 1. BASE
  2. EMITTER
  3. COLLECTOR

STYLE 3:
PIN 1. ANODE
  2. ANODE
  3. CATHODE

STYLE 4:
PIN 1. CATHODE
  2. CATHODE
  3. ANODE

STYLE 5:
PIN 1. DRAIN
  2. SOURCE
  3. GATE

STYLE 6:
PIN 1. GATE
  2. SOURCE & SUBSTRATE
  3. DRAIN

STYLE 7:
PIN 1. SOURCE
  2. DRAIN
  3. GATE

STYLE 8:
PIN 1. DRAIN
  2. GATE
  3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
  2. EMITTER
  3. BASE 2

STYLE 10:
PIN 1. CATHODE
  2. GATE
  3. ANODE

STYLE 11:
PIN 1. ANODE
  2. CATHODE & ANODE
  3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
  2. GATE
  3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
  2. GATE
  3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
  2. COLLECTOR
  3. BASE

STYLE 15:
PIN 1. ANODE 1
  2. CATHODE
  3. ANODE 2

STYLE 16:
PIN 1. ANODE
  2. GATE
  3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
  2. BASE
  3. EMITTER

STYLE 18:
PIN 1. ANODE
  2. CATHODE
  3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
  2. ANODE
  3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
  2. CATHODE
  3. ANODE

STYLE 21:
PIN 1. COLLECTOR
  2. EMITTER
  3. BASE

STYLE 22:
PIN 1. SOURCE
  2. GATE
  3. DRAIN

STYLE 23:
PIN 1. GATE
  2. SOURCE
  3. DRAIN

STYLE 24:
PIN 1. EMITTER
  2. COLLECTOR/ANODE
  3. CATHODE

STYLE 25:
PIN 1. MT 1
  2. GATE
  3. MT 2

STYLE 26:
PIN 1. V_{CC}
  2. GROUND 2
  3. OUTPUT

STYLE 27:
PIN 1. MT
  2. SUBSTRATE
  3. MT

STYLE 28:
PIN 1. CATHODE
  2. ANODE
  3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
  2. ANODE
  3. CATHODE

STYLE 30:
PIN 1. DRAIN
  2. GATE
  3. SOURCE

STYLE 31:
PIN 1. GATE
  2. DRAIN
  3. SOURCE

STYLE 32:
PIN 1. BASE
  2. COLLECTOR
  3. EMITTER

STYLE 33:
PIN 1. RETURN
  2. INPUT
  3. OUTPUT

STYLE 34:
PIN 1. INPUT
  2. GROUND
  3. LOGIC

STYLE 35:
PIN 1. GATE
  2. COLLECTOR
  3. EMITTER

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TO–92 (TO–226)		PAGE 2 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011
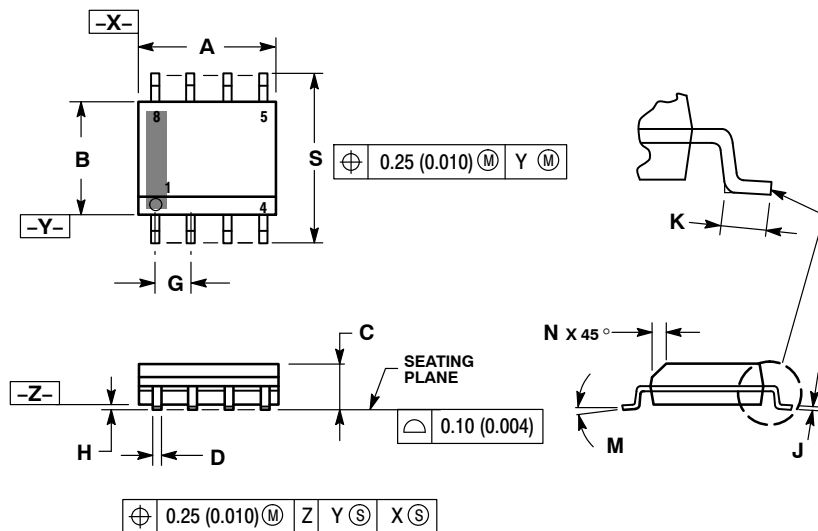
8
1
SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

$\bigoplus$ 0.25 (0.010) Ⓜ Y Ⓜ

$\bigoplus$ 0.25 (0.010) Ⓜ Z Y Ⓢ X Ⓢ

SEATING PLANE

$\triangle$ 0.10 (0.004)

N X 45°

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*

$\dfrac{1.52}{0.060}$

$\dfrac{7.0}{0.275}$ $\dfrac{4.0}{0.155}$

$\dfrac{0.6}{0.024}$ $\dfrac{1.270}{0.050}$

SCALE 6:1 $\left(\dfrac{mm}{inches}\right)$

IC

IC (Pb−Free)

Discrete

Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	
DESCRIPTION:	SOIC−8 NB	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−8 NB		PAGE 2 OF 2

ADDITIONAL INFORMATION

◊