NCV4250-2C

Low Dropout Voltage Tracking Regulator

The NCV4250−2C is a monolithic integrated low dropout tracking voltage regulator designed to provide a buffered output voltage that closely tracks the reference input voltage. The part can be used in automotive applications with remote sensors or any situation where it is necessary to isolate the output of the other regulator. The NCV4250−2C also enables the user to bestow a quick upgrade to their module when added current is needed and the existing regulator cannot provide.

Features

- Up to 50 mA Source Capability
- Low Output Tracking Tolerance
- Low Dropout (typ. 120 mV @ 10 mA)
- Low Quiescent Current in Stand−by Mode
- Wide Input Voltage Operating Range
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage and Reverse Bias Voltage
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Off the Module Loads (e.g. Sensors Power Supply)

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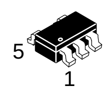
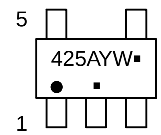
MARKING DIAGRAM



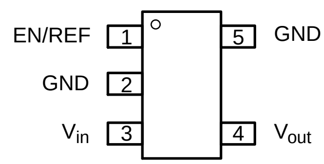
TSOP−5
CASE 483



425 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

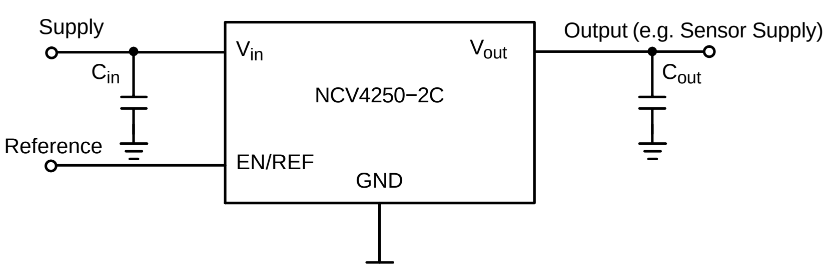


Figure 1. Applications Circuit

October, 2017 − Rev. 0

Publication Order Number:
NCV4250−2C/D

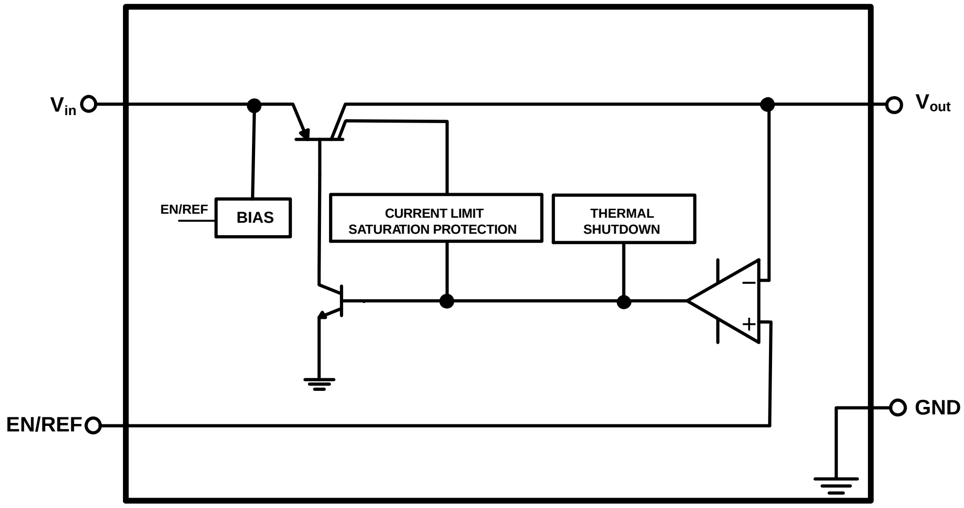


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin Name	Description
1	EN/REF	Enable / Reference. Connect the reference to this pin. A low signal disables the IC; a high signal switches it on. The reference voltage can be connected directly or by a voltage divider for lower output voltages.
2	GND	Power Supply Ground.
3	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
4	V_{out}	Tracker Output Voltage. Connect 1 μF capacitor with ESR < 3 Ω to ground.
5	GND	Power Supply Ground.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC (Note 1) DC	V_{in}	−42	45	V
Output Voltage	V_{out}	−1	40	V
Enable / Reference Input Voltage DC DC	$V_{EN/REF}$	−0.3	40	V
Maximum Junction Temperature	$T_{J(max)}$	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−3	3	kV

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50 mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP−5			°C/W
Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	136	
Thermal Resistance, Junction−to−Lead 2 (Note 4)	$R_{\Psi JL2}$	49	

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}	4	40	V
Enable / Reference Input Voltage	$V_{EN/REF}$	2.5	36	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{in} = 13.5 V, $V_{EN/REF}$ > = 2.5 V, C_{in} = 0.1 μF, C_{out} = 1 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Note 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage Tracking Accuracy	V_{in} = 6 V to 16 V, I_{out} = 1 mA to 10 mA	ΔV_{out}	−5	−	5	mV
Output Voltage Tracking Accuracy	V_{in} = 6 V to 28 V, I_{out} = 1 mA to 50 mA	ΔV_{out}	−25	−	25	mV
Output Voltage Tracking Accuracy	V_{in} = 6 V to 40 V, I_{out} = 1 mA to 10 mA	ΔV_{out}	−25	−	25	mV
Line Regulation	V_{in} = 6 V to 40 V, I_{out} = 10 mA	Reg_{line}	−10	−	10	mV
Load Regulation	I_{out} = 1 mA to 30 mA	Reg_{load}	−15	−	15	mV
Dropout Voltage (Note 6)	I_{out} = 10 mA, $V_{EN/REF}$ > 4 V	V_{DO}	−	120	300	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current Stand−by Mode	$V_{EN/REF}$ <= 0.4 V, T_J < 85°C	I_{DIS}	−	14	20	μA
Quiescent Current, $I_q = I_{in} - I_{out}$	 I_{out} <= 1 mA I_{out} <= 30 mA	I_q	 − −	 75 0.6	 150 3	 μA mA
Current Consumption Dropout Region, $I_q = I_{in} - I_{out}$	$V_{EN/REF} = V_{in}$ = 5 V, I_{out} = 0 mA	I_q	−	0.1	1	mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = ($V_{EN/REF}$ – 0.1 V)	I_{LIM}	51	90	120	mA
REVERSE CURRENT PROTECTION						
Reverse Current	V_{in} = 0 V, V_{out} = 16 V, $V_{EN/REF}$ = 5 V	I_{out_rev}	−5	−0.1	−	mA
Reverse Current at Negative Input Voltage	V_{in} = −16 V, V_{out} = 0 V, $V_{EN/REF}$ = 5 V	I_{in_rev}	−5	−0.02	−	mA
PSRR						
Power Supply Ripple Rejection	f = 100 Hz, 1 V_{pp}	PSRR	−	70	−	dB
ENABLE						
Enable / Reference Input Threshold Voltage Logic Low Logic High	 V_{out} = 0 V; | $V_{out} - V_{EN/REF}$ | < 25 mV	$V_{th(EN/REF)}$	 − 2.5	 − −	 0.4 36	V
Enable / Reference Input Current	$V_{EN/REF}$ = 5 V	$I_{EN/REF}$	−	0.1	0.5	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 7)		T_{SD}	151	175	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V.
7. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS $V_{EN/REF}$ = 5 V (unless otherwise noted)

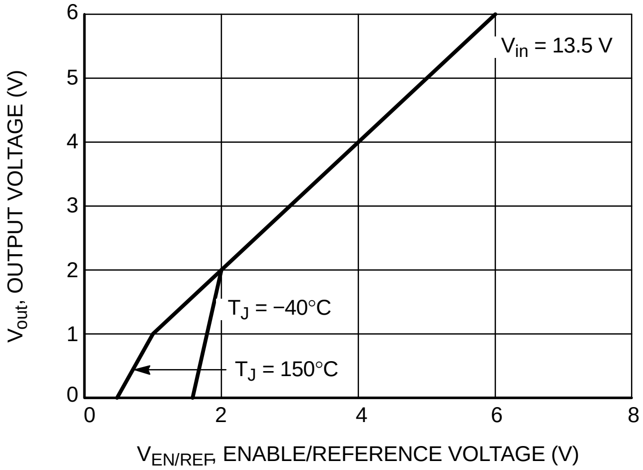


Figure 3. Output Voltage V_{out} vs. Reference Voltage $V_{EN/REF}$

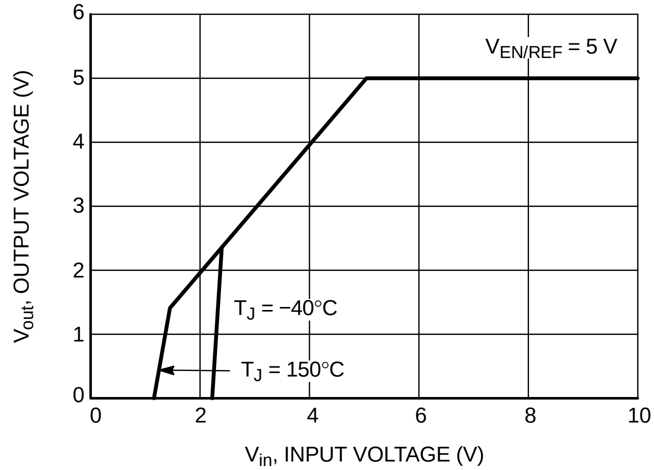


Figure 4. Output Voltage V_{out} vs. Input Voltage V_{in}

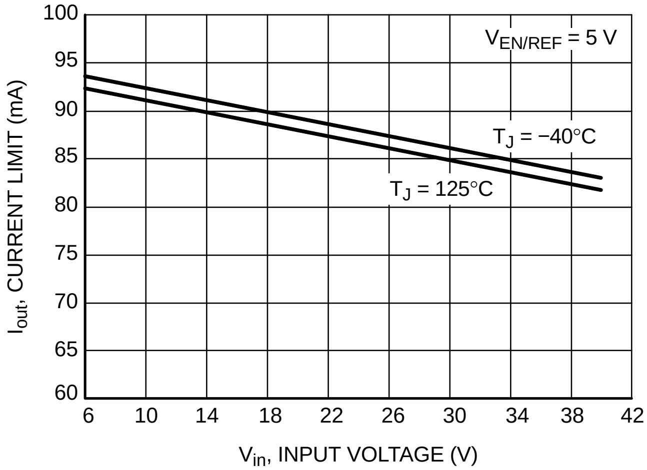


Figure 5. Maximum Output Current I_{out} vs. Input Voltage V_{in}

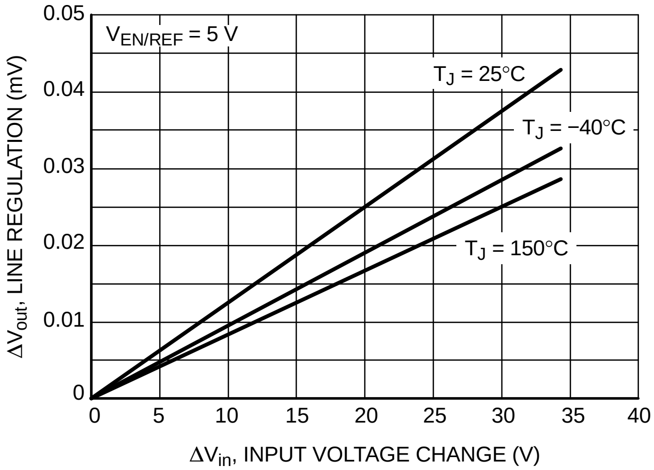


Figure 6. Line Regulation ΔV_{out} vs. Input Voltage Change ΔV_{in}

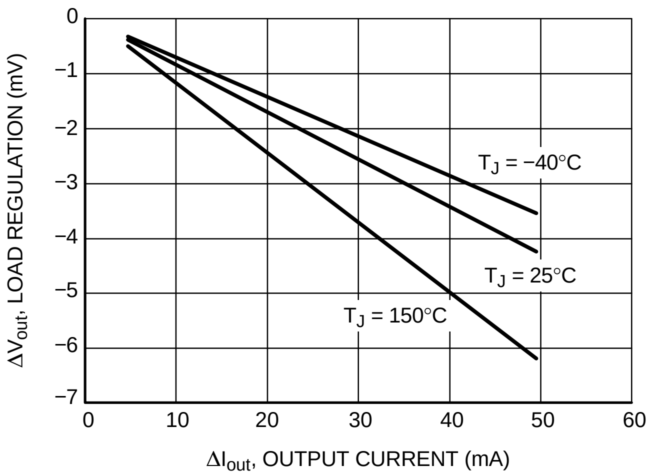


Figure 7. Load Regulation ΔV_{out} vs. Output Current Change ΔI_{out}

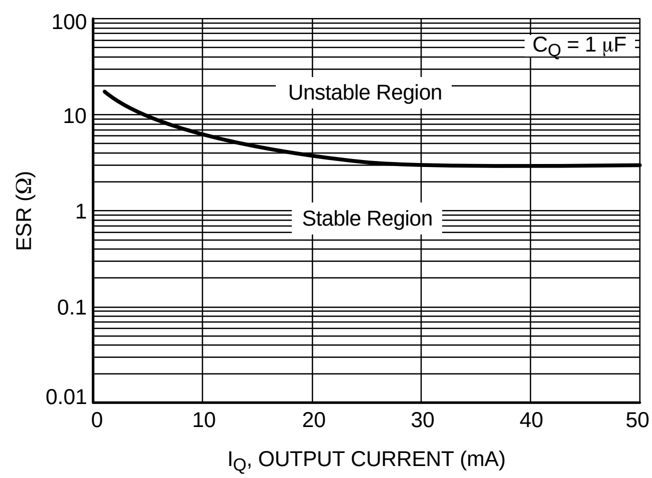


Figure 8. Output Capacitor Series Resistor ESR vs. Output Current I_{out}

TYPICAL CHARACTERISTICS $V_{EN/REF}$ = 5 V (unless otherwise noted)

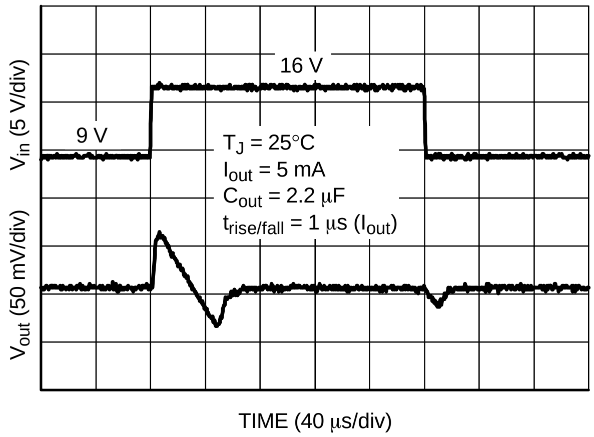


Figure 9. Line Transient Response

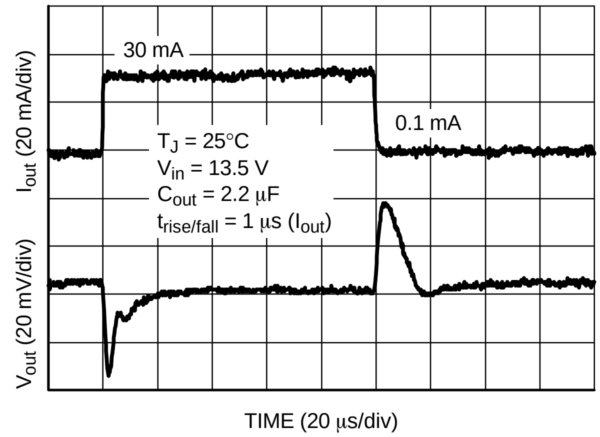


Figure 10. Load Transient Response

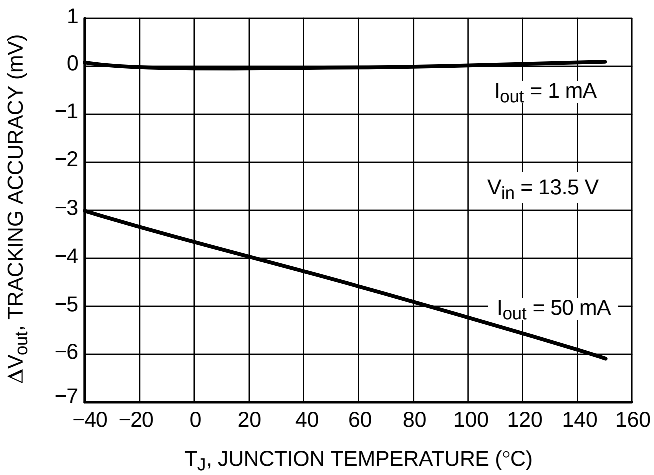


Figure 11. Tracking Accuracy ΔV_Q vs. Junction Temperature T_J

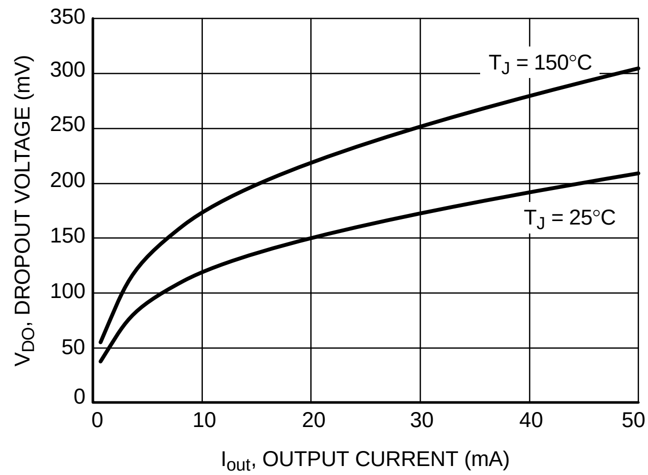


Figure 12. Dropout Voltage V_{DR} vs. Output Current I_{out}

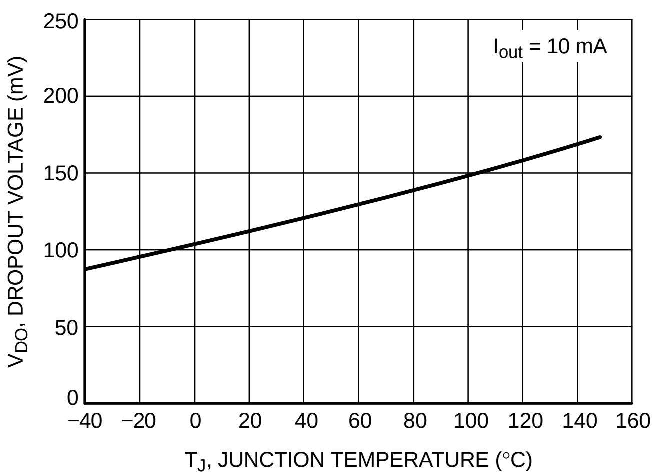


Figure 13. Dropout Voltage V_{DR} vs. Junction Temperature T_J

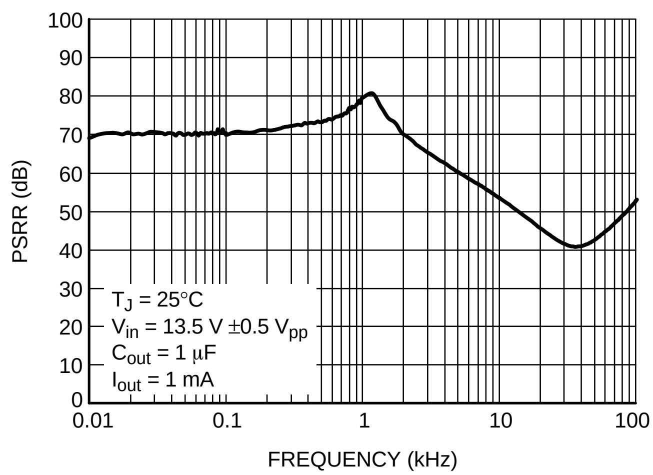


Figure 14. Power Supply Ripple Rejection PSRR

TYPICAL CHARACTERISTICS $V_{EN/REF}$ = 5 V (unless otherwise noted)

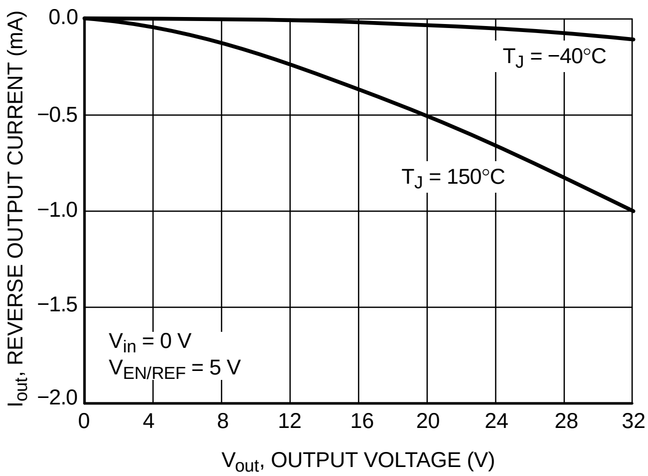


Figure 15. Reverse Output Current I_{out} vs. Output Voltage V_{out}

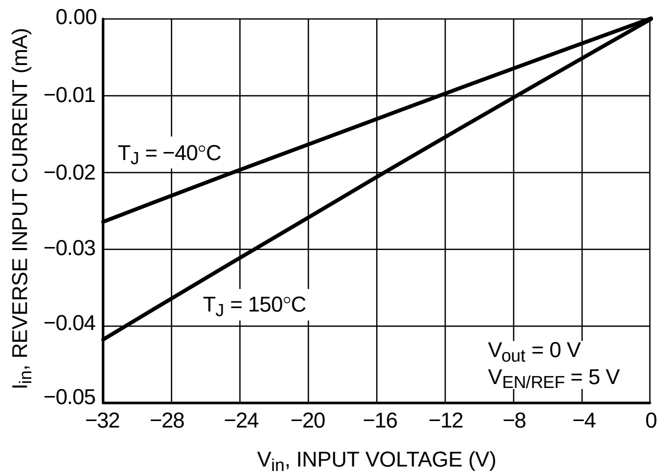


Figure 16. Reverse Current I_{in} vs. Input Voltage V_{in}

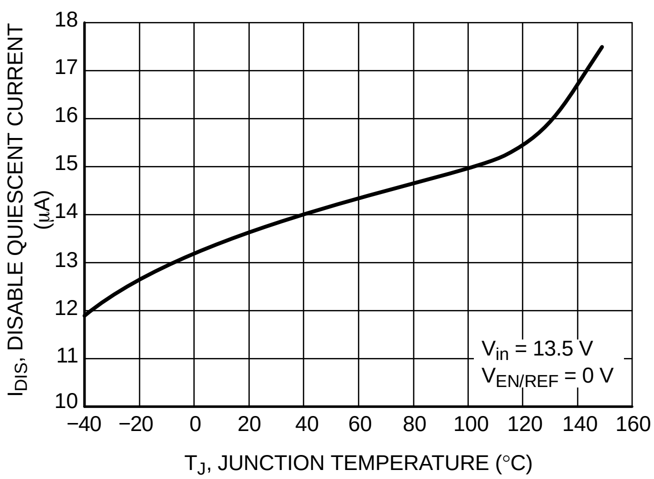


Figure 17. Disable Current Consumption I_q vs. Junction Temperature T_J

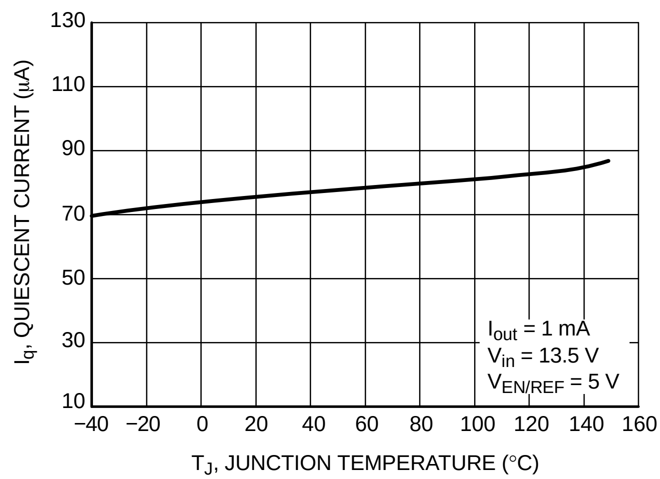


Figure 18. Current Consumption I_q vs. Junction Temperature T_J

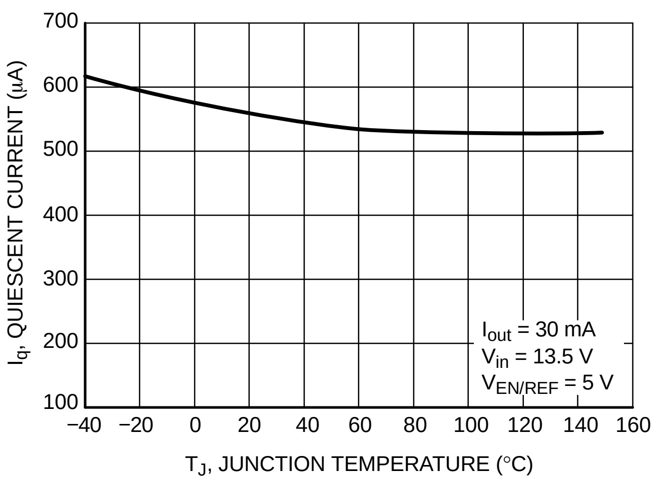


Figure 19. Current Consumption I_q vs. Junction Temperature T_J

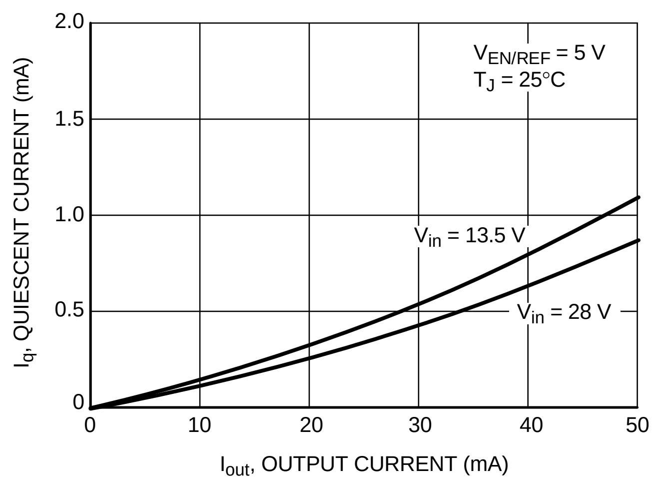


Figure 20. Current Consumption I_q vs. Output Current I_{out}

TYPICAL CHARACTERISTICS $V_{EN/REF}$ = 5 V (unless otherwise noted)

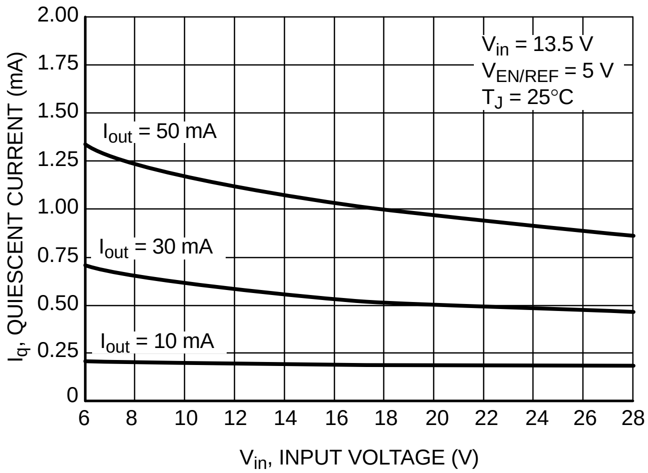


Figure 21. Current Consumption I_q vs. Input Voltage V_{in}

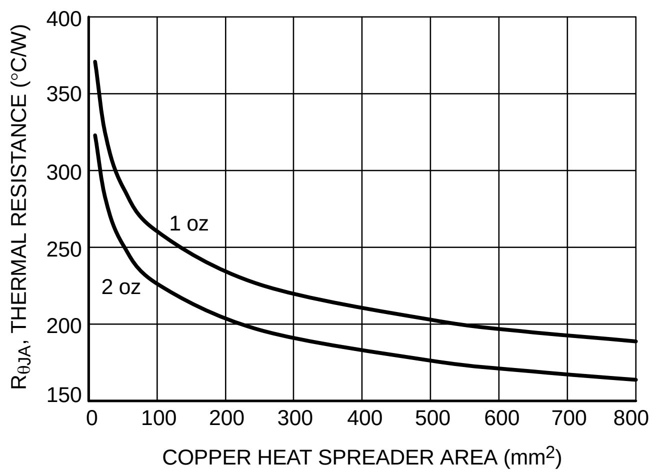


Figure 22. Thermal Resistance $R_{\theta JA}$ vs. Copper Spreader Area

APPLICATIONS INFORMATION

The NCV4250−2C tracking regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 3 to Figure 22.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV4250−2C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The output capacitor for the NCV4250C−2C is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst−case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to −40°C, a capacitor rated at that temperature must be used.

Tracking Regulator

The output voltage V_{out} is controlled by comparing it to the voltage applied at pin EN/REF and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_{out}, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of over temperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package.

The maximum output current is decreased at high input voltages.

The over temperature protection circuit prevents the IC from immediate destruction under fault conditions (e. g. Output continuously short−circuited) by reducing the output current. A thermal balance below 200°C junction temperature is established. Please note that a junction temperature above 150°C is outside the maximum ratings and reduces the IC lifetime.

The NCV4250−2C allows a negative supply voltage. However, several small currents are flowing into the IC. For details see electrical characteristics table and typical performance graphs. The thermal protection circuit is not operating during reverse polarity condition.

Thermal Considerations

As power in the NCV4250−2C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV4250−2C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV4250−2C can handle is given by:

$$P_{D(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV4250−2C soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 0.65 W when the ambient temperature (T_A) is 25°C. See Figure 22 for R_{thJA} versus PCB area. The power dissipated by the NCV4250−2C can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

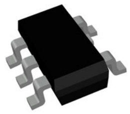
Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV4250−2C and make traces as short as possible.

ORDERING INFORMATION

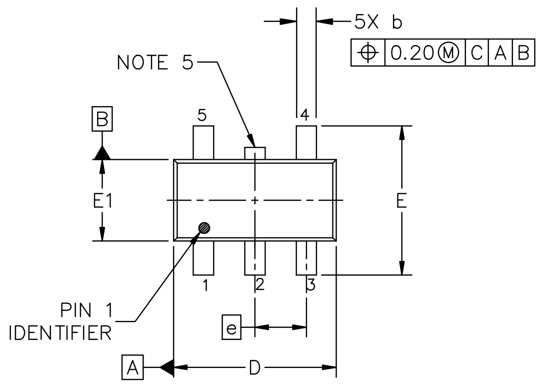
Device	Package	Shipping†
NCV4250−2CSNT1G	TSOP−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

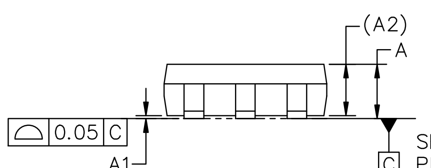
DATE 01 APR 2024



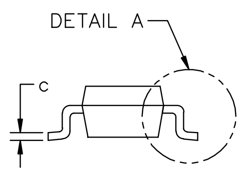
TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

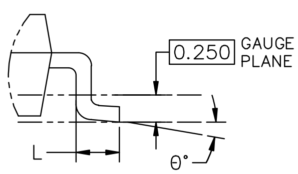


SIDE VIEW

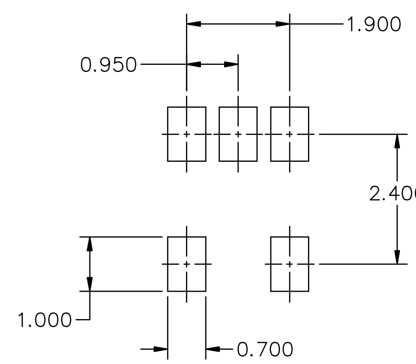


END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



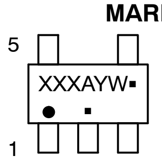
DETAIL "A"
SCALE 2:1



RECOMMENDED MOUNTING FOOTPRINT*

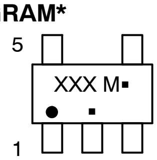
* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales