

LDO Linear Regulator – DELAY, Adjustable RESET, Sense Output, Micropower

5.0 V, 150 mA

NCV4279C

The NCV4279C is a 5.0 V precision micropower voltage regulator with an output current capability of 150 mA.

The output voltage is accurate within $\pm 2.0\%$ with a maximum dropout voltage of 0.5 V at 100 mA. Low quiescent current is a feature drawing only 125 μA with a 1.0 mA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active reset output RO with delay and a SI/SO monitor which can be used to provide an early warning signal to the microprocessor of a potential impending reset signal. The use of the SI/SO monitor allows the microprocessor to finish any signal processing before the reset shuts the microprocessor down.

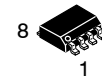
The active Reset circuit operates correctly at an output voltage as low as 1.0 V. The Reset function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to the R_{ADJ} lead. The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

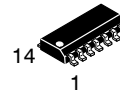
If the application requires pullup resistors at the logic outputs Reset and Sense Out, the NCV4269C with integrated resistors can be used.

Features

- 5.0 V $\pm 2.0\%$ Output
- Low 125 μA Quiescent Current
- Active Reset Output Low Down to $V_Q = 1.0$ V
- Adjustable Reset Threshold
- 150 mA Output Current Capability
- Fault Protection
 - ◆ +60 V Peak Transient Voltage
 - ◆ -40 V Reverse Voltage
 - ◆ Short Circuit
 - ◆ Thermal Overload
- Early Warning through SI/SO Leads
- Internally Fused Leads in SO-14 Package
- Very Low Dropout Voltage
- Electrical Parameters Guaranteed Over Entire Temperature Range
- AEC-Q100 Grade 1 Qualified and PPAP Capable
- These are Pb-Free Devices

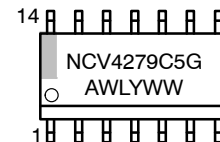
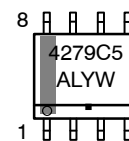


SO-8
D1 SUFFIX
CASE 751



SO-14
D2 SUFFIX
CASE 751A

MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G = PB-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 12.

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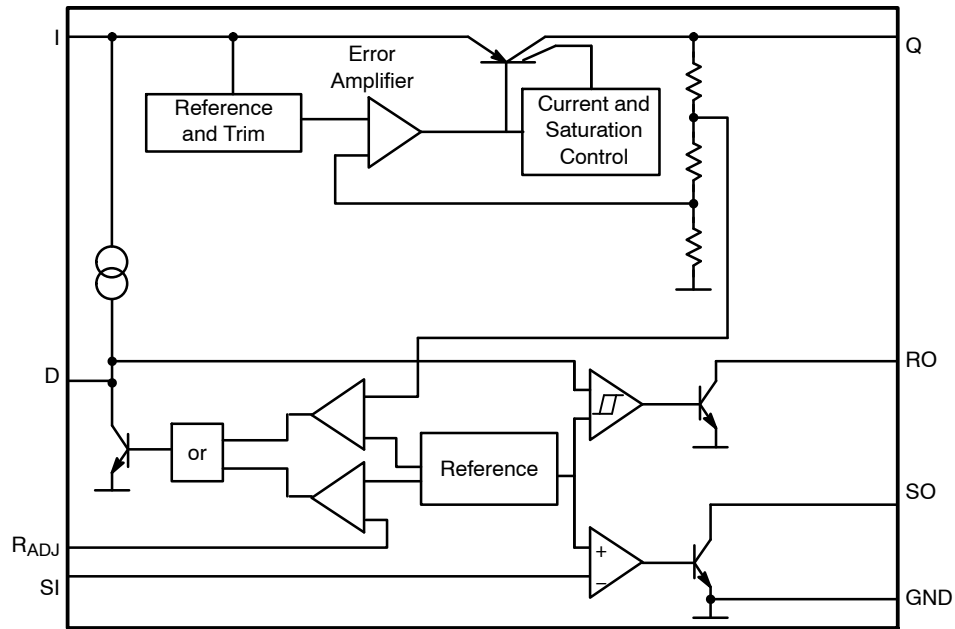
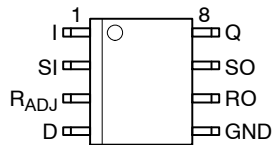
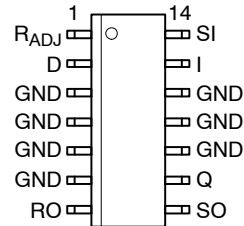


Figure 1. Block Diagram

PIN CONNECTIONS



SO-8



SO-14

PACKAGE PIN DESCRIPTION

Pin Symbol	Package Pin Number		Function
	SO-8	SO-14	
R _{ADJ}	3	1	Reset Threshold Adjust; if not used to connect to GND.
D	4	2	Reset Delay; To Set Time Delay, Connect to GND with a Capacitor
GND	5	3, 4, 5, 6, 10, 11, 12	Ground
RO	6	7	Reset Output; This is an Open-Collector Output. Leave Open if Not Used.
SO	7	8	Sense Output; This is an Open-Collector Output. If not used, keep open.
Q	8	9	5 V Output; Connect to GND with a 10 μ F Capacitor, ESR < 2.5 Ω .
I	1	13	Input; Connect to GND Directly at the IC with a Ceramic Capacitor.
SI	2	14	Sense Input; If not used, Connect to Q.

MAXIMUM RATINGS ($T_J = -40^{\circ}\text{C}$ to 150°C)

Symbol	Parameter	Min	Max	Unit
V_I I_I	Input to Regulator	-40 Internally Limited	45 Internally Limited	V
V_I	Input Peak Transient Voltage (Note 3)	-	60	V
V_{SI} I_{SI}	Sense Input	-40 -1	45 1	V mA
V_{RADJ} I_{RADJ}	Reset Threshold Adjust	-0.3 -10	7 10	V mA
V_D I_D	Reset Delay	-0.3 Internally Limited	7 Internally Limited	V
I_q	Ground	50	-	mA
V_{RO} I_{RO}	Reset Output	-0.3 Internally Limited	7 Internally Limited	V
V_{SO} I_{SO}	Sense Output	-0.3 Internally Limited	7 Internally Limited	V
V_Q I_Q	Regulated Output	-0.5 -10	7 -	V mA
T_J T_{STG}	Junction Temperature Storage Temperature	- -50	150 150	$^{\circ}\text{C}$ $^{\circ}\text{C}$
V_I T_J	Input Voltage Operating Range Junction Temperature Operating Range	- -40	45 150	V $^{\circ}\text{C}$

LEAD TEMPERATURE SOLDERING AND MSL

Symbol	Parameter	Value	Unit
MSL	MSL, 8-Lead, 14-Lead, LS Temperature 260°C Peak (Note 4)	1	-

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and exceeds the following ratings:

Human Body Model (HBM) ≤ 4.0 kV per AEC-Q100-002.

Machine Model (MM) ≤ 200 V per AEC-Q100-003.

2. Latchup tested per AEC-Q100-004.

3. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750-1.

4. Lead free: 60-150 Sec above 217°C , 40 Sec Max at Peak, 265°C Peak.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Values)	Unit
SO-8 Package (Note 5)		
Junction-to-Pin 6 ($\Psi - \text{JL6}, \Psi_{L6}$)	63.2	$^{\circ}\text{C/W}$
Junction-to-Ambient Thermal Resistance ($R_{\theta JA}, \theta_{JA}$)	167	$^{\circ}\text{C/W}$
SO-14 Package (Note 5)		
Junction-to-Pin 4 ($\Psi - \text{JL4}, \Psi_{L4}$)	18.4	$^{\circ}\text{C/W}$
Junction-to-Ambient Thermal Resistance ($R_{\theta JA}, \theta_{JA}$)	114	$^{\circ}\text{C/W}$

5. 2 oz copper, 100 mm² copper area, 1.5 mm thick FR4

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ELECTRICAL CHARACTERISTICS ($T_J = -40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, $V_I = 13.5\text{ V}$ unless otherwise specified)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
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REGULATOR

V_Q	Output Voltage	$1\text{ mA} \leq I_Q \leq 100\text{ mA}$; $6\text{ V} \leq V_I \leq 16\text{ V}$	4.90	5.00	5.10	V
I_Q	Current Limit	–	150	430	500	mA
I_q	Current Consumption; $I_q = I_I - I_Q$	$I_Q = 1\text{ mA}$, RO, SO High	–	125	250	μA
I_q	Current Consumption; $I_q = I_I - I_Q$	$I_Q = 1\text{ mA}$, RO High, SO Low (Note 6)	–	560	650	μA
I_q	Current Consumption; $I_q = I_I - I_Q$	$I_Q = 10\text{ mA}$, RO, SO High	–	230	450	μA
I_q	Current Consumption; $I_q = I_I - I_Q$	$I_Q = 50\text{ mA}$, RO, SO High	–	0.9	3.0	mA
V_{dr}	Dropout Voltage	$I_Q = 100\text{ mA}$ (Note 7)	–	0.25	0.5	V
ΔV_Q	Load Regulation	$I_Q = 5\text{ mA}$ to 100 mA	–	1	20	mV
ΔV_Q	Line Regulation	$V_I = 6\text{ V}$ to 26 V ; $I_Q = 1\text{ mA}$	–	1	30	mV

RESET GENERATOR

V_{RT}	Reset Switching Threshold	–	4.50	4.65	4.80	V
$V_{RADJ,TH}$	Reset Adjust Switching Threshold	$V_Q > 3.5\text{ V}$	1.26	1.35	1.44	V
$V_{RO,SAT}$	Reset Output Saturation Voltage	$V_Q < V_{RT}$, $R_{RO} = 20\text{ k}\Omega$	–	0.03	0.4	V
V_{UD}	Upper Delay Switching Threshold	–	1.4	1.8	2.2	V
V_{LD}	Lower Delay Switching Threshold	–	0.3	0.45	0.60	V
$V_{D,SAT}$	Saturation Voltage on Delay Capacitor	$V_Q < V_{RT}$	–	–	0.1	V
$I_{D,C}$	Charge Current	$V_D = 1\text{ V}$	3.0	6.5	9.5	μA
t_d	Delay Time L \rightarrow H	$C_D = 100\text{ nF}$	17	28	–	ms
t_{RR}	Delay Time H \rightarrow L	$C_D = 100\text{ nF}$	–	1.5	–	μs

INPUT VOLTAGE SENSE

$V_{SI,High}$	Sense Threshold High	–	1.24	1.31	1.38	V
$V_{SI,Low}$	Sense Threshold Low	–	1.16	1.20	1.28	V
$V_{SO,Low}$	Sense Output Saturation Voltage	$V_{SI} < 1.20\text{ V}$; $V_Q > 3\text{ V}$; $R_{SO} = 20\text{ k}\Omega$	–	0.03	0.4	V
I_{SI}	Sense Input Current	–	–1.0	0.1	1.0	μA

THERMAL SHUTDOWN

T_{SD}	Thermal Shutdown Temperature (Note 8)	$I_{OUT} = 1\text{ mA}$	150	–	200	$^{\circ}\text{C}$
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Including $20\text{ k}\Omega$ external SO pull-up resistor current.

7. Dropout voltage = $V_I - V_Q$ measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.

8. Values based on design and/or characterization.

The diagram consists of four vertically stacked waveforms sharing a common time axis t .

- Top waveform (V_I):** Input voltage. It shows a ramp-up, a long plateau, a sharp drop (voltage dip), a recovery ramp, a long plateau, a sharp spike (secondary spike), and a final plateau.
- Second waveform (V_Q):** Gate voltage. It follows the input voltage with a delay t_d during the initial ramp-up. It shows a recovery ramp after the voltage dip, a recovery ramp after the secondary spike, and a recovery ramp after the overload event. The recovery time after the secondary spike is labeled t_{RR} and is noted as $< t_{RR}$.
- Third waveform (V_D):** Drain voltage. It shows a ramp-up, a plateau, a sharp drop during the voltage dip, a recovery ramp, a plateau, a sharp drop during the secondary spike, a recovery ramp, a plateau, a sharp drop during the overload event, and a recovery ramp. The recovery time after the secondary spike is labeled t_{RR} . The relationship $\frac{dV}{dt} = \frac{I_D}{C_D}$ is indicated for the recovery ramps.
- Bottom waveform (V_{RO}):** Output voltage. It shows a ramp-up, a plateau, a drop to $V_{RO,SAT}$ during the voltage dip, a recovery ramp, a plateau, a drop to $V_{RO,SAT}$ during the secondary spike, a recovery ramp, a plateau, a drop to $V_{RO,SAT}$ during the overload event, and a recovery ramp.

Labels at the bottom indicate the fault conditions corresponding to the events in the waveforms:

- Power-on-Reset
- Thermal Shutdown
- Voltage Dip at Input
- Undervoltage
- Secondary Spike
- Overload at Output

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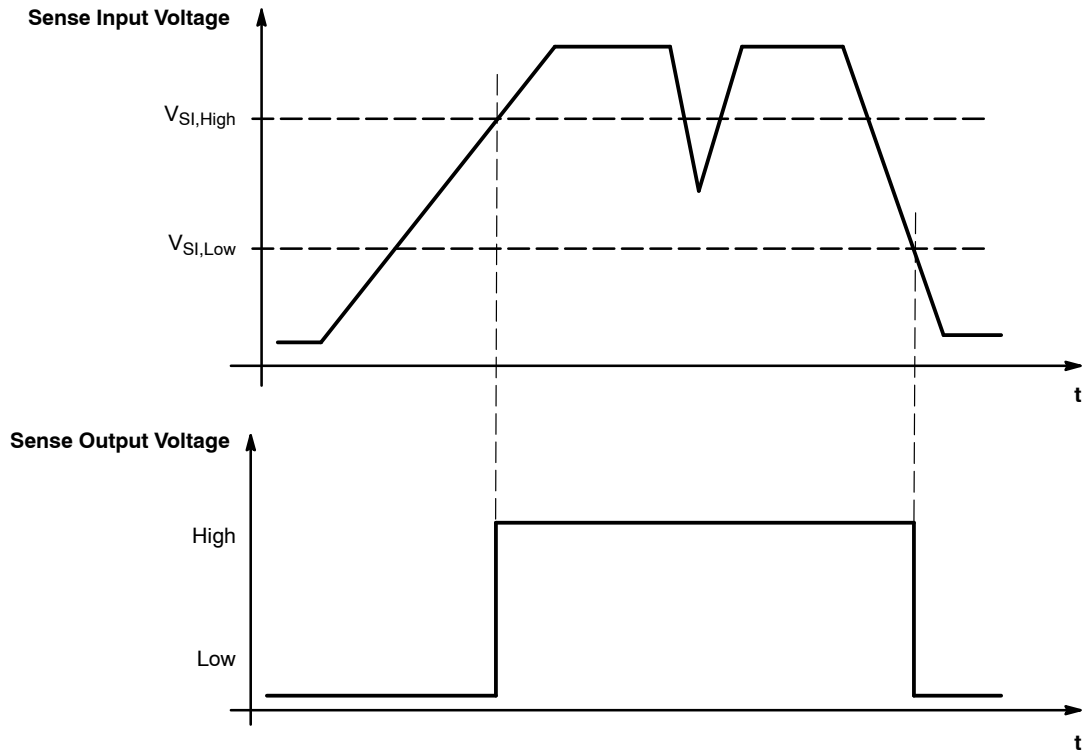


Figure 4. Sense Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

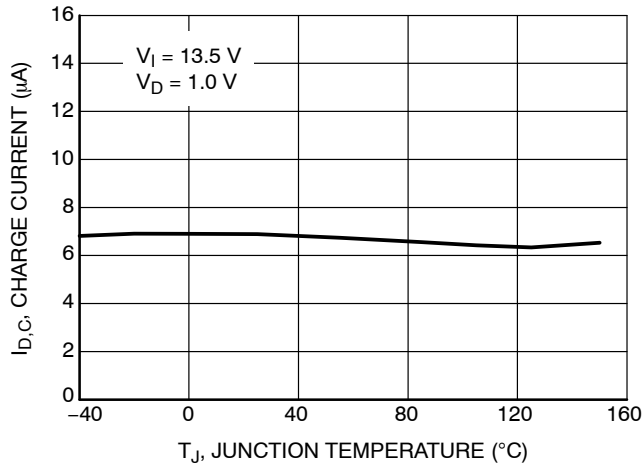


Figure 5. Charge Current $I_{D,C}$ vs. Temperature T_J

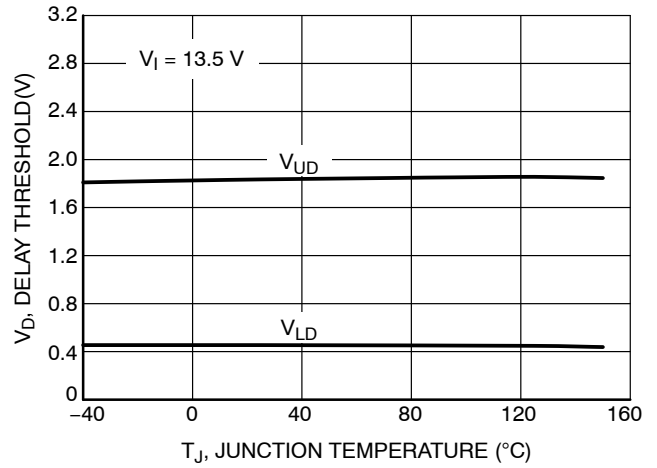


Figure 6. Switching Voltage V_{UD} and V_{LD} vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

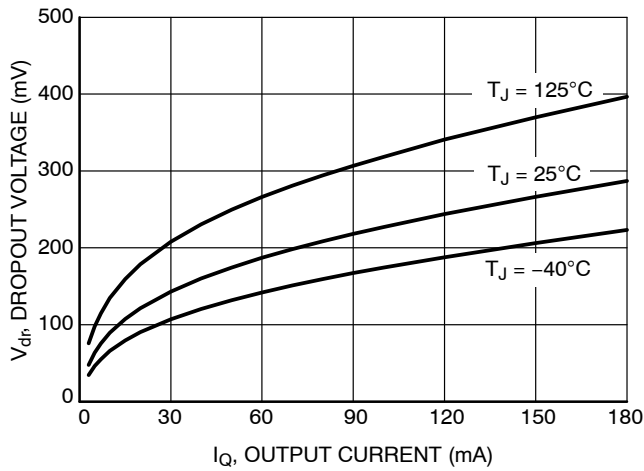


Figure 7. Drop Voltage V_{dr} vs. Output Current I_Q

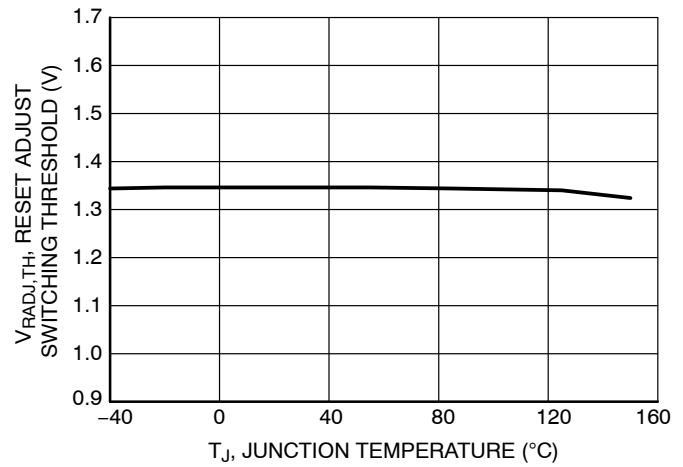


Figure 8. Reset Adjust Switching Threshold, $V_{RADJ,TH}$ vs. Temperature T_J

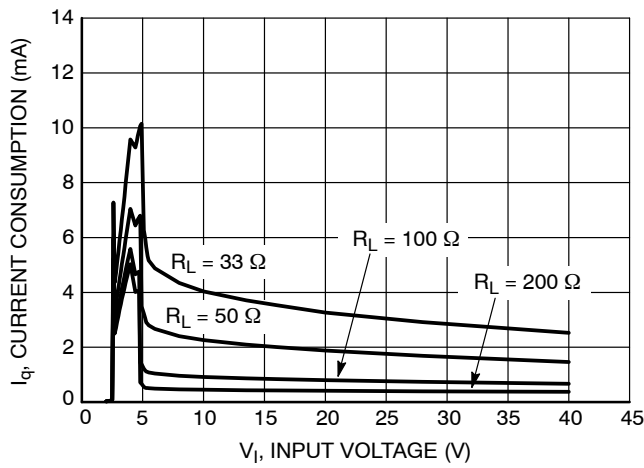


Figure 9. Current Consumption I_Q vs. Input Voltage V_I

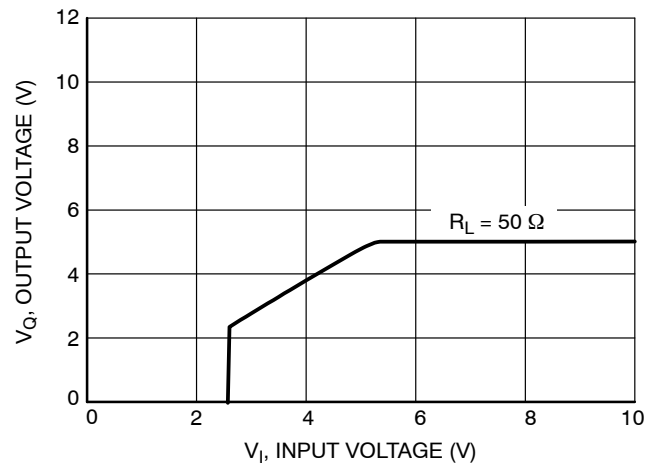


Figure 10. Output Voltage V_Q vs. Input Voltage V_I

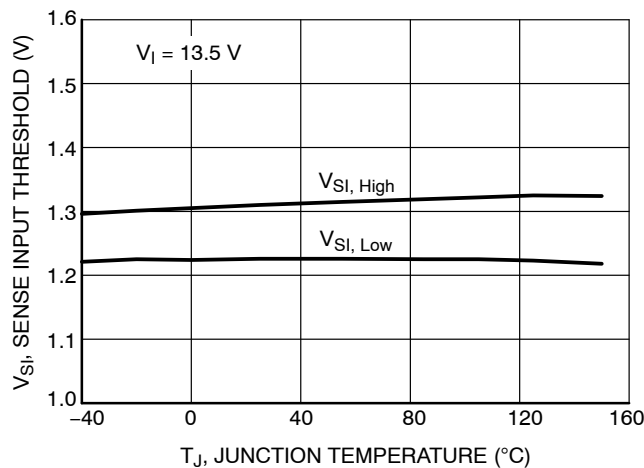


Figure 11. Sense Threshold V_{Sl} vs. Temperature T_J

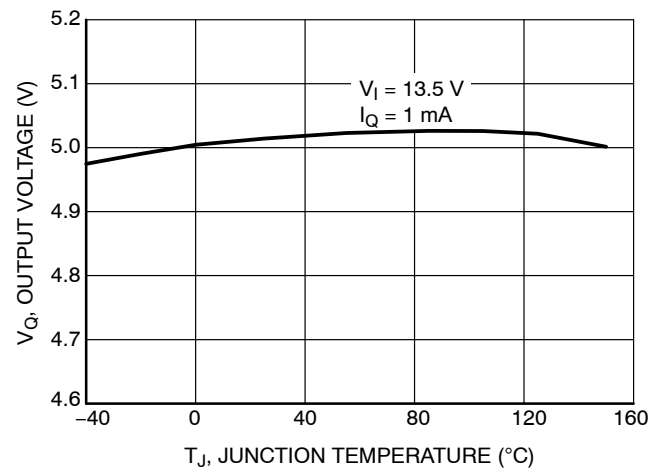


Figure 12. Output Voltage V_Q vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

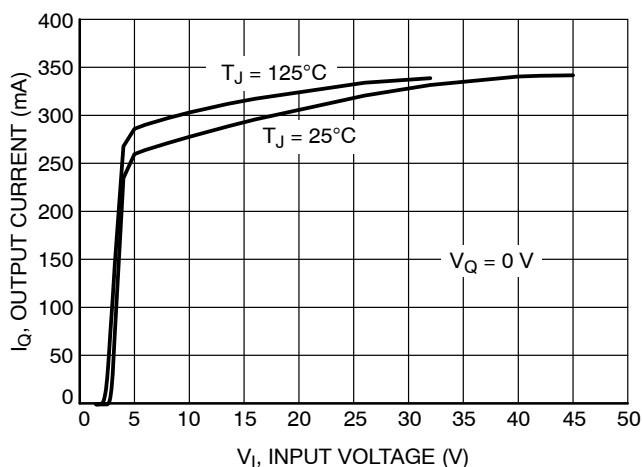


Figure 13. Output Current I_Q vs. Input Voltage V_I

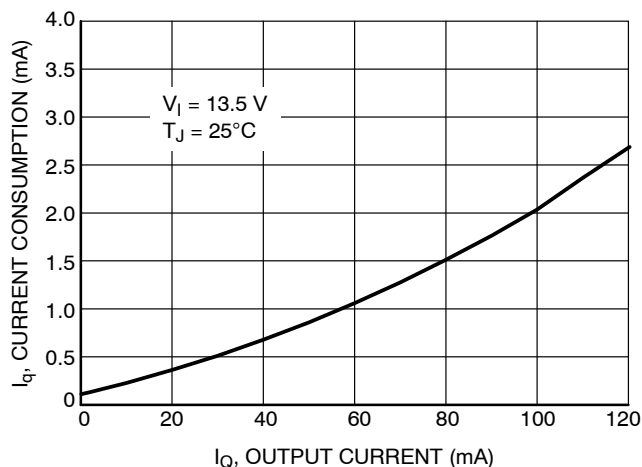


Figure 14. Current Consumption I_q vs. Output Current I_Q

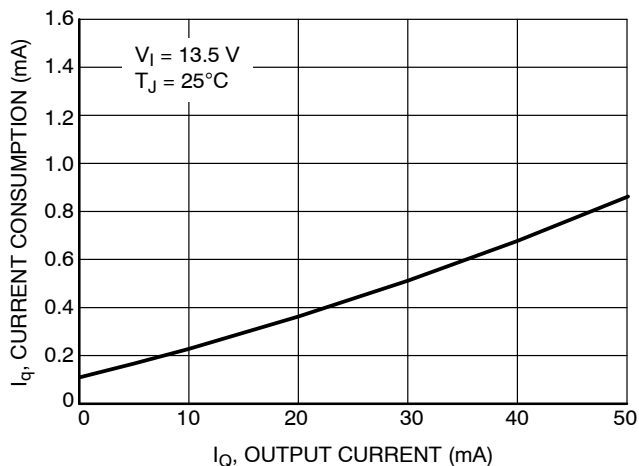


Figure 15. Current Consumption I_q vs. Output Current I_Q

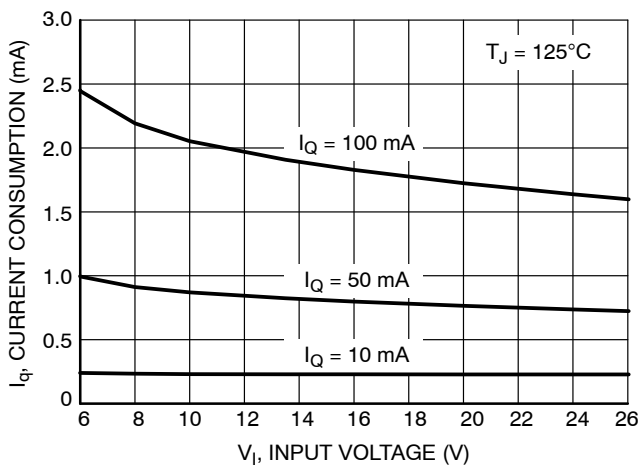


Figure 16. Quiescent Current I_q vs. Input Voltage V_I

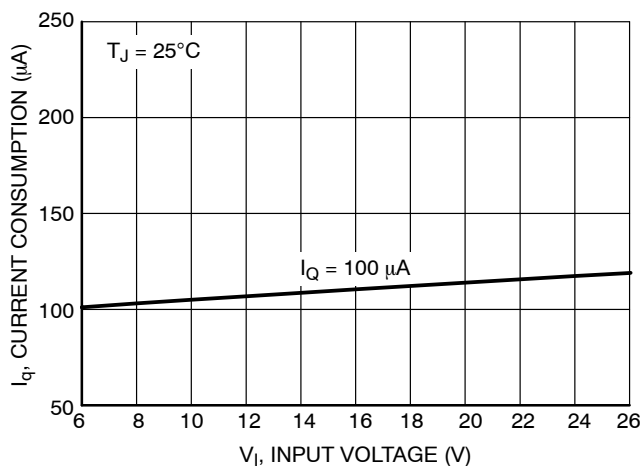


Figure 17. Quiescent Current I_q vs. Input Voltage V_I

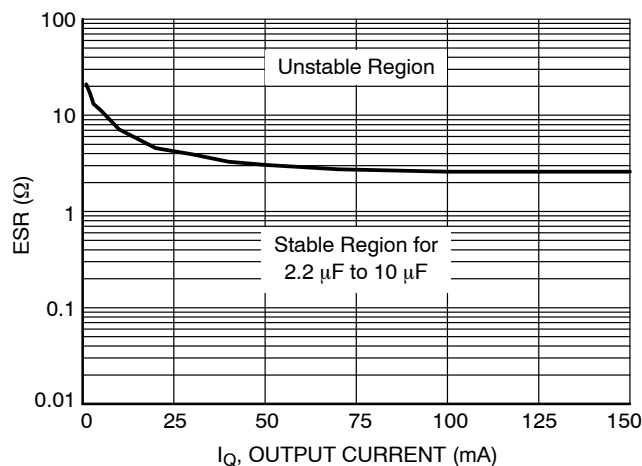


Figure 18. Output Stability, Capacitance ESR vs. Output Load Current

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TYPICAL THERMAL CHARACTERISTICS (continued)

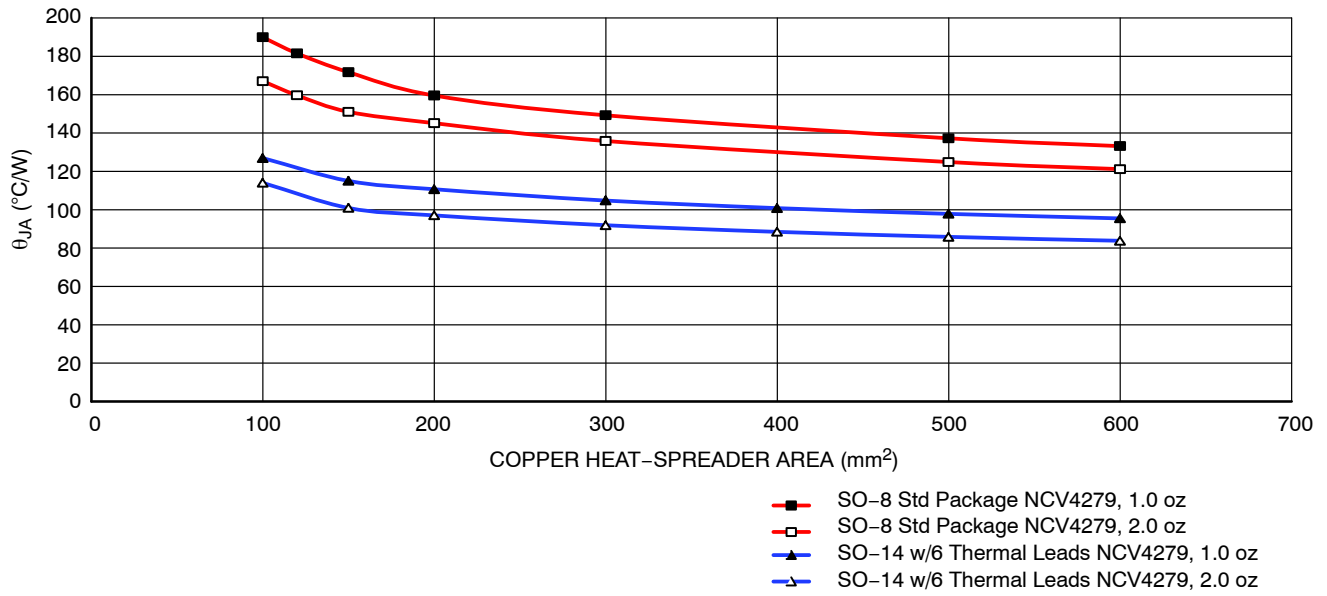


Figure 19. Junction-to-Ambient Thermal Resistance (θ_{JA}) vs. Heat Spreader Area

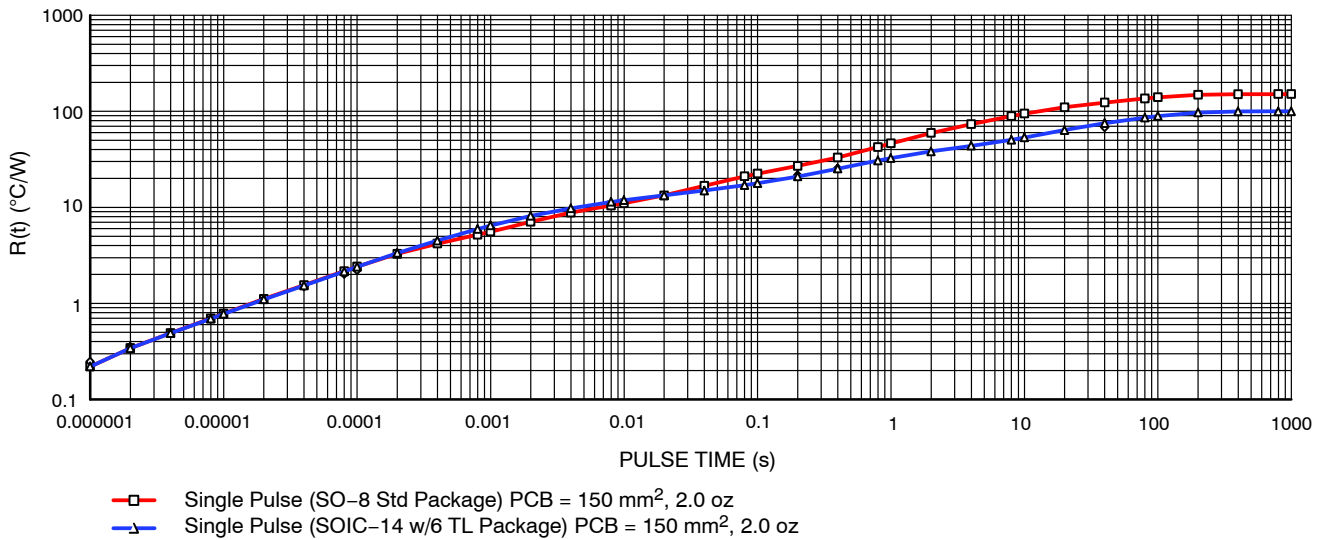


Figure 20. $R(t)$ vs. Pulse Time

APPLICATION DESCRIPTION

OUTPUT REGULATOR

The output is controlled by a precision trimmed reference. The PNP output has drive quiescent current control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

RESET OUTPUT (RO)

A reset signal, Reset Output, RO, (low voltage) is generated as the IC powers up. After the output voltage V_Q increases above the reset threshold voltage V_{RT} , the delay timer D is started. When the voltage on the delay timer V_D passes V_{UD} , the reset signal RO goes high. A discharge of the delay timer V_D is started when V_Q drops and stays below the reset threshold voltage V_{RT} . When the voltage of the delay timer V_D drops below the lower threshold voltage V_{LD} the reset output voltage V_{RO} is brought low to reset the processor.

The reset output RO is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that RO is valid for V_Q as low as 1.0 V.

RESET ADJUST (R_{ADJ})

The reset threshold V_{RT} can be decreased from a typical value of 4.65 V to as low as 3.5 V by using an external voltage divider connected from the Q lead to the pin RADJ, as shown in Figure 21. The resistor divider keeps the voltage above the $V_{RADJ,TH}$ (typical 1.35 V) for the desired input voltages, and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{RT} = V_{RADJ,TH} \cdot (RADJ1 + RADJ2) / RADJ2 \quad (\text{eq. 1})$$

If the reset adjust option is not needed, the R_{ADJ} pin should be connected to GND causing the reset threshold to go to its default value (typically 4.65 V).

RESET DELAY (D)

The reset delay circuit provides a delay (programmable by capacitor C_D) on the reset output lead RO. The delay lead D provides charge current $I_{D,C}$ (typically 6.5 μA) to the external delay capacitor C_D during the following times:

1. During Powerup (once the regulation threshold has been exceeded).
2. After a reset event has occurred and the device is back in regulation. The delay capacitor is set to discharge when the regulation (V_{RT} , reset threshold voltage) has been violated. When the delay capacitor discharges to V_{LD} , the reset signal RO pulls low.

SETTING THE DELAY TIME

The delay time is set by the delay capacitor C_D and the charge current I_D . The time is measured by the delay capacitor voltage charging from the low level of V_{DSAT} to the higher level V_{UD} . The time delay follows the equation:

$$t_d = [C_D (V_{UD} - V_{D,SAT})] / I_D \quad (\text{eq. 2})$$

Example:

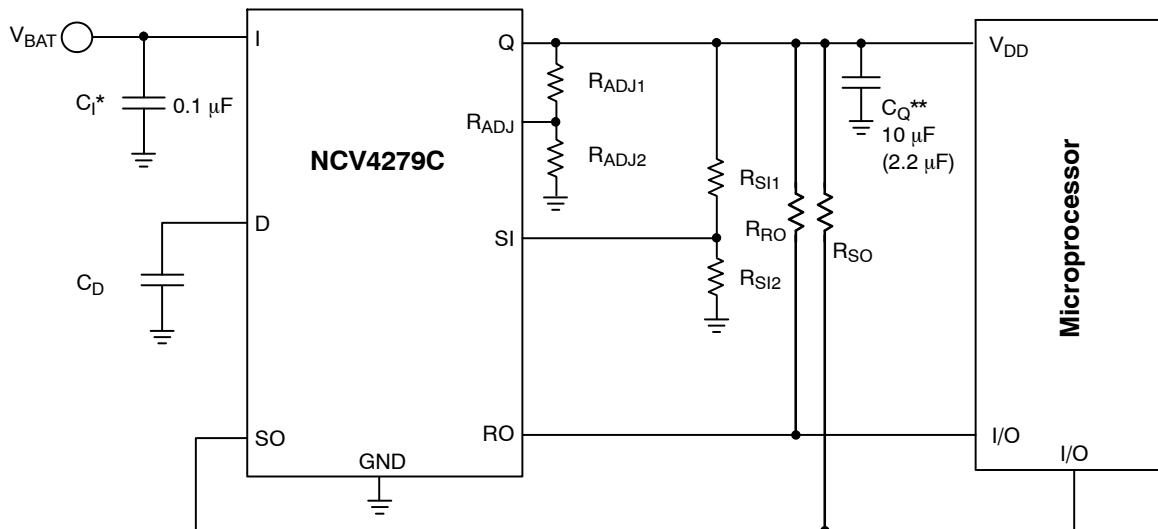
Using $C_D = 100 \text{ nF}$.

Use the typical value for $V_{D,SAT} = 0.1 \text{ V}$.

Use the typical value for $V_{UD} = 1.8 \text{ V}$.

Use the typical value for Delay Charge Current $I_D = 6.5 \mu\text{A}$.

$$t_d = [100 \text{ nF} (1.8 - 0.1 \text{ V})] / 6.5 \mu\text{A} = 26.2 \text{ ms} \quad (\text{eq. 3})$$



* C_1 required if regulator is located far from the power supply filter.

** C_Q – minimum cap required for stability is 2.2 μF while higher over/under-shoots may be expected. Cap must operate at required temperature range.

Figure 21. Application Diagram

SENSE INPUT (SI) / SENSE OUTPUT (SO) VOLTAGE MONITOR

An on-chip comparator is available to provide early warning to the microprocessor of a possible reset signal. The output is from an open collector driver. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor SI (Figure 21). The values for R_{SI1} and R_{SI2} are selected for a typical threshold of 1.20 V on the SI Pin.

SIGNAL OUTPUT

Figure 22 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 21. As the output voltage (V_O) falls, the monitor threshold ($V_{SI,Low}$), is crossed. This causes the voltage on the SO output to go low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal. When the voltage on the SO goes low and the RO stays high the current consumption is typically 560 μA at 1 mA load current.

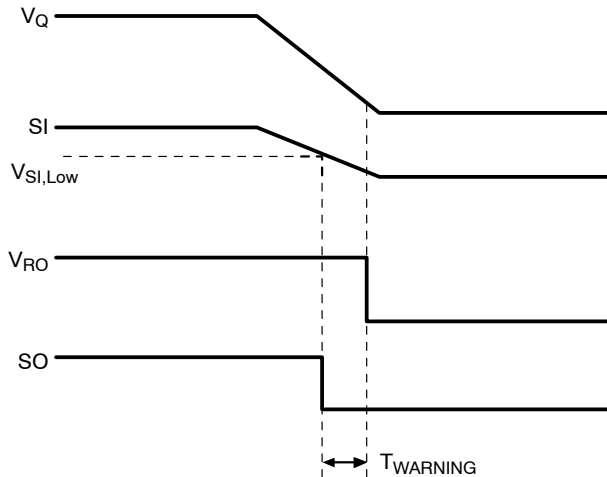


Figure 22. SO Warning Waveform Time Diagram

STABILITY CONSIDERATIONS

The input capacitor C_I in Figure 21 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1.0 Ω in series with C_I .

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive

solution, but, if the circuit operates at low temperatures ($-25^{\circ}C$ to $-40^{\circ}C$), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The 10 μF output capacitor C_O shown in Figure 21 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at C_O is min 2.2 μF and max ESR is 2.5 Ω . There is no min ESR limit which was proved with MURATA's ceramic caps GRM31MR71A225KA01 (2.2 μF , 10 V, X7R, 1206) and GRM31CR71A106KA01 (10 μF , 10 V, X7R, 1206) directly soldered between output and ground pins.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 21) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad (\text{eq. 4})$$

where:

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = (150^{\circ}C - T_A) / P_D \quad (\text{eq. 5})$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below $150^{\circ}C$. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (\text{eq. 6})$$

where:

$R_{\theta JC}$ = the junction-to-case thermal resistance,

$R_{\theta CS}$ = the case-to-heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers. Thermal, mounting, and heatsinking considerations are discussed in the onsemi application note [AN1040/D](#), available on the onsemi website.

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ORDERING INFORMATION

Device	Output Voltage	Package	Shipping [†]
NCV4279CD150R2G	5.0 V	SO-8 (Pb-Free)	2,500 / Tape & Reel

DISCONTINUED (Note 9)

NCV4279CD250R2G	5.0 V	SO-14 (Pb-Free)	2,500 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

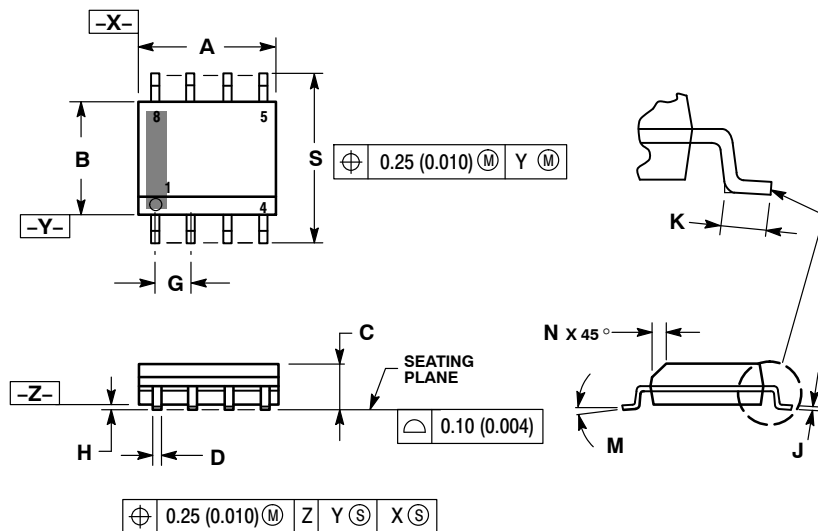
9. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*


SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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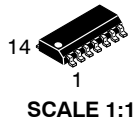
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

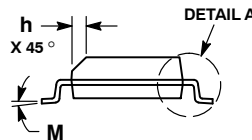
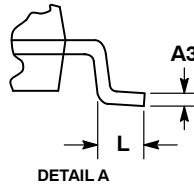
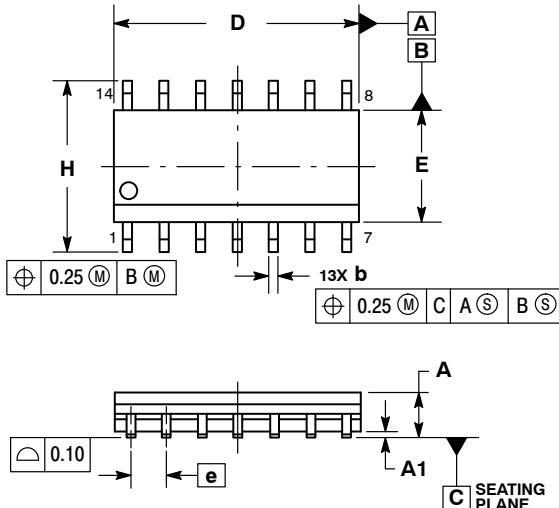
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SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

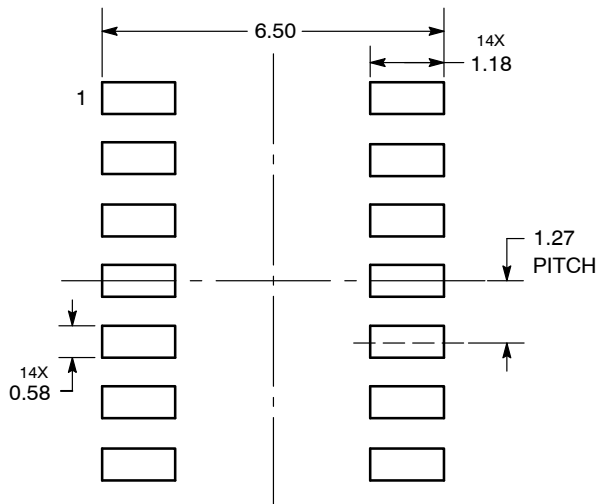


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

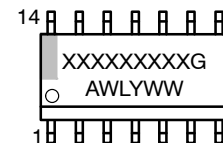
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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