Voltage Regulator - Low Dropout, Inhibit

30 mA

NCV4296-2C

The NCV4296–2C is a monolithic integrated low dropout voltage regulator with an output current capability of 30 mA available in the TSOP–5 package.

The output voltage is accurate within ±4.0% with a maximum dropout voltage of 250 mV with an input up to 45 V. Low quiescent current is a feature typically drawing only 160 μA with a 1 mA load. With Inhibit feature, the regulator can be turned off and the device consumes less than 5 μA of quiescent current. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit and thermal overload conditions.

Features

- Output Voltage Options: 3.3 V, 5.0 V
- Output Voltage Accuracy: ±4.0%
- Output Current: up to 30 mA
- Low Quiescent Current (typ. 160 μA @ 1 mA)
- Low Dropout Voltage (typ. 65 mV @ 20 mA)
- Wide Input Voltage Operating Range: up to 45 V
- Inhibit Input
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Polarity Protection and Reverse Bias Protection
- AEC–Q100 Grade 1 Qualified and PPAP Capable
- This is a Pb–Free Device

Typical Applications

- Microprocessor Systems Power Supply

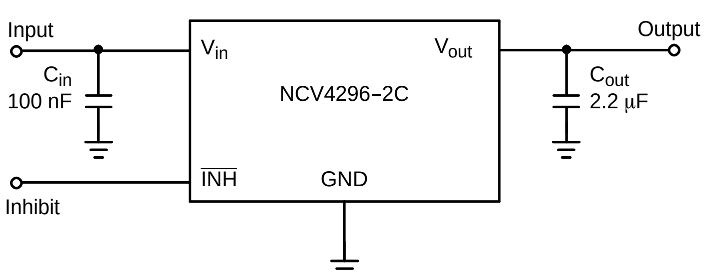
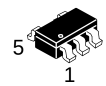
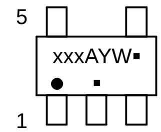


Figure 1. Applications Circuit

MARKING DIAGRAM



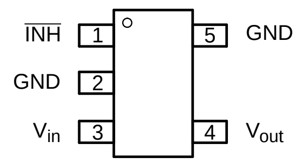
TSOP–5
CASE 483



xxx = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

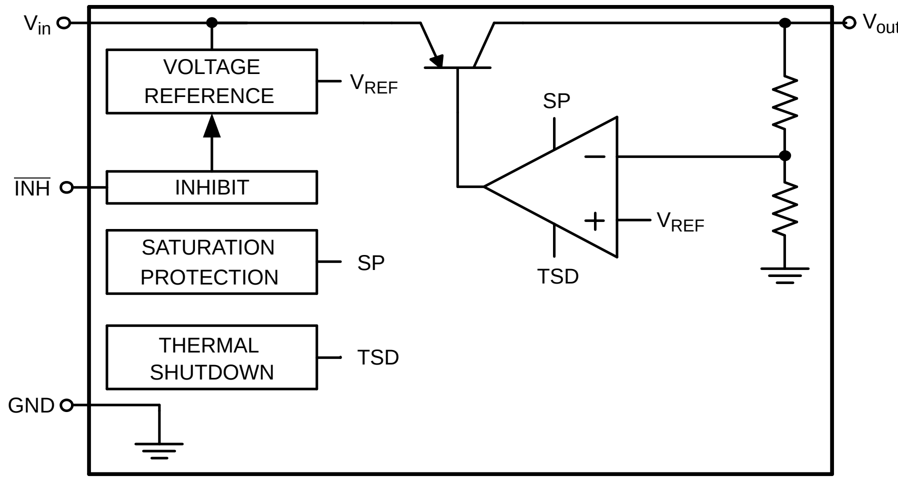


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin Name	Description
1	$\overline{INH}$	Inhibit Input. Low level disables the IC.
2	GND	Power Supply Ground.
3	V_{in}	Unregulated Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
4	V_{out}	Regulated Positive Output Voltage. Connect 2.2 μF capacitor with ESR < 7 Ω to ground.
5	GND	Power Supply Ground.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC (Note 1) DC	V_{in}	−42	45	V
Input Voltage (Note 2) Load Dump − Suppressed	U_s	−	60	V
Output Voltage	V_{out}	−6	30	V
Inhibit Input Voltage DC	$V_{\overline{INH}}$	−42	45	V
Inhibit Input Current Range DC Transient, −0.3 V ≤ V_{in} 45 V, t_p < 1 ms	$I_{\overline{INH}}$	−0.5 −5	− 5	mA
Maximum Junction Temperature	$T_{J(max)}$	−40	150	°C
Storage Temperature	T_{STG}	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes <50mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP−5 Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	136.2	°C/W

5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	V_{in}	$V_{out, nom}$ + 0.5 or 3.5	45	V
Inhibit Input Voltage	$V_{\overline{INH}}$	−0.3	40	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum V_{in} = $V_{out, nom}$ + 0.5 or 3.5, whichever is higher.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, $V_{\overline{INH}}$ > 2.5 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Note 7)

Parameter		Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT							
Output Voltage	5.0 V	V_{in} = 13.5 V, I_{out} = 1 mA to 30 mA V_{in} = 6 V to 40 V, I_{out} = 10 mA	V_{out}	4.80 4.80	5.00 5.00	5.20 5.20	V
	3.3 V	V_{in} = 13.5 V, I_{out} = 1 mA to 30 mA V_{in} = 4.3 V to 40 V, I_{out} = 10 mA		3.17 3.17	3.30 3.30	3.43 3.43	
Line Regulation		V_{in} = $V_{in,\ min}$ to 36 V, I_{out} = 5 mA, T_J = 25°C V_{in} = $V_{in,\ min}$ to 36 V, I_{out} = 5 mA	Reg_{line}	− −	5 10	20 30	mV
Load Regulation		I_{out} = 1 mA to 25 mA, T_J = 25°C I_{out} = 1 mA to 25 mA	Reg_{load}	− −	3 10	20 30	mV
Dropout Voltage (Note 8)		I_{out} = 20 mA	V_{DO}	−	65	250	mV
DISABLE AND QUIESCENT CURRENTS							
Disable Current		$V_{\overline{INH}}$ <= 0.4 V, T_J < 85°C $V_{\overline{INH}}$ <= 0.4 V	I_{DIS}	− −	0 0	1 5	μA
Quiescent Current, $I_q = I_{in} - I_{out}$		I_{out} < 0.1 mA, T_J < 85°C I_{out} < 1 mA I_{out} < 30 mA	I_q	− − −	150 160 0.8	170 200 4	μA μA mA
CURRENT LIMIT PROTECTION							
Current Limit		V_{out} = $V_{out,\ nom}$ – 100 mV	I_{LIM}	30	−	−	mA
PSRR							
Power Supply Ripple Rejection		f = 100 Hz, 0.5 V_{pp}	PSRR	−	60	−	dB
INHIBIT							
Inhibit Input Threshold Voltage Low (Off−State) High (On−State)		 V_{out} < 0.1 V V_{out} > 0.95 x $V_{out,\ nom}$	$V_{\overline{INH}}$	 0.4 −	 1.76 1.82	 − 2.2	V
Inhibit Input Current Low (Off−State) High (On−State)		 $V_{\overline{INH}}$ = 0 V $V_{\overline{INH}}$ = 5 V	 $I_{\overline{INH}\_OFF}$ $I_{\overline{INH}\_ON}$	 −2 −	 − 6	 2 12	μA
THERMAL SHUTDOWN							
Thermal Shutdown Temperature (Note 9)			T_{SD}	151	175	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V. If V_{out} < 5 V, then $V_{DO} = V_{in} - V_{out}$. Maximum dropout voltage value is limited by minimum input voltage $V_{in} = V_{out,\ nom}$ + 0.5 V recommended for guaranteed operation at maximum output current.
9. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS − 5.0 V VERSION

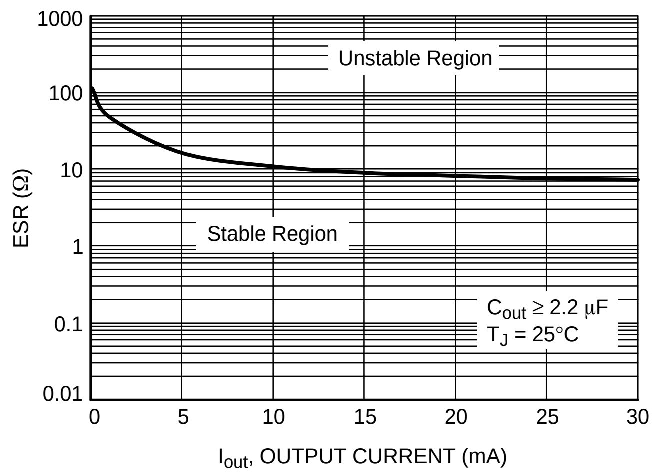


Figure 3. Output Stability with Output Capacitor ESR

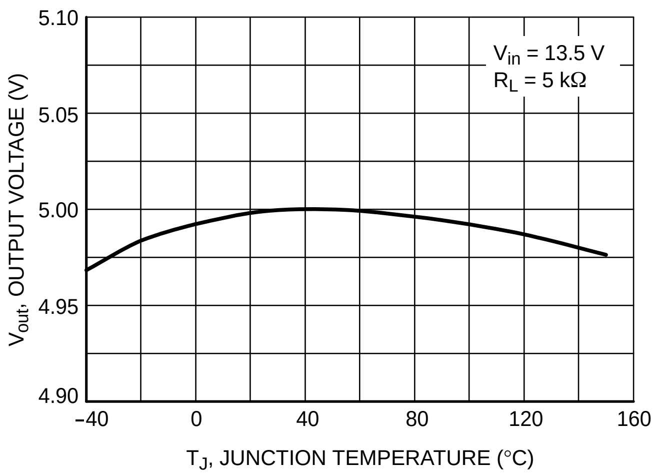


Figure 4. Output Voltage vs. Junction Temperature

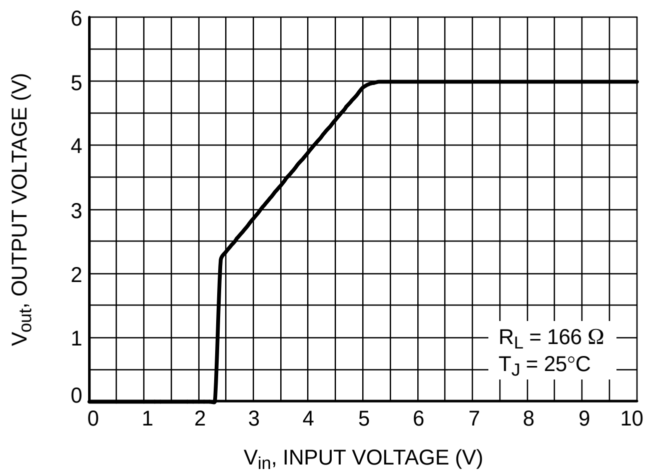


Figure 5. Output Voltage vs. Input Voltage

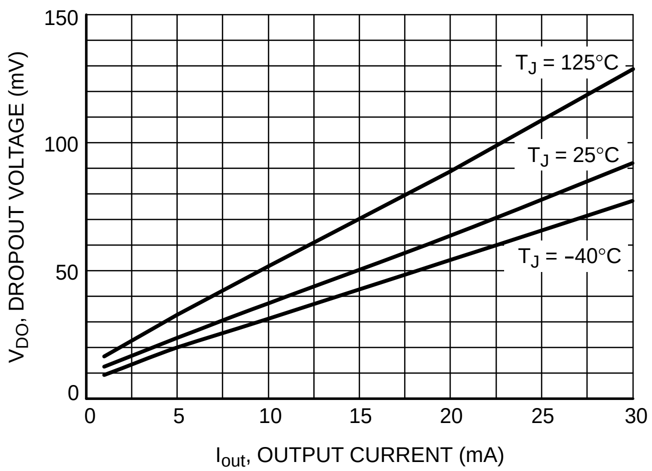


Figure 6. Dropout Voltage vs. Output Current

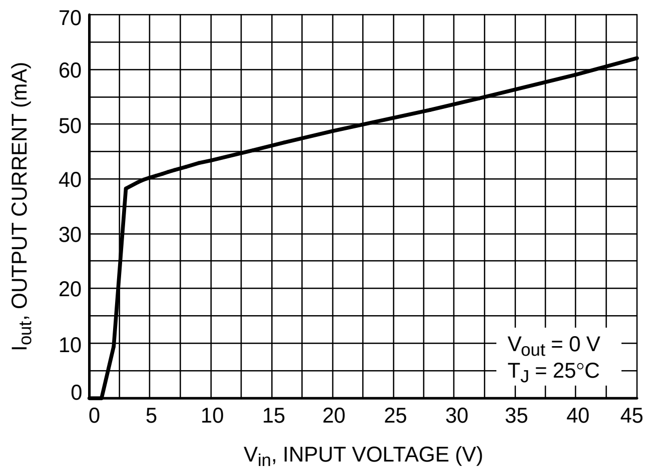


Figure 7. Maximum Output Current vs. Input Voltage

TYPICAL CHARACTERISTICS − 5.0 V VERSION

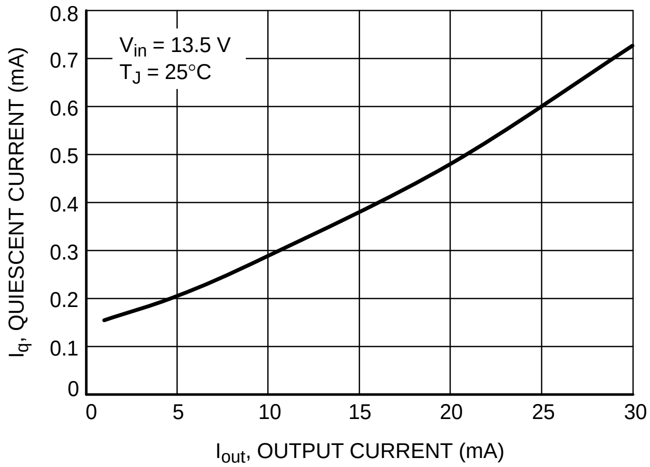


Figure 8. Quiescent Current vs. Output Current (High Load)

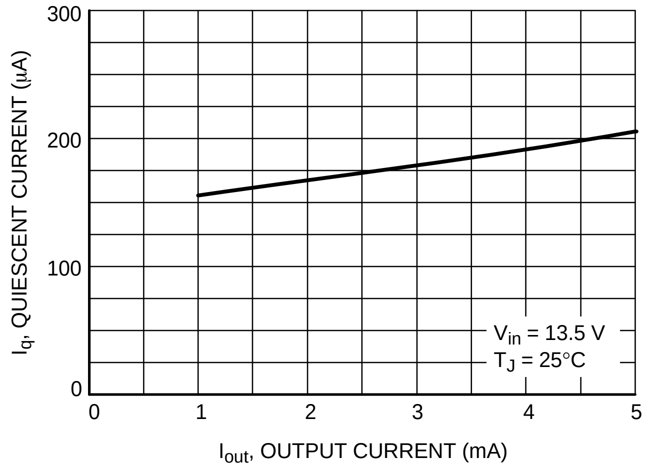


Figure 9. Quiescent Current vs. Output Current (Low Load)

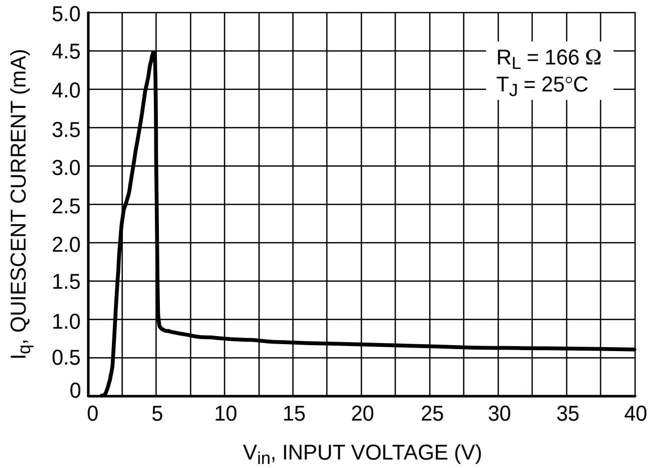


Figure 10. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTICS − 3.3 V VERSION

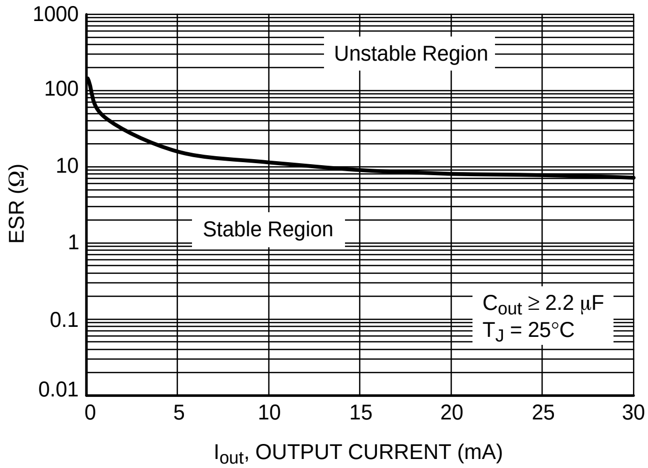


Figure 11. Output Stability with Output Capacitor ESR

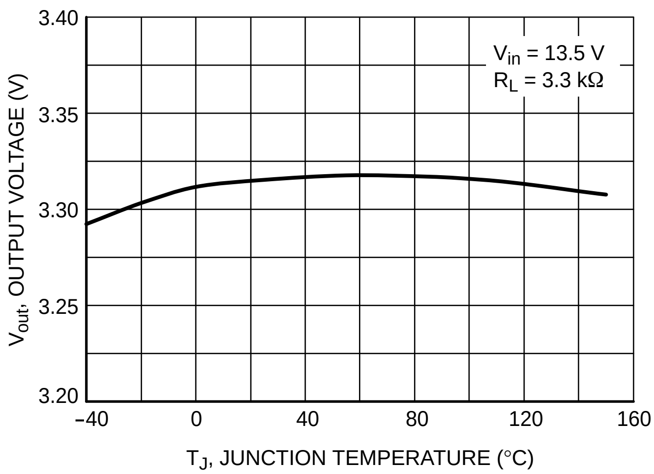


Figure 12. Output Voltage vs. Junction Temperature

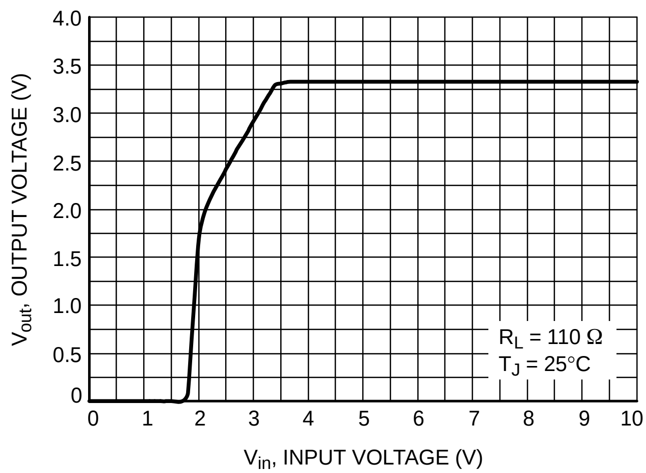


Figure 13. Output Voltage vs. Input Voltage

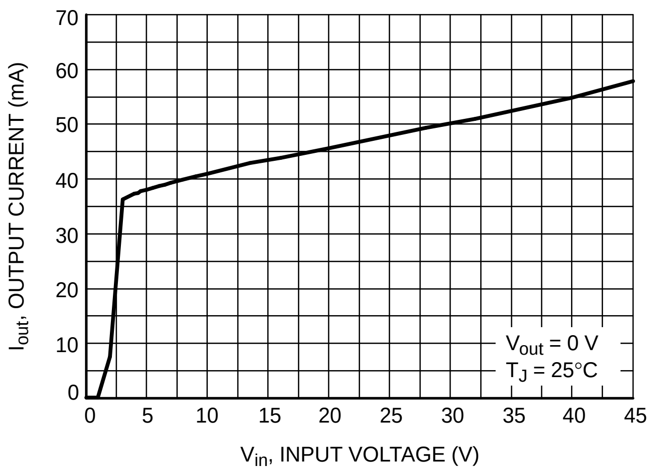


Figure 14. Maximum Output Current vs. Input Voltage

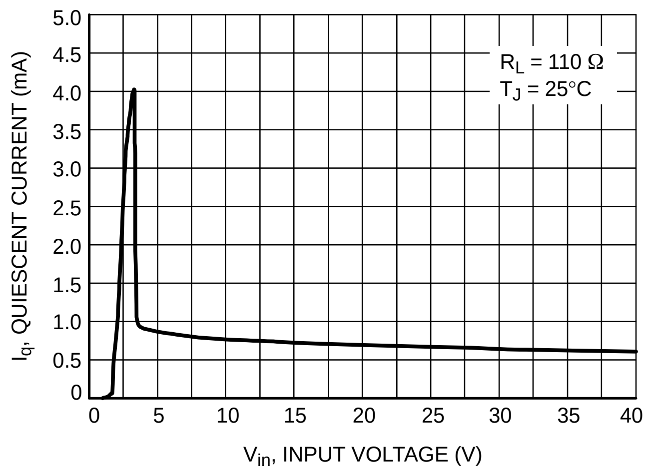


Figure 15. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTICS − 3.3 V VERSION

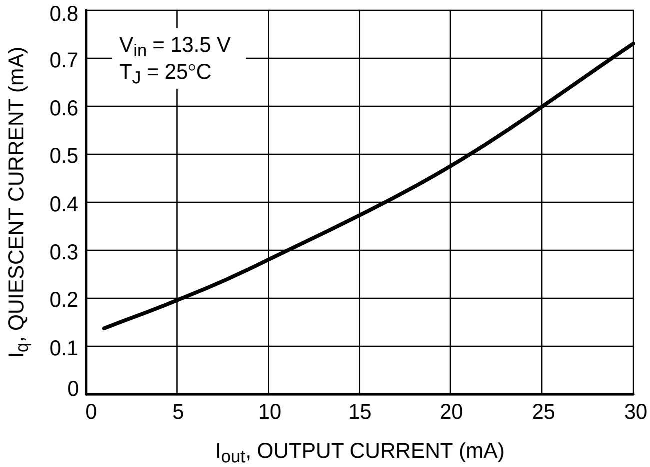


Figure 16. Quiescent Current vs. Output Current (High Load)

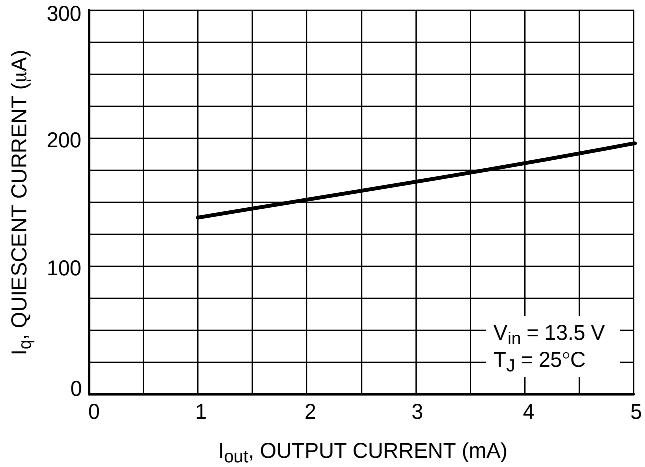


Figure 17. Quiescent Current vs. Output Current (Low Load)

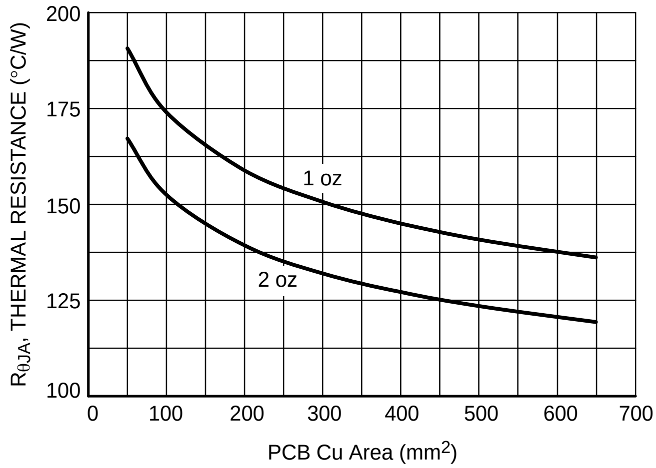


Figure 18. $R_{\theta JA}$ vs. PCB Cu Area

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Inhibit pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops 100 mV below its nominal value. It means that the device is capable to supply minimum 30 mA.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV4296−2C low dropout regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 3 to Figure 18.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV4296−2C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{out})

The NCV4296−2C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs. Output Current is shown in Figures 3 and 11. The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load transient response.

Inhibit Operation

The Inhibit pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet.

Thermal Considerations

As power in the NCV4296−2C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV4296−2C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV4296−2C can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV4296−2C soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 0.92 W when the ambient temperature (T_A) is 25°C. See Figure 18 for R_{thJA} versus PCB area. The power dissipated by the NCV4296−2C can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

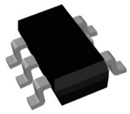
Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV4296−2C and make traces as short as possible.

ORDERING INFORMATION

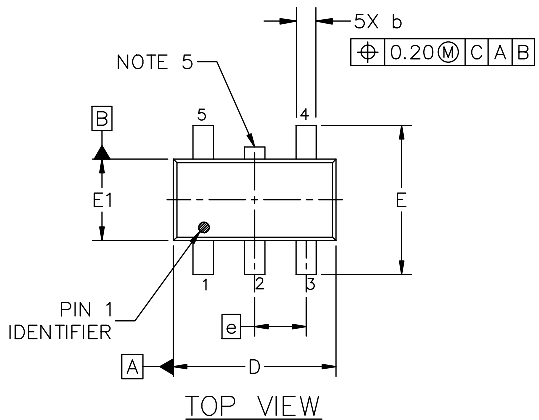
Device	Marking	Package	Shipping†
NCV4296−2CSN50T1G	65V	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV4296−2CSN33T1G	63V	TSOP−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



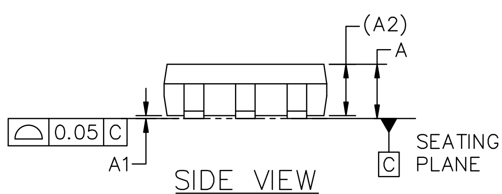
TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

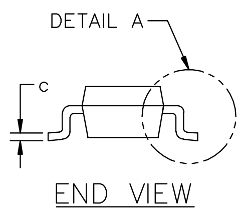
DATE 01 APR 2024



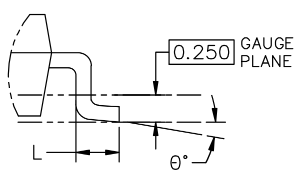
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

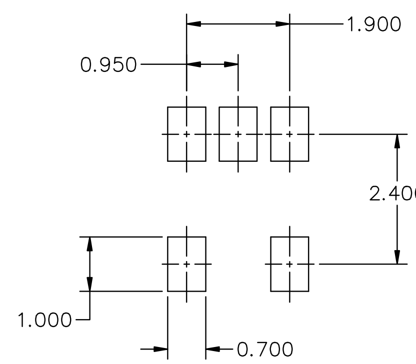




DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



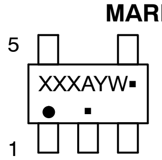
DETAIL "A"
SCALE 2:1



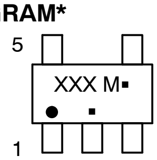
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP−5 3.00x1.50x0.95, 0.95P	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊