# Stand-alone LIN Transceiver

# NCV7329

SOIC−8
CASE 751AZ

DFN8
CASE 507AB

## Description

The NCV7329 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU−state machine that recognizes and translates the instructions specific to that function.

The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

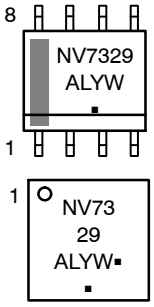
## Features

- LIN−Bus Transceiver
  - Compliant to ISO 17987−4 (Backwards Compatible to LIN Specification rev. 2.x, 1.3) and SAE J2602
  - Bus Voltage ±42 V
  - Transmission Rate 1 kbps to 20 kbps
  - TxD Timeout Function
  - Integrated Slope Control
- Protection
  - Thermal Shutdown
  - Undervoltage Protection
  - Bus Pins Protected Against Transients in an Automotive Environment
- Modes
  - Normal Mode: LIN Transceiver Enabled, Communication via the Bus is Possible
  - Sleep Mode: LIN Transceiver Disabled, the Consumption from $V_{BB}$ is Minimized
  - Standby Mode: Transition Mode Reached after Wake−up Event on the LIN Bus
- Compatibility
  - Pin−Compatible Subset with NCV7321
  - K−line Compatible

## Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Require− ments; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

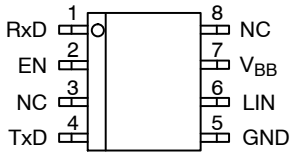
## MARKING DIAGRAMS



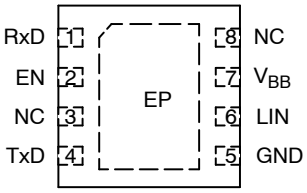

| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

## PIN CONNECTIONS




SOIC−8 (Top View)




DFN8 (Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

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## BLOCK DIAGRAM

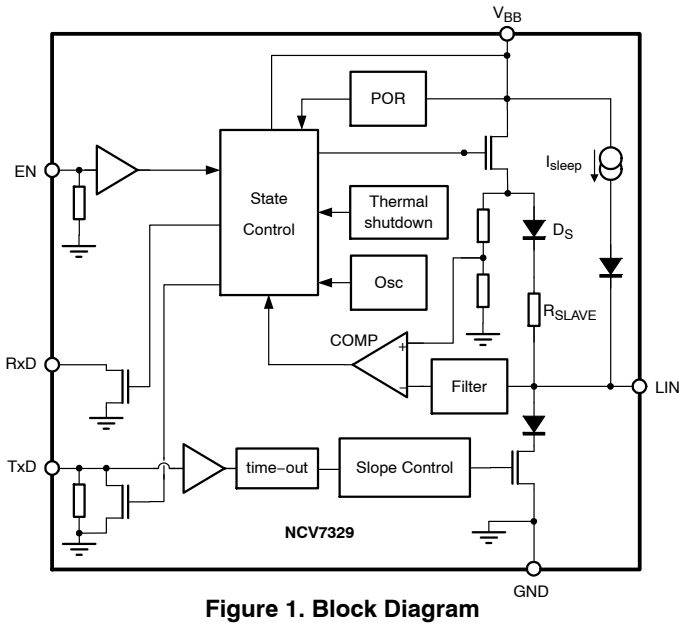


**Figure 1. Block Diagram**

## TYPICAL APPLICATION

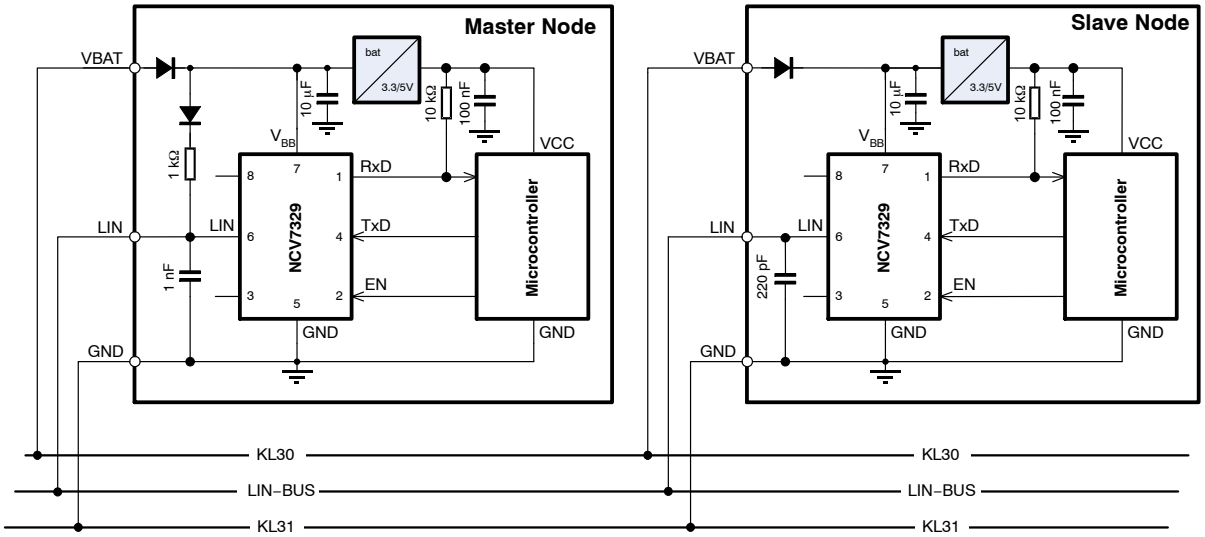


**Figure 2. Typical Application Diagram for a Master Node**

**Table 1. PIN DESCRIPTION**

| Pin | Name | Description |
|---|---|---|
| 1 | RxD | Receive Data Output; Low in Dominant State; Open−Drain Output |
| 2 | EN | Enable Input, Transceiver in Normal Operation Mode when High, Pull−down Resistor to GND |
| 3 | NC | Not Connected |
| 4 | TxD | Transmit Data Input, Low for Dominant State, Pull−down to GND |
| 5 | GND | Ground |
| 6 | LIN | LIN Bus Output/Input |
| 7 | $V_{BB}$ | Battery Supply Input |
| 8 | NC | Not Connected |
| − | EP | Exposed Pad. Recommended to connect to GND or left floating in application (DFN8 package only). |



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**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{BB}$ | Voltage on Pin $V_{BB}$ | −0.3 | +42 | V |
| $V_{LIN}$ | LIN Bus Voltage with respect to GND | −42 | +42 | V |
| | LIN Bus Voltage with respect to $V_{BB}$ | −42 | +42 | V |
| V_Dig_IO | DC Input Voltage on Pins (EN, RxD, TxD) | −0.3 | +7 | V |
| $V_{ESD}$ | Human Body Model (LIN Pin) (Note 1) | −8 | +8 | kV |
| | Human Body Model (All Pins) (Note 1) | −4 | +4 | kV |
| | Charged Device Model (All Pins) (Note 2) | −750 | +750 | V |
| | Machine Model (All Pins) (Note 3) | −200 | +200 | V |
| $V_{ESDIEC}$ | Electrostatic Discharge Voltage (LIN Pin) System Human Body Model (Note 4) Conform to IEC 61000−4−2 | −8 | +8 | kV |
| $T_J$ | Junction Temperature Range | −40 | +150 | °C |
| $T_{STG}$ | Storage Temperature Range | −55 | +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC−Q100−011.
3. In accordance to JEDEC JESD22−A115. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and 0.75 μH coil.
4. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor. System HBM levels are verified by an external test−house.

**Table 3. THERMAL CHARACTERISTICS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| | Thermal characteristics, SOIC−8 (Note 5) | | |
| $R_{\theta JA}$ | Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 6) | 131 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 7) | 81 | °C/W |
| | Thermal characteristics, DFN8 (Note 5) | | |
| $R_{\theta JA}$ | Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 6) | 125 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 7) | 58 | °C/W |

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. Values based on test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
7. Values based on test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.


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## ELECTRICAL CHARACTERISTICS

### Definitions

All voltages are referenced to GND (pin 5) unless otherwise specified. Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

**Table 4. DC CHARACTERISTICS** ($V_{BB}$ = 5 V to 18 V; $T_J$ = −40°C to +150°C; Typical values are given at $V_{BB}$ = 12 V and $T_J$ = 25°C Bus Load = 500 Ω ($V_{BB}$ to LIN); unless otherwise specified.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SUPPY PIN ($V_{BB}$)** | | | | | | |
| $V_{BB}$ | Battery Supply | | 5 | | 18 | V |
| $I_{BB}$ | Battery Supply Current | Normal Mode; LIN recessive | 0.2 | 0.55 | 1.2 | mA |
| $I_{BB}$ | Battery Supply Current | Normal Mode; TxD = Low, LIN Dominant | 2 | 3.9 | 6.5 | mA |
| $I_{BB}$ | Battery Supply Current | Sleep and Standby Mode; LIN recessive; $V_{LIN} = V_{BB}$; $T_J$<85°C | | 6 | 10 | μA |
| $I_{BB}$ | Battery Supply Current | Sleep and Standby Mode; LIN recessive; $V_{LIN} = V_{BB}$ | | 6 | 15 | μA |
| **POR AND $V_{BB}$ MONITOR** | | | | | | |
| PORH_$V_{BB}$ | Power−on Reset; High Level on $V_{BB}$ | $V_{BB}$ Rising | 2.7 | 3.5 | 4.4 | V |
| PORL_$V_{BB}$ | Power−on Reset; Low Level on $V_{BB}$ | $V_{BB}$ Falling | 1.3 | 2.1 | 2.7 | V |
| MONH_$V_{BB}$ | Battery Monitoring High Level | $V_{BB}$ Rising | 3.2 | 4.2 | 5.0 | V |
| MONL_$V_{BB}$ | Battery Monitoring Low Level | $V_{BB}$ Falling | 3.0 | 4.0 | 4.8 | V |
| **TRANSMITTER DATA INPUT (PIN TxD)** | | | | | | |
| $V_{IL_TxD}$ | Low Level Input Voltage | | −0.3 | | +0.8 | V |
| $V_{IH_TxD}$ | High Level Input Voltage | | 2 | | 7 | V |
| $R_{PD_TxD}$ | Pull−down Resistor on TxD Pin | | 50 | 125 | 325 | kΩ |
| **RECEIVER DATA OUTPUT (PIN RxD)** | | | | | | |
| $I_{OL_RxD}$ | Low Level Output Current | $V_{RXD}$ = 0.4 V | 2 | | | mA |
| $I_{OH_RxD}$ | High Level Output Current | | −5 | | +5 | μA |
| **ENABLE INPUT (PIN EN)** | | | | | | |
| $V_{IL_EN}$ | Low Level Input Voltage | | −0.3 | | +0.8 | V |
| $V_{IH_EN}$ | High Level Input Voltage | | 2 | | 7 | V |
| $R_{PD_EN}$ | Pull−down Resistor to Ground | | 100 | 250 | 650 | kΩ |
| **LIN BUS LINE (PIN LIN)** | | | | | | |
| $V_{BUS_DOM}$ | Bus Voltage for Dominant State | | | | 0.4 | $V_{BB}$ |
| $V_{BUS_REC}$ | Bus Voltage for Recessive State | | 0.6 | | | $V_{BB}$ |
| $V_{REC_DOM}$ | Receiver Threshold | LIN Bus Recessive − Dominant | 0.4 | | 0.6 | $V_{BB}$ |
| $V_{REC_REC}$ | Receiver Threshold | LIN Bus Dominant − Recessive | 0.4 | | 0.6 | $V_{BB}$ |
| $V_{REC_CNT}$ | Receiver Centre Voltage | ($V_{REC_DOM}$ + $V_{REC_REC}$) / 2 | 0.475 | 0.500 | 0.525 | $V_{BB}$ |
| $V_{REC_HYS}$ | Receiver Hysteresis | ($V_{REC_REC}$ − $V_{REC_DOM}$) | 0.050 | | 0.175 | $V_{BB}$ |
| $V_{LIN_DOM}$ | Dominant Output Voltage | Normal mode; $V_{BB}$ = 7 V | | | 1.2 | V |
| | | Normal mode; $V_{BB}$ = 18 V | | | 2.0 | V |
| $I_{BUS_no_GND}$ | Communication not Affected | $V_{BB}$ = GND = 12 V; 0 < $V_{LIN}$ < 18 V | −1 | | +1 | mA |

8. Values based on design and characterization. Not tested in production.



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**Table 4. DC CHARACTERISTICS** ($V_{BB}$ = 5 V to 18 V; $T_J$ = −40°C to +150°C; Typical values are given at $V_{BB}$ = 12 V and $T_J$ = 25°C Bus Load = 500 Ω ($V_{BB}$ to LIN); unless otherwise specified.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **LIN BUS LINE (PIN LIN)** | | | | | | |
| $I_{BUS_no_VBB}$ | LIN Bus Remains Operational | $V_{BB}$ = GND = 0 V; 0 < $V_{LIN}$ < 18 V | | | 5 | μA |
| $I_{BUS_LIM}$ | Current limitation for Driver | Dominant State; $V_{LIN}$ = $V_{BB_MAX}$ | 40 | | 200 | mA |
| $I_{BUS_PAS_dom}$ | Receiver Leakage current; Driver OFF | TxD = High; $V_{LIN}$ = 0 V; $V_{BB}$ = 12 V | −1 | | | mA |
| $I_{sleep}$ | Receiver Leakage current; see Figure 1 | Sleep mode; $V_{LIN}$ = 0 V; $V_{BB}$ = 12 V | −16 | −8 | −3 | μA |
| $I_{BUS_PAS_rec}$ | Receiver Leakage current; Driver OFF; (Note 8) | TxD = High; 8 V < $V_{BB}$ < 18 V; 8 V < $V_{LIN}$ < 18 V; $V_{LIN}$ ≥ $V_{BB}$ | | | 20 | μA |
| $V_{SERDiode}$ | Voltage Drop on Serial Diode | Voltage drop on $D_S$, see Figure 1 | 0.4 | 0.7 | 1 | V |
| $R_{SLAVE}$ | Internal Pull−up Resistance | see Figure 1 | 20 | 30 | 60 | kΩ |
| $C_{LIN}$ | Capacitance on Pin LIN, (Note 8) | | | 20 | 30 | pF |

8. Values based on design and characterization. Not tested in production.



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**Table 5. AC CHARACTERISTICS** ($V_{BB}$ = 5 V to 18 V; $T_J$ = −40°C to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **LIN TRANSCEIVER** | | | | | | |
| D1 | Duty Cycle 1 = $t_{BUS_REC(min)}$ / ($2xt_{BIT}$) (See Figure 4) | $TH_{REC(max)}$ = 0.744 x $V_{BB}$<br>$TH_{DOM(max)}$ = 0.581 x $V_{BB}$<br>$t_{BIT}$ = 50 µs<br>$V_{BB}$ = 5 V to 18 V | 0.396 | | 0.500 | |
| D2 | Duty Cycle 2 = $t_{BUS_REC(max)}$ / ($2xt_{BIT}$) (See Figure 4) | $TH_{REC(min)}$ = 0.422 x $V_{BB}$<br>$TH_{DOM(min)}$ = 0.284 x $V_{BB}$<br>$t_{BIT}$ = 50 µs<br>$V_{BB}$ = 5 V to 18 V | 0.500 | | 0.581 | |
| D3 | Duty Cycle 3 = $t_{BUS_REC(min)}$ / ($2xt_{BIT}$) (See Figure 4) | $TH_{REC(max)}$ = 0.778 x $V_{BB}$<br>$TH_{DOM(max)}$ = 0.616 x $V_{BB}$<br>$t_{BIT}$ = 96 µs<br>$V_{BB}$ = 5 V to 18 V | 0.417 | | 0.500 | |
| D4 | Duty Cycle 4 = $t_{BUS_REC(max)}$ / ($2xt_{BIT}$) (See Figure 4) | $TH_{REC(min)}$ = 0.389 x $V_{BB}$<br>$TH_{DOM(min)}$ = 0.251 x $V_{BB}$<br>$t_{BIT}$ = 96 µs<br>$V_{BB}$ = 5 V to 18 V | 0.500 | | 0.590 | |
| $t_{TX_PROP_DOWN}$ | Propagation Delay of TxD to LIN. TxD High to Low (See Figure 7) | | | | 14 | µs |
| $t_{TX_PROP_UP}$ | Propagation Delay of TxD to LIN. TxD Low to High (See Figure 7) | | | | 14 | µs |
| **LIN RECEIVER** | | | | | | |
| $t_{RX_PD}$ | Propagation Delay of Receiver, Rising and falling Edge (See Figure 5) | $R_{RxD}$ = 2.4 kΩ; $C_{RXD}$ = 20 pF | 0.1 | | 6 | µs |
| $t_{RX_SYM}$ | Propagation Delay Symmetry | $R_{RxD}$ = 2.4 kΩ; $C_{RXD}$ = 20 pF; Rising edge with respect to falling edge | −2 | | +2 | µs |
| **MODE TRANSITIONS AND TIMEOUTS** | | | | | | |
| $t_{LIN_WAKE}$ | Duration of LIN Dominant for Detection of Wake−up via LIN Bus (See Figure 6) | Sleep Mode | 40 | 70 | 150 | µs |
| $t_{TxD_TIMEOUT}$ | TxD Dominant Timeout | Normal Mode, TxD = Low | 14 | 25 | 46 | ms |
| $t_{INIT_NORM}$ | Time From Rising Edge of EN pin to the moment when the transmitter is able to correctly transmit | | 15 | 30 | 75 | µs |
| $t_{ENABLE}$ | Duration of EN pin in High Level State for transition to Normal Mode | | 11 | 20 | 55 | µs |
| $t_{DISABLE}$ | Duration of EN pin in Low Level State for transition to Sleep Mode | | 11 | 20 | 55 | µs |
| $t_{TO_STB}$ | Delay from LIN Bus Dominant to Recessive Edge to Entering of Standby Mode after Valid LIN Wake−up (See Figure 6) | Sleep Mode | 5 | 10 | 40 | µs |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J(sd)}$ | Shutdown Junction Temperature | Temperature Rising | 160 | 180 | 200 | °C |

9. Values based on design and characterization. Not tested in production.



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## FUNCTIONAL DESCRIPTION

### Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications.

The NCV7329 contains the LIN transmitter, LIN receiver, power−on−reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for a maximum specified transmission speed of 20 kbps.

**Table 6. OPERATING MODES**

| Pin EN | Mode | Pin RxD | LIN bus |
|---|---|---|---|
| x | Unpowered | Floating | OFF; Floating |
| Low | Sleep | Floating | OFF; Floating |
| Low | Standby | Low indicates wake−up | OFF; 30 kΩ |
| High | Normal | LOW: dominant<br>HIGH: recessive | ON; 30 kΩ |

### Unpowered Mode

As long as $V_{BB}$ remains below its power−on−reset level, the chip is kept in a safe unpowered state. The LIN transmitter is inactive, the LIN pin is left floating and only a weak pull−down is connected on pin TxD. Pin RxD remains floating.

The unpowered state will be entered from any other state when $V_{BB}$ falls below its power−on−reset level (PORL_$V_{BB}$). When $V_{BB}$ rises above the power−on−reset high threshold (PORH_$V_{BB}$), the NCV7329 switches to a Sleep mode.

### Normal Mode

In the Normal mode, the full functionality of the LIN transceiver is available. The transceiver can transmit and receive data via the LIN bus with speed up to 20 kbps. Data according the state of TxD input are sent to the LIN bus while pin RxD reflects the logical symbol received on the LIN bus − high−impedant for recessive and Low for dominant. A 30 kΩ resistor in series with a reverse−protection diode is internally connected between LIN and $V_{BB}$ pins.

The signal on pin TxD passes through a timer, which releases the bus in case the TxD remains low for longer than $t_{TxD_TIMEOUT}$. It prevents the LIN bus being permanently driven dominant and thus blocking all subsequent communication due to a failure of the application (e.g. software error). The transmission can continue once the TxD returns to High logical level.

In case the junction temperature increases above the thermal shutdown threshold ($T_{J(sd)}$), e.g. due to a short of the LIN wiring to the battery, the transmitter is disabled and releases the LIN bus to recessive. Once the junction temperature decreases back below the thermal shutdown level, the transmission can be enabled again. However, to avoid thermal oscillations, first a High logical level on TxD must be encountered before the transmitter is enabled.

As required by SAE J2602, the transceiver must behave safely below its operating range – it shall either continue to transmit correctly (according its specification) or remain silent (transmit a recessive state regardless of the TxD signal). A battery monitoring circuit in NCV7329 deactivates the transmitter in the Normal mode if the $V_{BB}$ level drops below MONL_$V_{BB}$. Transmission is enabled again when $V_{BB}$ reaches MONH_$V_{BB}$. The internal logic remains in the normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power−on−reset levels are overlapping, it's ensured by the implementation that the monitoring level never falls below the power−on−reset level.

The Normal mode can be entered from either Standby or Sleep mode when EN Pin is High for longer than $t_{ENABLE}$. When the transition is made from Standby mode, TxD pull−down is set to weak and RxD is put into a high−impedance immediately after EN becomes High (before the expiration of $t_{ENABLE}$ filtering time). This excludes signal conflicts between the Standby mode pin settings and the signals required to control the chip in the Normal mode after a local wake−up vs. High logical level on TxD required to send a recessive symbol to the LIN bus.

### Sleep Mode

Sleep mode provides extremely low current consumption. The LIN transceiver is inactive and the battery consumption is minimized.

This mode is entered in one of the following ways:

- After the voltage level at $V_{BB}$ pin rises above its power−on−reset level (PORH_$V_{BB}$). In this case, RxD Pin remains high−impedant and the pull−down applied on pin TxD remains weak.
- After assigning Low logical level to pin EN for longer than $t_{DISABLE}$ while NCV7329 is in the Normal mode.

### Standby Mode

Standby mode is entered from the Sleep mode when a remote wake−up event occurred. The Low level on RxD pin indicates interrupt flag for the microcontroller.



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## OPERATING STATES

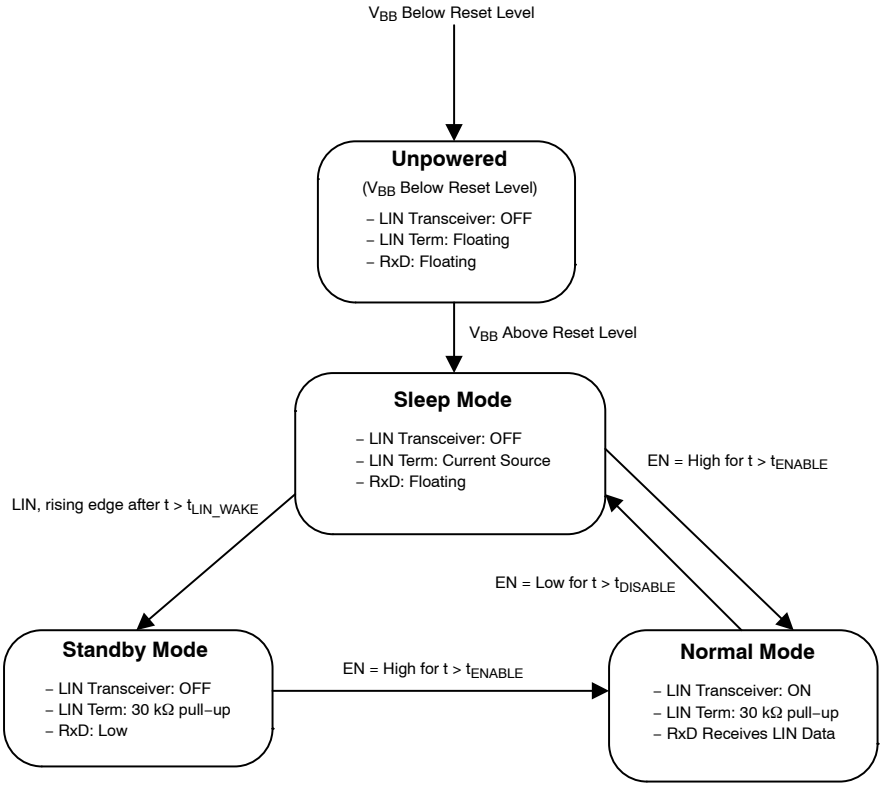


**Figure 3. State Diagram**



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## MEASUREMENT SETUPS AND DEFINITIONS

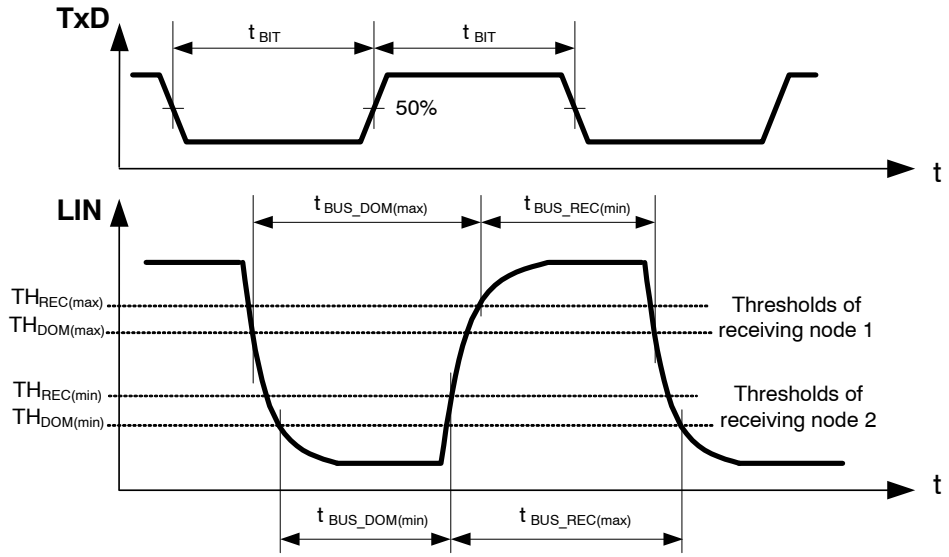


**Figure 4. LIN Transmitter Duty Cycle**

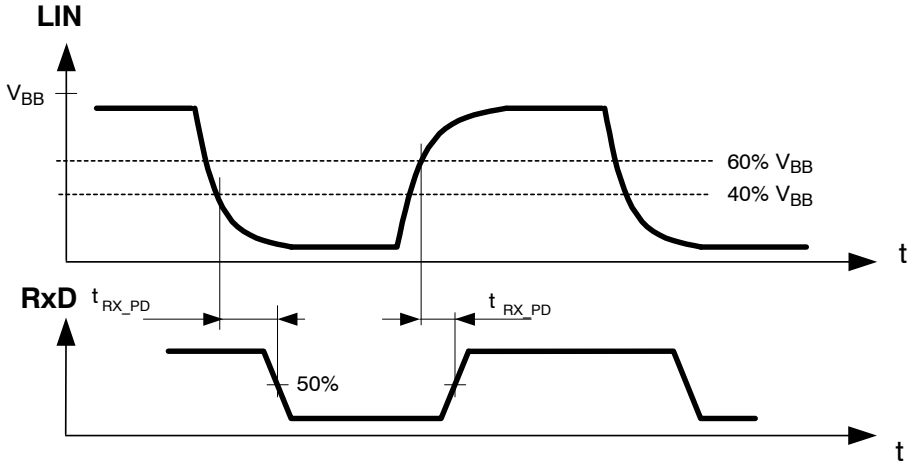


**Figure 5. LIN Receiver Timing**

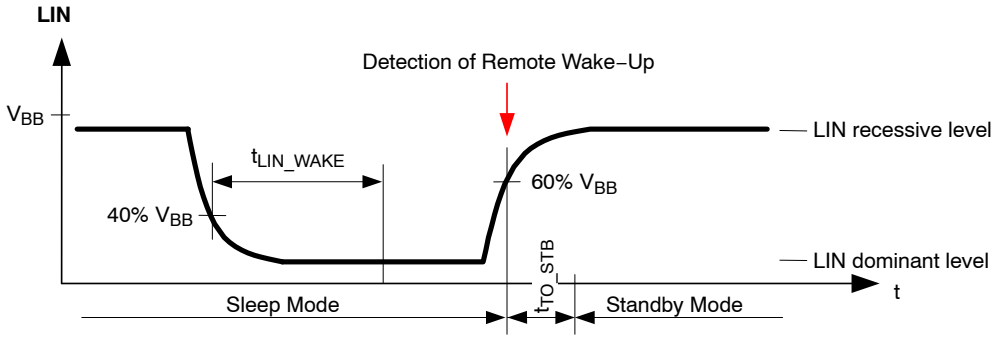


**Figure 6. Remote (LIN) Wake−up Detection**



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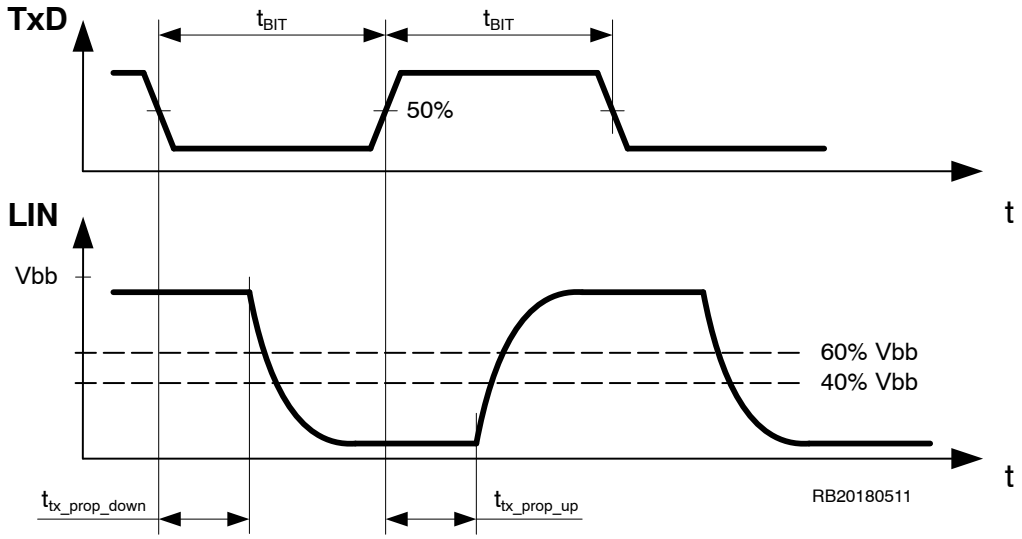


**Figure 7. LIN Transmitter Timing**

## DEVICE ORDERING INFORMATION

| Part Number | Description | Temperature Range | Package | Shipping† |
|---|---|---|---|---|
| NCV7329D10R2G | Stand−alone LIN Transceiver | −40°C to +125°C | SOIC−8 (Pb−Free) | 3,000 / Tape & Reel |
| NCV7329MW0R2G | Stand−alone LIN Transceiver | −40°C to +125°C | DFN8 (Pb−Free) | 3,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 1 | Rebranded the Data Sheet to **onsemi** format. | 5/21/2025 |



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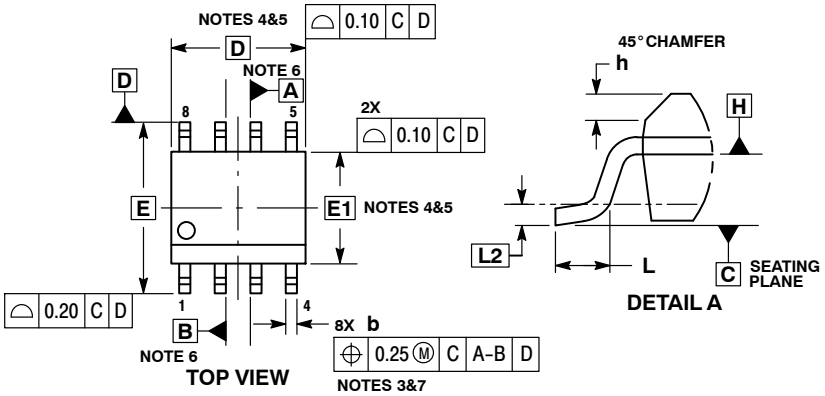
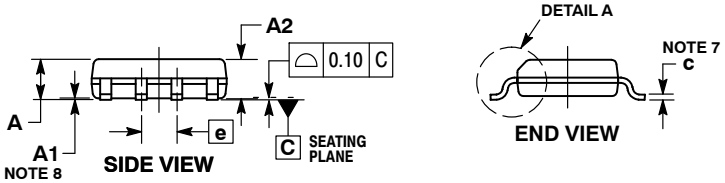
**SCALE 1:1**

**SOIC−8**
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

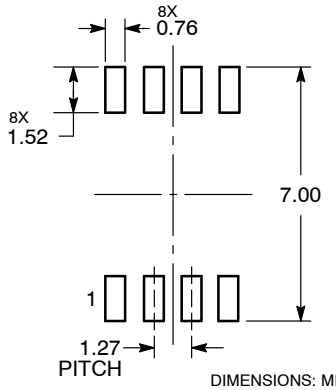



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | --- |
| b | 0.31 | 0.51 |
| c | 0.10 | 0.25 |
| D | 4.90 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| h | 0.25 | 0.41 |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |

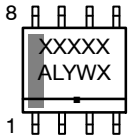
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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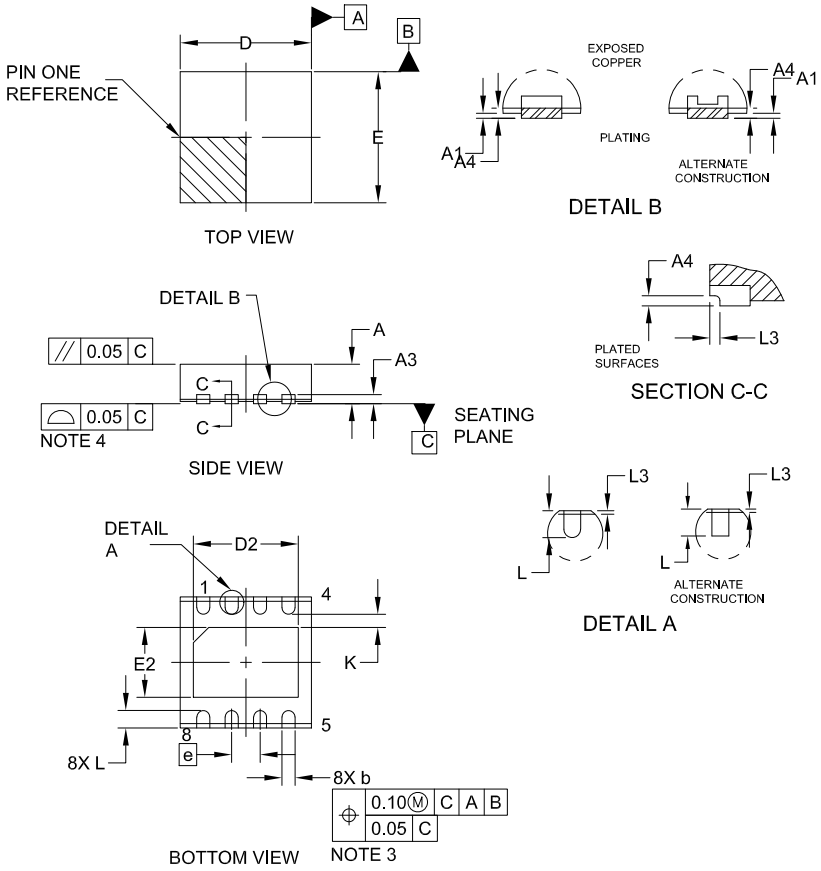
**SCALE 2:1**

**DFNW8 3x3, 0.65P**
CASE 507AB
ISSUE E

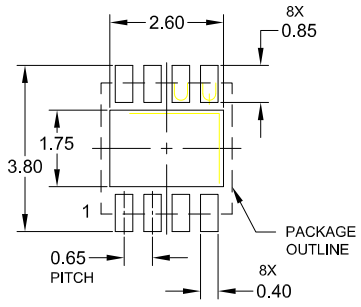
DATE 02 JUL 2021




NOTES:

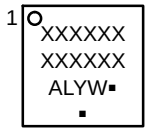
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | — | — | 0.05 |
| A3 | | 0.20 REF | |
| A4 | 0.10 | --- | — |
| b | 0.25 | 0.30 | 0.35 |
| D | 2.95 | 3.00 | 3.05 |
| D2 | 2.30 | 2.40 | 2.50 |
| E | 2.95 | 3.00 | 3.05 |
| E2 | 1.50 | 1.60 | 1.70 |
| e | | 0.65 BSC | |
| K | | 0.30 REF | |
| L | 0.35 | 0.40 | 0.45 |
| L3 | 0.00 | 0.05 | 0.10 |




RECOMMENDED
MOUNTING FOOTPRINT

## GENERIC MARKING DIAGRAM*




XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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