

SPI Controlled H-bridge and Dual-Half Bridge Pre-Driver

NCV7535

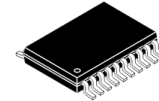
The NCV7535 is a monolithic SPI controlled H-bridge pre-driver providing control of a DC-motor. Due to the SPI interface, it includes enhanced feature set useful in automotive systems. This allows a highly integrated solution.

Features

- Main Supply Functional Operating Range from 5 V to 28 V
- Main Supply Parametrical Operating Range 6 V to 18 V
- Active and Standby Operating Modes
- Compatible to Low-ohmic Standard Level N-channel MOSFETs
- Enhanced Charge Pump for Internal High-side Supply
- Specific Pin for N-channel MOSFET Reverse Battery Protection
- Programmable Slew-rate, Dead-time and Over-current Level
- PWM Operation up to 25 kHz
- Active or Passive Freewheeling
- High-side or Low-side Freewheeling
- Configurable into Single H-bridge or Dual Half-bridges Mode
- 24-Bit SPI Interface
- Protection Against Short-circuit, Over-voltage, Under-voltage and Over-temperature
- TSSOP20 Package
- AEC-Q100 Qualified and PPAP Capable
- This is a Pb-free Device

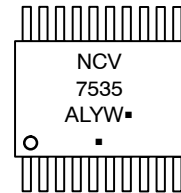
Typical Applications

- Replacing Systems with Relays by MOSFETs
- Motor Drivers



TSSOP20
CASE 948AD

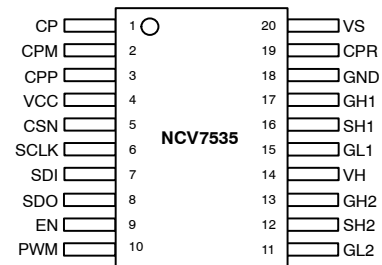
MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|----------------------|-----------------------|
| NCV7535DBR2G | TSSOP20 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Pin Type | Description |
|---------|----------|------------------------------------|---|
| 1 | CP | Analog output | Charge pump output for high-side gate drive supply |
| 2 | CPM | Analog output | Minus terminal for pump capacitor |
| 3 | CPP | Analog output | Plus terminal for pump capacitor |
| 4 | VCC | Supply input | Logic supply of the device |
| 5 | CSN | Digital input with pull-up | SPI chip select input |
| 6 | SCLK | Digital input with pull-down | SPI clock input |
| 7 | SDI | Digital input with pull-down | SPI data input |
| 8 | SDO | Digital push-pull output, tristate | SPI data output |
| 9 | EN | Digital input with pull-down | Enable input |
| 10 | PWM | Digital input with pull-down | Input for pulse width modulated driver duty cycle |
| 11 | GL2 | Analog output | Output to gate of low-side switch 2 |
| 12 | SH2 | Analog input output | Connection to source of high-side switch 2 |
| 13 | GH2 | Analog output | Output to gate of high-side switch 2 |
| 14 | VH | Analog input | Connection to drain of high-side switched for short circuit detection |
| 15 | GL1 | Analog output | Output to gate of low-side switch 1 |
| 16 | SH1 | Analog input output | Connection to source of high-side switch 1 |
| 17 | GH1 | Analog output | Output to gate of high-side switch 1 |
| 18 | GND | Ground | Ground connection |
| 19 | CPR | Analog output | Reverse Polarity N-FET Control Output |
| 20 | VS | Battery supply input | Power-supply of the device |

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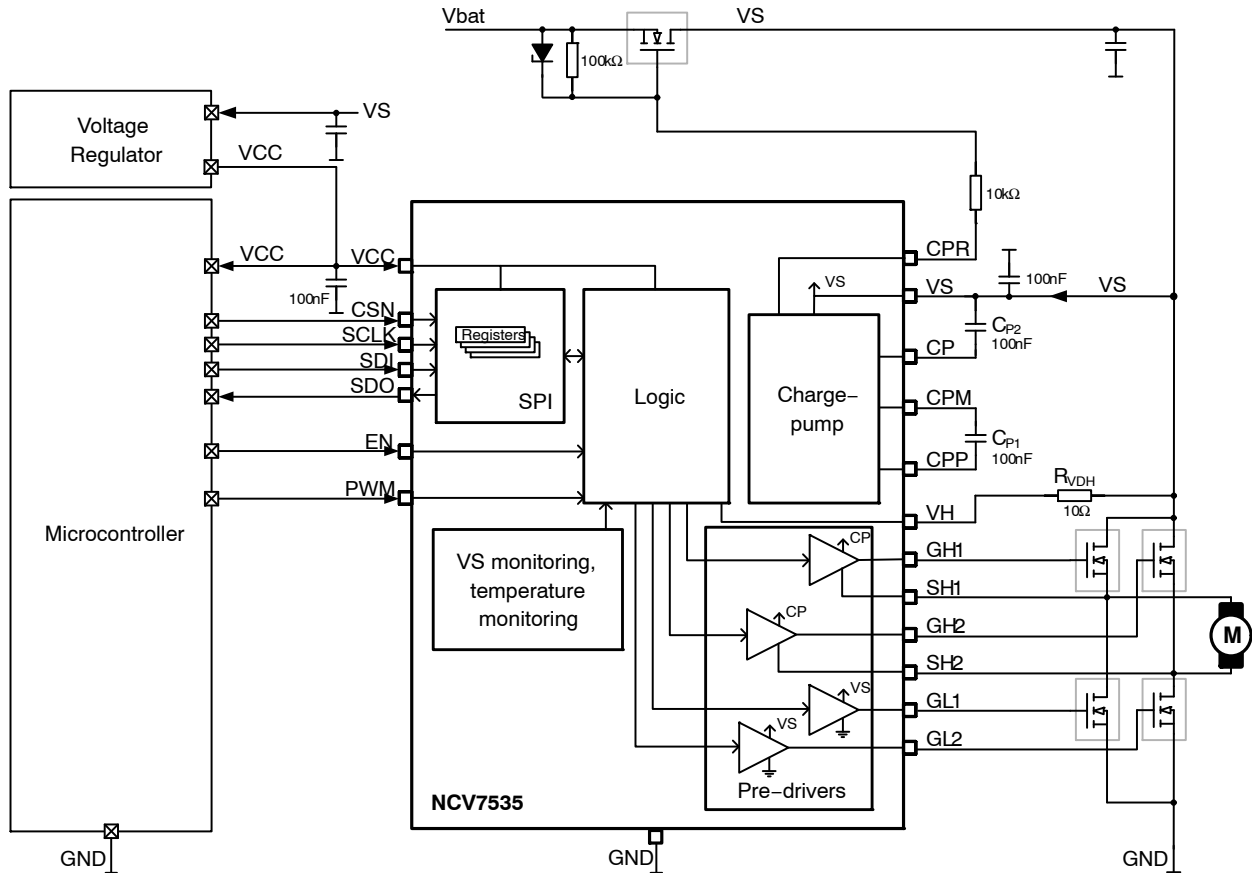


Figure 1. Block Diagram and Typical Application Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|---------------|--|----------------|--------------------------|------|
| Vmax_VS | Power supply voltage | -0.3 | 40 | V |
| Vmax_CPR | Reverse Polarity FET Control Output Voltage | -25 Vs - 25 | 40 Vs + 16 | V |
| Vmax_CP, CPP | Positive Charge-pump CP and CPP voltages | -0.3 | 40 | V |
| Vmax_CPM | Negative Charge-pump voltage | -0.3 | VS + 0.3 | V |
| Vmax_GHx, SHx | Gate driver voltage transient, < 500 ns Gate driver voltage transient, < 10 s Gate driver voltage DC | -4 -2 -2 | 40 VS + 2 VS + 0.3 | V |
| Vmax_VGSx | Voltage difference V(GHx) - V(SHx) (high side Vgs), Qgate = 60 nC | -0.3 | 17 VS + 0.3 | V |
| Vmax_GLx | GLx pin voltage transient (low side Vgs) < 500 ns GLx pin voltage DC, Qgate = 60nC | -0.3 | 17 VS + 0.3 | V |
| Vmax_VH | Sense line for VS | -0.3 | 40 | V |
| Vmax_VCC | Logic supply | -0.3 | 5.5 | V |
| Vmax_digIO | DC voltage at digital pins - SDI, SDO, SCLK, PWM - CSN, EN | -0.3 -0.3 | VCC + 0.3 5.8 | V |
| Iinj_digIO | Injection current into VCC-related digital pins (SDI, SCLK, PWM) | | 1 | mA |
| MSL | Moisture Sensitivity Level | | 3 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|--------------------|------|
| $R_{\theta JL}$ $R_{\theta JA}$ | Thermal Characteristics Thermal Resistance, Junction-to-Lead Thermal Reference, Junction-to-Ambient | 60 130 (Note 1) | °C/W |

1. Values represent typical still air steady-state thermal performance on 1 oz. copper FR4 PCB 4 layers with 650 mm² copper area

Table 4. OPERATING RANGES

| Symbol | Parameter | Min | Max | Unit |
|-----------------|--|-----|------|------|
| Vop_VS_par, | Power supply voltage for valid parameter specifications | 6 | 18 | V |
| Vop_VS_func, VH | Power supply for correct functional behavior (see Note 2) | 5 | 28 | V |
| Vop_VGSx | Voltage difference GHx – SHx (Vgs), Qgate = 60 nC | 0 | 17 | V |
| Vop_GLx | GLx pin voltage range DC, Qgate = 60 nC (voltage internally limited during flyback) | 0 | 17 | V |
| Vop_VCC | Logic supply | 4.5 | 5.25 | V |
| Vop_digIO | DC voltage at digital pins (SDI, SDO, SCLK, CSN, PWM, EN) | 0 | VCC | V |
| Tj_op | Junction temperature | -40 | +150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The device must see a VS voltage above VS Under-voltage (Vuv_vs) and below VS Over-voltage (Vov_vs) detection levels to drive the H-bridge normally.

Table 5. ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V, 4.5 V ≤ VCC ≤ 5.25 V, -40°C ≤ Tj ≤ 150°C; unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------------------|---------------------------------|--|-----|-----|---------|----------|
| Vs, VCC SUPPLIES | | | | | | |
| Vs | Supply Voltage | Functional (see Note 3) | 5 | | 28 | V |
| | | Parameter specification | 6 | | 18 | |
| I_VS_Standby | VS consumption in Standby mode | Standby mode, VS = 12 V, VCC = 0 V or EN = 0, Charge-pump off No SPI communication, Tj = 85°C (see Note 4) | | 10 | 20 | μA |
| I_Vcc_Standby | VCC consumption in Standby mode | Standby mode, VS = 12 V, VCC = 5 V, EN = 0, Charge-pump off No SPI communication, Tj = 85°C (see Note 4) | | 10 | 20 | μA |
| I_VS_Active | VS consumption in Active mode | Active mode, VS = 12 V, VCC = 5 V, external H-bridge static, No SPI communication fPWM = 25 kHz, Qg = 60 nC | | | 4 10 | mA mA |
| I_Vcc_Active | VCC consumption in Active mode | Active mode | | 3.3 | 8 | mA |

OVERVOLTAGE AND UNDERVOLTAGE DETECTION

| | | | | | | |
|-------------|-----------------------------|--------------------------|-----|------|-----|---|
| Vuv_vs(on) | VS Under-Voltage detection | VS increasing | 5.6 | | 6.4 | V |
| Vuv_vs(off) | | VS decreasing | 5.0 | | 5.7 | |
| Vuv_vs(hys) | VS Under-Voltage hysteresis | Vuv_vs(on) – Vuv_vs(off) | | 0.65 | | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- The device must see a VS voltage above VS Under-voltage (Vuv_vs) and below VS Over-voltage (Vov_vs) detection levels to drive the H-bridge normally.
- The Load must not have path to VS
- ICP is internal load due to H-bridge switching (no external load)
- Internal propagation delay and re-synchronization time are not included
- Over-current is not detected during the transitions

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Table 5. ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V, 4.5 V ≤ VCC ≤ 5.25 V, -40°C ≤ Tj ≤ 150°C; unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

OVERVOLTAGE AND UNDERVOLTAGE DETECTION

| | | | | | | |
|--------------|---|--|------|-----|------|----|
| Vov_vs(off) | VS Over-Voltage detection | VS increasing | 22.5 | 24 | 25.5 | V |
| Vov_vs(on) | | VS decreasing | 20.5 | 22 | 23.5 | |
| Vov_vs(hys) | VS Over-Voltage hysteresis | Vov_vs(off) – Vov_vs(on) | | 2 | | V |
| Vuv_vcc(off) | VCC Under-Voltage detection | VCC increasing | | 3.0 | 3.2 | V |
| Vuv_vcc(on) | | VCC decreasing | 2.6 | 2.8 | | |
| Vuv_vcc(hys) | VCC Under-Voltage hysteresis | Vuv_vcc(off) – Vuv_vcc(on) | | 0.2 | | V |
| td_uvov | VS Under-Voltage / Over-Voltage filter time | Time to set the power supply fail bit UOV_OC in the Global Status Byte | 48 | 76 | 125 | μs |

CHARGE-PUMP

| | | | | | | |
|-------|---|--|--------|-----|---------|-----|
| fCP | Charge pump frequency | | 300 | 425 | 550 | kHz |
| Vcp1 | Charge pump output voltage1 | VS > 10.5 V, Icp = -10 mA (see Note 5), Cp1 = Cp2 = 100 nF | VS+8 | | VS+15.1 | V |
| Vcp2 | Charge pump output voltage2 | VS > 6 V, Icp = -5 mA, Cp1 = Cp2 = 100 nF | VS+4.5 | | | V |
| R_CPR | Switch impedance between CPR and CP | tested at 0.5 mA | 250 | 300 | 420 | Ω |
| I_CPR | Current capability of Reverse Polarity Gate Control | | | | 1 | mA |

GATE OUTPUTS

| | | | | | | |
|---------------|--|---|------|------|-----|------|
| dVGx_fast | Slew Rate of gate driver | VS=13.5 V, SPI bit CONFIG.SRF=1, Gate charge ≤ 60 nC | | 30 | | V/μs |
| dVGx_slow | Slew Rate of gate driver | VS=13.5 V, SPI bit CONFIG.SRF=0, Gate charge ≤ 60 nC | | 5 | | V/μs |
| lpull_SHx_act | SH1/2 pull-up current in Active mode, H-Bridge off | SHx = 1.2 V | -240 | -140 | -60 | μA |
| fPWM | PWM frequency | | | | 25 | kHz |
| tprop | Propagation delay of PWM rising or falling edge to gate activation | Measured at 50% PWM input signal to 10% rising or 90% falling edge of the gates Measured with dVGxfast & 5 nF load | 200 | 500 | 800 | ns |
| tjitter | Jitter versus PWM rising or falling edge to gate activations | Measured at 50% PWM input signal to 10% rising or 90% falling edge of the gates Measured with dVGxfast & 5 nF load | -150 | 0 | 150 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- The device must see a VS voltage above VS Under-voltage (Vuv_vs) and below VS Over-voltage (Vov_vs) detection levels to drive the H-bridge normally.
- The Load must not have path to VS
- ICP is internal load due to H-bridge switching (no external load)
- Internal propagation delay and re-synchronization time are not included
- Over-current is not detected during the transitions

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Table 5. ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V, 4.5 V ≤ VCC ≤ 5.25 V, -40°C ≤ T_J ≤ 150°C; unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---------------------|--|--|------|--|------|------|
| GATE OUTPUTS | | | | | | |
| tdLH | Additional cross conduction protection time, low-to-high transition (Note 6) | Programmable via SPI bits CONFIG.NOCRLH[3:0] | -33% | 0.25 0.5 0.75 1 1.25 1.5 1.75 2 2.25 2.5 2.75 3 3.25 3.5 3.75 4 | +33% | μs |
| tdHL | Additional cross conduction protection time, high-to-low transition (Note 6) | Programmable via SPI bits CONFIG.NOCRHL[3:0] | -33% | 0.25 0.5 0.75 1 1.25 1.5 1.75 2 2.25 2.5 2.75 3 3.25 3.5 3.75 4 | +33% | μs |

OVER CURRENT DETECTION OF THE EXTERNAL H-BRIDGE

| | | | | | | |
|-----------------|---|--|---------------|--|---------------|----|
| Vthoc | Programmable Over-Current detection threshold of external V _{ds} V(VH)-V(SH _x) for high side and V(SH _x) versus Ground for low side (Note 7) | Programmable via SPI bits CONFIG.OCTH[2:0] | -10% -0.03 | 0.25 0.5 0.75 1 1.25 1.5 1.75 2 | +10% +0.03 | V |
| t _{oc} | Filter time for OC protection (Note 7) | | 4 | 6 | 12 | μs |
| I _{VH} | VH pin input current | VS = 12 V, SH _x = 0 V or SH _x = VS | | | 200 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The device must see a VS voltage above VS Under-voltage (V_{uv_vs}) and below VS Over-voltage (V_{ov_vs}) detection levels to drive the H-bridge normally.
4. The Load must not have path to VS
5. ICP is internal load due to H-bridge switching (no external load)
6. Internal propagation delay and re-synchronization time are not included
7. Over-current is not detected during the transitions

Table 5. ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V, 4.5 V ≤ VCC ≤ 5.25 V, -40°C ≤ Tj ≤ 150°C; unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|--|------------------------------------|---------|-----|---------|------|
| DIGITAL INPUTS CSN, SCLK, PWM, SDI, EN | | | | | | |
| Vinl | Input low level | VCC = 5 V | | | 30% VCC | V |
| Vinh | Input high level | VCC = 5 V | 70% VCC | | | V |
| Vin_hyst | Input hysteresis | VCC = 5 V | 6% VCC | | | V |
| Rcsn_pu | CSN pull-up resistor | VCC = 5 V, 0 V < Vcsn < 70% VCC | 30 | 120 | 250 | kΩ |
| Rsclk_pd | SCLK pull-down resistor | VCC = 5 V, Vsclk = 1.5 V | 30 | 60 | 220 | kΩ |
| Rsd_i_pd | SDI pull-down resistor | VCC = 5 V, Vsdi = 1.5 V | 30 | 60 | 220 | kΩ |
| Rpwm_pd | PWM pull-down resistor | VCC = 5 V Vpwm = 1.5 V | 30 | 60 | 220 | kΩ |
| Ren_pd | EN pull-down resistor | VCC = 5 V Ven = 1.5 V | 30 | 120 | 250 | kΩ |
| Ccsn/sclk/pwm | Pin capacitance (not tested in production, based on design and characterization) | 0 V < Vpin < VCC | | | 10 | pF |

DIGITAL OUTPUT SDO

| | | | | | | |
|-----------|---|---------------------------------|---------|--|---------|----|
| Vsdol | Output low level | Isdo = 5 mA | | | 20% VCC | V |
| Vsdoh | Output high level | Isdo = -5 mA | 80% VCC | | | V |
| Ileak_sdo | Tristate leakage current | Vcsn = VCC, 0 V < Vsdo < VCC | -10 | | 10 | μA |
| Csdo | Tristate input capacitance (not tested, based on design and characterization) | Vcsn = VCC, 0 V < Vsdo < VCC | | | 10 | pF |

DIGITAL INPUTS EN, CSN, SCLK, SDI; TIMING

| | | | | | | |
|-----------|---|-----------|-----|------|-----|----|
| tsclk | Clock period | VCC = 5 V | | 1000 | | ns |
| tsclk_h | Clock high time | | 115 | | | ns |
| tsclk_l | Clock low time | | 115 | | | ns |
| tset_csn | CSN setup time, CSN low before rising edge of SCLK | | 400 | | | ns |
| tset_sclk | SCLK setup time, SCLK low before rising edge of CSN | | 400 | | | ns |
| tset_si | SDI setup time | | 200 | | | ns |
| thold_si | SDI hold time | | 200 | | | ns |
| tr_in | Rise time of input signal SDI, SCLK, CSN | | | | 100 | ns |
| tf_in | Fall time of input signal SDI, SCLK, CSN | | | | 100 | ns |

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- The device must see a VS voltage above VS Under-voltage (Vuv_vs) and below VS Over-voltage (Vov_vs) detection levels to drive the H-bridge normally.
- The Load must not have path to VS
- ICP is internal load due to H-bridge switching (no external load)
- Internal propagation delay and re-synchronization time are not included
- Over-current is not detected during the transitions

Table 5. ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V, 4.5 V ≤ VCC ≤ 5.25 V, -40°C ≤ Tj ≤ 150°C; unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|-----------------|-----|-----|-----|------|
| DIGITAL INPUTS EN, CSN, SCLK, SDI; TIMING | | | | | | |
| tcsn_hi_stdby | Minimum CSN high time, switching from Standby mode | | | 5 | 10 | μs |
| tcsn_hi_min | Minimum CSN high time, Active mode | | | 2 | 4 | μs |
| ten_neg | Minimum EN negative pulse which is seen as 0 (after synchronization) | | 325 | | | ns |
| tcsn_hi_en_hi | Minimum time between CSN high and EN high edge | | 100 | | | ns |
| ten_hi_csn_lo | Minimum time between EN high and CSN low edge | | 100 | | | ns |

OPERATING MODES TIMING

| | | | | | | |
|-----------|---|--|--|-----|------|----|
| tsact | Time delay from Standby (CSN rising edge MODE=1 and EN=1) into Active mode (NRDY=0) | | | 240 | 340 | μs |
| tacts | Time to place device from Active to Standby after rising edge CSN and MODE=0 or EN=0 | | | | 13.5 | μs |
| tsrt_stby | Time to place device back to Standby from Startup phase if after 1 st SPI communication MODE=0 or EN=0 | | | | 8 | μs |

THERMAL PROTECTION

| | | | | | | |
|----------------------|---|-----------------------|-----|-----|-----|----|
| Tj _{sd_on} | Thermal shutdown threshold, Tj increasing | Junction temperature | 160 | 175 | 195 | °C |
| Tj _{sd_off} | Thermal shutdown threshold, Tj decreasing | Junction temperature | 155 | | | °C |
| Tj _{sd_hys} | Thermal shutdown hysteresis | | | 5 | | °C |
| td_tx | Filter time for thermal shutdown | TSD Global Status bit | 10 | | 125 | μs |

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- The Load must not have path to VS
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- Over-current is not detected during the transitions

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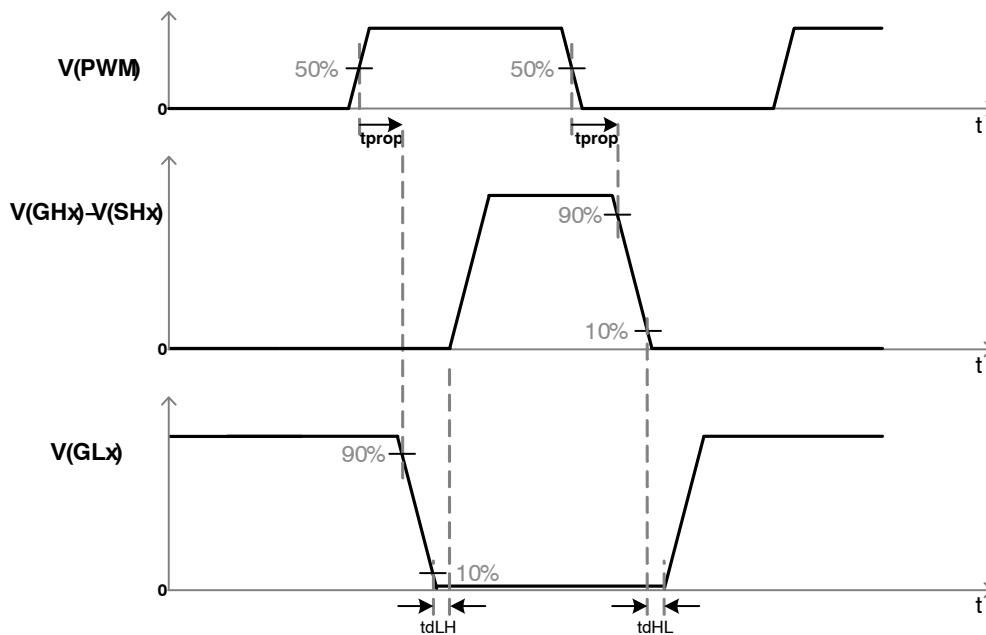


Figure 2. Cross Conduction Protection Timing

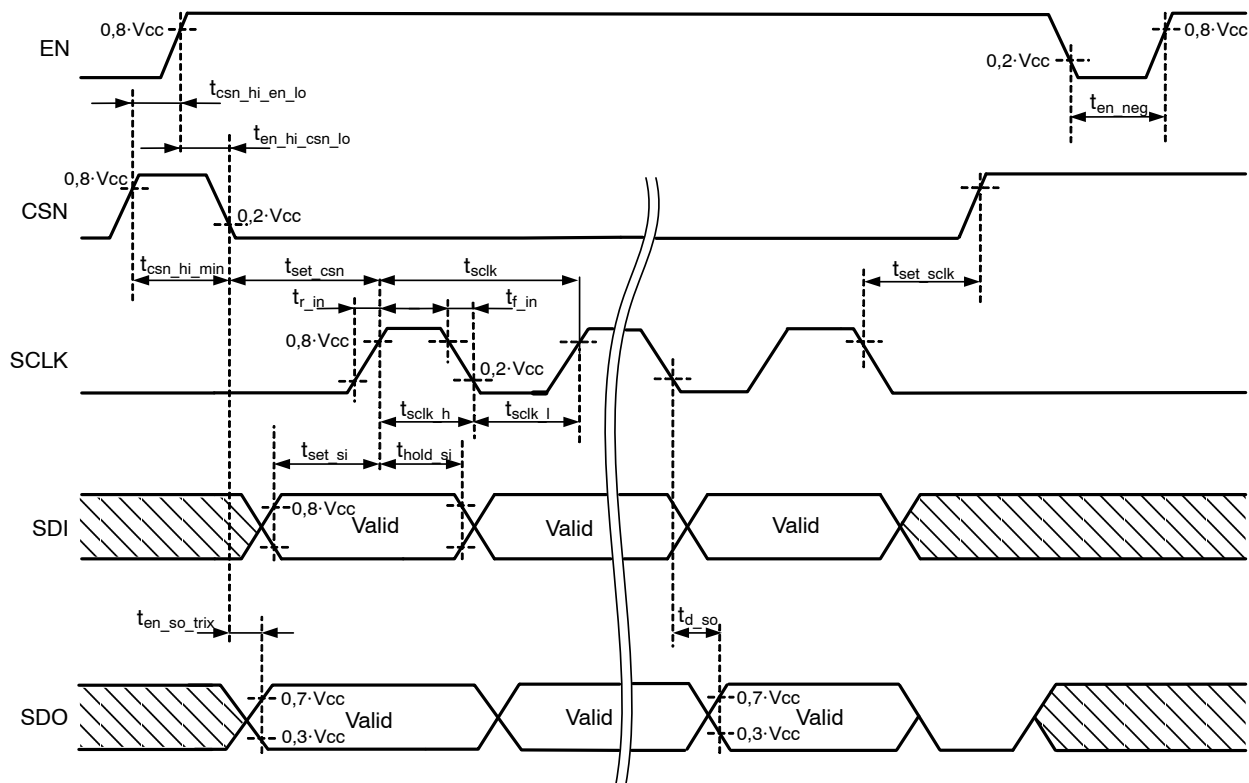


Figure 3. SPI Timing Parameters

Detailed Operating Description

Power Up/Down Control

In order to prevent uncontrolled operation of the device during power/up down, an under-voltage lockout feature is implemented. Both supply voltages (VCC and VS) are monitored for under-voltage conditions supporting a safe power-up transition. When VS drops below the under-voltage threshold $V_{uv_vs(off)}$ (VS under-voltage threshold) all output transistors are switched OFF.

Mode Control

Wake-up and Mode Control

Two different modes are available:

- Active mode
- Standby mode

After a power-up of VCC, the device starts in a Standby mode (VCC in Under-Voltage). Pulling the chip-select signal CSN to low level and pulling-up the enable signal EN to high level causes the device state to change into a Start-Up mode, waiting for setting SPI bit $CONTROL_0.MODE = 1$ (analog part active).

If bit MODE remains reset (0), the device returns to the Standby mode after an internal delay $tsrt_stby$, clearing all register content and keeping all output transistors OFF.

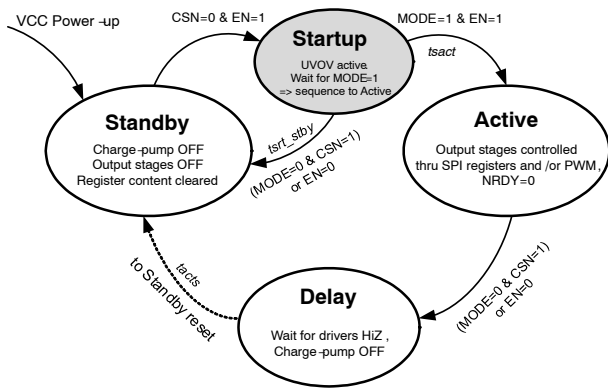


Figure 4. Mode Transitions Diagram

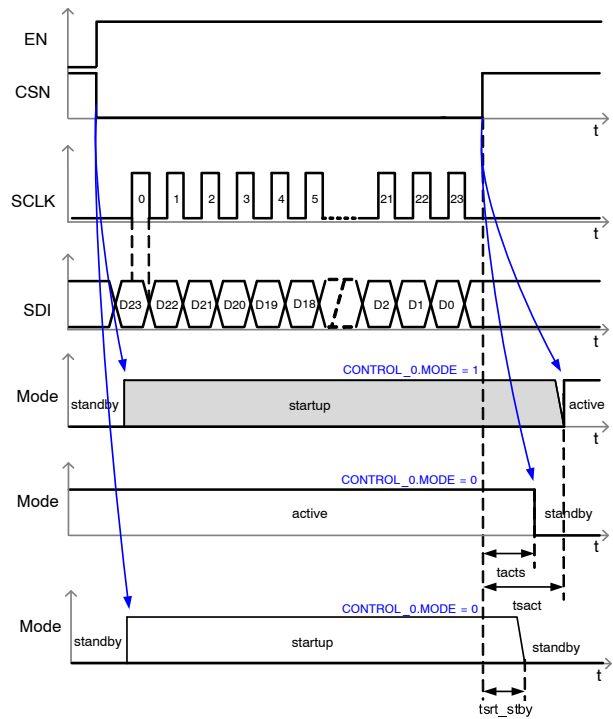


Figure 5. Mode Timing Diagram

Cross-current Protection and PWM Control

The pre-drivers are protected against cross-currents by internal circuitry. If one driver is turned off (LS or HS), the activation of the other driver of the same output will be automatically delayed by the cross current protection mechanism until the active driver is safely turned off.

The Control signals required for the activations under PWM operation are described below:

PWM low will place the bridge into a freewheeling condition according to the $CONTROL_0.FWH$ bit setting:

- $FWH = 1$: “PWM low” will switch off the low side transistor and will, depending on FWA, turn on the high side ($FWA=1$) for active freewheeling or leave the transistor open ($FWA = 0$) for passive freewheeling
- $FWH = 0$: “PWM low” will switch off the high side transistor and will, depending on FWA, turn on the low side ($FWA=1$) for active freewheeling or leave the transistor open ($FWA = 0$) for passive freewheeling

The device can be used with SPI mode control only – then the PWM input pin must be forced to a high level.

| | | FWA=1 (Active free-wheeling) | | FWA=0 (Passive free-wheeling) | |
|------------------------------|------------------------------------|---------------------------------|-------|----------------------------------|-------|
| | | PWM=1 | PWM=0 | PWM=1 | PWM=0 |
| HS1=1, HS2=0 LS1=0, LS2=1 | FWH=1 (High-side free-wheeling) | | | | |
| | FWH=0 (Low-side free-wheeling) | | | | |
| HS1=0, HS2=1 LS1=1, LS2=0 | FWH=1 (High-side free-wheeling) | | | | |
| | FWH=0 (Low-side free-wheeling) | | | | |
| HS1=0, HS2=0 LS1=1, LS2=1 | FWH=x | | | | |
| HS1=1, HS2=1 LS1=0, LS2=0 | FWH=x | | | | |
| Any other HS/LS setting | FWH=x | All transistors off | | | |

Figure 6. Bridge Configurations

Over-Voltage and Under-Voltage Shutdown

If the supply voltage VS rises above the switch off voltage $V_{ov_vs(off)}$ or falls below $V_{uv_vs(off)}$, all output transistors are switched OFF.

Over-Temperature Shutdown

The device provides an over-temperature protection. If the junction temperature rises above T_{jsd_on} threshold, the thermal shutdown bit TSD is set and all the output transistors are switched OFF. The shutdown delay for the over-temperature is t_{d_tx} . The output channels can be re-enabled after the device is cooled down and the TSD flag has been reset by the microcontroller by setting $CONTROL_0.MODE = 0$.

Over-Current Shutdown

Over Current is detected by the device when the drain-source voltage (Vds) of the external N-MOSFETs saturates. Above the Over-Current threshold (programmable via SPI register bits $CONFIG.OCTH[2:0]$), the over current is detected. During the bridge transitions, the error detection is masked (Vds can be higher than the OCTH during the slopes).

If the device is in full-bridge mode ($CONFIG.HALF_HB = 0$), the full bridge is disabled in case of over-current.

Otherwise, if the device is in half-bridge mode ($CONFIG.HALF_HB = 1$), only the half-bridge in affected by the over-current is disabled.

SPI Control

General Description

The 4-wire SPI interface establishes a full duplex synchronous serial communication link between the NCV7535 and the application's microcontroller. The NCV7535 always operates in slave mode whereas the controller provides the master function. A SPI access is performed by applying an active-low slave select signal at CSN. SDI is the data input, SDO the data output. The SPI master provides the clock to the NCV7535 via the SCLK input. The digital input data is sampled at the rising edge at SCLK. The data output SDO is in high impedance state (tri-state) when CSN is high. To readout the global error flag without sending a complete SPI frame, SDO indicates the corresponding value as soon as CSN is set to active. With the first rising edge at SCLK after the high-to-low transition of CSN, the content of the selected register is transferred into the output shift register.

The NCV7535 provides one control registers ($CONTROL_0$), one status register ($STATUS_0$) and one general configuration register ($CONFIG$). Each of these register contains 16-bit data, together with the 8-bit frame header (access type, register address), the SPI frame length is therefore 24 bits. In addition to the read/write accessible registers, the NCV7535 provides five 8-bit ID registers (ID_HEADER , $ID_VERSION$, $ID_CODE1/2$ and $ID_SPI-FRAME$) with 8-bit data length. The content of these registers can still be read out by a 24-bit access, the data is then transferred in the MSB section of the data frame.

SPI Frame Format

Figure 7 shows the general format of the NCV7535 SPI frame.

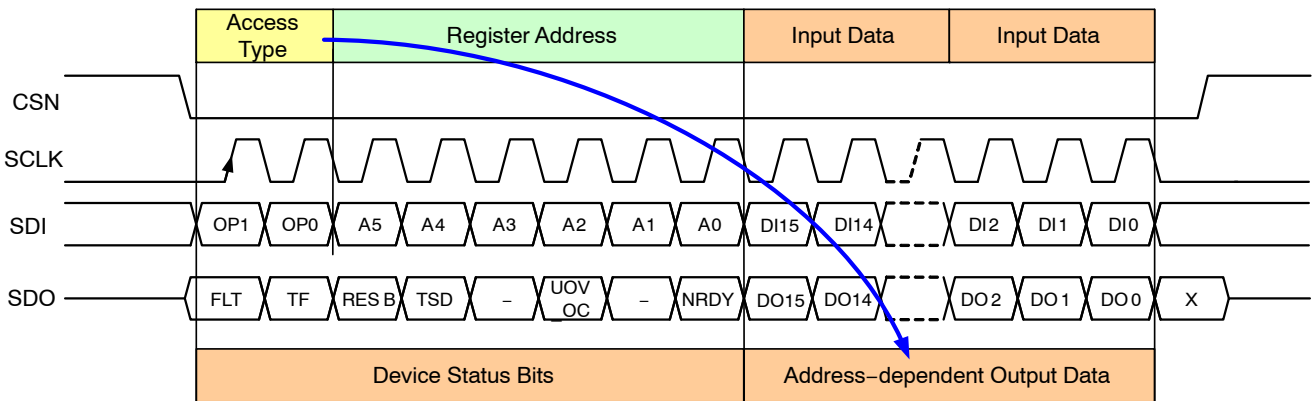


Figure 7. SPI Frame Format

24-bit SPI Interface

Both 24-bit input and output data are MSB first. Each SPI-input frame consists of a command byte followed by two data bytes. The data returned on SDO within the same frame always starts with the global status byte. It provides

general status information about the device. It is then followed by 2 data bytes (in-frame response) which content depends on the information transmitted in the command byte. For write access cycles, the global status byte is followed by the previous content of the addressed register.

Chip Select Not (CSN)

CSN is the SPI input pin which controls the data transfer of the device. When CSN is high, no data transfer is possible and the output pin SDO is set to high impedance. If CSN goes low, the serial data transfer is allowed and can be started. The communication ends when CSN goes high again.

Serial Clock (SCLK)

If CSN is set to low, the communication starts with the rising edge of the SCLK input pin. At each rising edge of SCLK, the data at the input pin Serial IN (SDI) is latched. The data is shifted out thru the data output pin SDO after the falling edges of SCLK. The clock SCLK must be active only within the frame time, means when CSN is low. The correct transmission is monitored by counting the number of clock pulses during the communication frame. If the number of SCLK pulses does not correspond to the frame width indicated in the SPI-frame-ID (Chip ID Register, address 3Eh) the frame will be ignored and the communication failure bit “TF” in the global status byte will be set. Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

Serial Data In (SDI)

During the rising edges of SCLK (CSN is low), the data is transferred into the device thru the input pin SDI in a serial way. The device features a stuck-at-one detection, thus upon detection of a command = FFFFFFFh, the device will be forced into the Standby mode. All output drivers are switched off.

Serial Data Out (SDO)

The SDO data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global status bit, FLT (Global Error Flag). The first rising edge of the SCLK input after a high to low transition of the CSN pin will transfer the content of the selected register into the data out shift register. Each subsequent falling edge of the SCLK will shift the next bit thru SDO out of the device.

Command Byte / Global Status Byte

Each communication frame starts with a command byte (Table 6). It consists of an operation code (OP[1:0]) which specifies the type of operation (Read, Write, Read & Clear, Readout Device Information) and a six bit address (A[5:0]). If less than six address bits are required, the remaining bits are unused but are reserved. Both Write and Read mode allow access to the internal registers of the device. A “Read & Clear”-access is used to read a status register and subsequently clear its content. The “Read Device Information” allows to read out device related information such as ID-Header, Product Code, Silicon Version and Category and the SPI-frame ID. While receiving the command byte, the global status byte is transmitted to the microcontroller. It contains global fault information for the device.

ID Register

Chip ID Information is stored in five special 8-bit ID. The content can be read out at the beginning of the communication.

Table 6. COMMAND BYTE (IN) / GLOBAL STATUS BYTE (OUT)

| Bit | Command Byte (IN) / Global Status Byte (OUT) | | | | | | | |
|-------------|--|-----|------|-----|----|--------|----|------|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NCV7535 IN | OP1 | OP0 | A5 | A4 | A3 | A2 | A1 | A0 |
| NCV7535 OUT | FLT | TF | RESB | TSD | - | UOV_OC | - | NRDY |
| Reset Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 7. COMMAND BYTE, ACCESS MODE

| OP1 | OP0 | Description |
|-----|-----|----------------------------|
| 0 | 0 | Write Access (W) |
| 0 | 1 | Read Access (R) |
| 1 | 0 | Read and Clear Access (RC) |
| 1 | 1 | Read Device ID (RDID) |

Table 8. COMMAND BYTE, REGISTER ADDRESS

| A[5:0] | Access | Description | Content |
|--------|--------|-------------------------------|--|
| 00h | R/W | Control Register CONTROL_0 | Device mode control, external H-Bridge outputs control |
| 10h | R/RC | Status Register STATUS_0 | Pre-driver diagnosis |
| 3Fh | R/W | Configuration Register CONFIG | Mask bits for global fault bits, PWM mapping |

Table 9. GLOBAL STATUS BYTE CONTENT

| FLT | Global Fault Bit | |
|--------|------------------------------------|--|
| 0 | No fault Condition | Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB bit inverted). It is reflected via the SDO pin while CSN is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSN is held low. This operation does not cause the Transmission error Flag in the Global Status Byte to be set. |
| 1 | Fault Condition | |
| TF | SPI Transmission Error | |
| 0 | No Error | If the number of clock pulses within the previous frame was unequal 0 (FLT polling) or 24. The frame was ignored and this flag was set. |
| 1 | Error | |
| RESB | Reset Bar (Active low) | |
| 0 | Reset | Bit is set to "0" after a Power-on-Reset or a stuck-at-1 fault at SI (SPI-input data = FFFFFFFh) has been detected. All outputs are disabled. |
| 1 | Normal Operation | |
| TSD | Over-temperature Shutdown | |
| 0 | No Thermal Shutdown | Thermal Shutdown Status indication. In case of a Thermal Shutdown, all output drivers including the charge pump output are deactivated (high impedance). The TSD bit has to be cleared thru a SW reset to reactivate the output drivers and the chargepump output. |
| 1 | Thermal Shutdown | |
| UOV_OC | VS Monitoring, Over-current Status | |
| 0 | No Fault | This bit represents a logical OR combination of under-/overvoltage signals (VS) and overcurrent signals. |
| 1 | Fault | |
| NRDY | Not Ready | |
| 0 | Device Ready | This bit indicates that the drivers cannot be activated and the chargepump is switched off. After transition from Standby to Active mode, an internal timer is started to allow the internal chargepump to settle before any outputs can be activated. This bit is cleared automatically after the startup is completed. |
| 1 | Device Not Ready | |

Table 10. CHIP ID INFORMATION

| A[5:0] | Access | Description | Content |
|--------|--------|----------------|---------|
| 00h | R | ID header | 4300h |
| 01h | R | Version | 0100h |
| 02h | R | Product Code 1 | 7500h |
| 03h | R | Product Code 2 | 3500h |
| 3Eh | R | SPI Frame ID | 0200h |

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|------|
| Access type | - | - | - | - | - | - | RW | RW | RW | RW | - | RW | RW | RW | RW | RW |
| Bit name | - | - | - | - | - | - | HS1 | LS1 | HS2 | LS2 | - | FWH | FWA | OVR | UVR | MODE |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| HS/LS Outputs Control | HSx | LSx | Description | Remark |
|-----------------------|-----|-----|-----------------|--|
| | 0 | 0 | default | Activating both HS and LS at the same time is prevented by the internal logic. High-side or low-side freewheeling configuration is performed by FWH and FWA SPI bits |
| | 0 | 1 | LSx enabled | |
| | 1 | 0 | HSx enabled | |
| | 1 | 1 | Gate driver OFF | |

| Freewheeling High side or low side | FWH | Description | Remark |
|------------------------------------|-----|-------------|------------------------|
| | 0 | default | Freewheeling Low side |
| | 1 | | Freewheeling High side |

| Freewheeling Active or passive | FWA | Description | Remark |
|--------------------------------|-----|-------------|----------------------|
| | 0 | default | Passive freewheeling |
| | 1 | | Active freewheeling |

| Over-voltage Recovery | OVR | Description | Remark |
|-----------------------|-----|-------------|--|
| | 0 | default | Over-voltage Recovery function enabled |
| | 1 | | No Over-voltage Recovery |

| Under-voltage Recovery | UVR | Description | Remark |
|------------------------|-----|-------------|---|
| | 0 | default | Under-voltage Recovery function enabled |
| | 1 | | No Under-voltage Recovery |

| Mode Control | MODE | Description | Remark |
|--------------|------|-------------|---------|
| | 0 | default | Standby |
| | 1 | | Active |

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STATUS_0 Register

Address: 10h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----|-----|-----|-----|-----|-----|--------|--------|--------|--------|----|----|------|------|----|----|
| Access type | - | - | - | - | - | - | R/RC | R/RC | R/RC | R/RC | - | - | R/RC | R/RC | - | - |
| Bit name | - | - | - | - | - | - | OC HS1 | OC LS1 | OC HS2 | OC LS2 | - | - | VSUV | VSOV | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Over-current detection | OCx | Description | Remark |
|------------------------|-----------------------|--------------------------|--|
| | 0 | No over-current detected | During an over-current event in one of the HS or LS, the belonging over-current status bit STATUS_0.OCx is set and the dedicated output is switched off. (The global status bit UOV_OC is set, also). To reactivate the output stage again, the microcontroller has to clear the OC failure bit. |
| 1 | Over-current detected | | |

| Vs Under-voltage | VSUV | Description | Remark |
|------------------|------------------------|---------------------------|--|
| | 0 | No under-voltage detected | In case of a Vs under-voltage event, the output stages will be deactivated immediately and the corresponding failure flag will be set and latched. By default (CONTROL_0.UVR cleared) the output stages will be reactivated automatically after Vs is recovered. |
| 1 | Under-voltage detected | | |

| Vs Over-voltage | VSOV | Description | Remark |
|-----------------|----------------------|-------------------------|---|
| | 0 | No overvoltage detected | In case of a Vs over-voltage event, the output stages will be deactivated immediately and the corresponding failure flag will be set and latched. By default (CONTROL_0.OVR cleared) the output stages will be reactivated automatically after Vs is recovered. |
| 1 | Overvoltage detected | | |

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CONFIG Register

Address: 3Fh

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|----------|----------|--------|--------|--------|---------|-----|----|----|----|
| Access type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | - | - | - |
| Bit name | NOCR LH3 | NOCR LH2 | NOCR LH1 | NOCR LH0 | NOCR HL3 | NOCR HL2 | NOCR HL1 | NOCR HL0 | OCTH 2 | OCTH 1 | OCTH 0 | HALF HB | SRF | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| No-Crossing Timing Configuration | NOCR LH3 | NOCR LH2 | NOCR LH1 | NOCR LH0 | | Description | Remarks |
|----------------------------------|----------|----------|----------|----------|--|----------------------------------|---------|
| | 0 | 0 | 0 | 0 | | default | |
| 0 | 0 | 0 | 0 | 1 | | No-crossing limit = 500 ns | |
| 0 | 0 | 0 | 1 | 0 | | No-crossing limit = 750 ns | |
| 0 | 0 | 0 | 1 | 1 | | No-crossing limit = 1 μ s | |
| 0 | 1 | 0 | 0 | 0 | | No-crossing limit = 1.25 μ s | |
| 0 | 1 | 0 | 0 | 1 | | No-crossing limit = 1.5 μ s | |
| 0 | 1 | 1 | 0 | 0 | | No-crossing limit = 1.75 μ s | |
| 0 | 1 | 1 | 1 | 1 | | No-crossing limit = 2 μ s | |
| 1 | 0 | 0 | 0 | 0 | | No-crossing limit = 2.25 μ s | |
| 1 | 0 | 0 | 0 | 1 | | No-crossing limit = 2.5 μ s | |
| 1 | 0 | 1 | 0 | 0 | | No-crossing limit = 2.75 μ s | |
| 1 | 0 | 1 | 1 | 1 | | No-crossing limit = 3 μ s | |
| 1 | 1 | 0 | 0 | 0 | | No-crossing limit = 3.25 μ s | |
| 1 | 1 | 0 | 0 | 1 | | No-crossing limit = 3.5 μ s | |
| 1 | 1 | 1 | 1 | 0 | | No-crossing limit = 3.75 μ s | |
| 1 | 1 | 1 | 1 | 1 | | No-crossing limit = 4 μ s | |

| No-Crossing Timing Configuration | NOCR HL3 | NOCR HL2 | NOCR HL1 | NOCR HL0 | | Description | Remarks |
|----------------------------------|----------|----------|----------|----------|--|----------------------------------|---------|
| | 0 | 0 | 0 | 0 | | default | |
| 0 | 0 | 0 | 0 | 1 | | No-crossing limit = 500 ns | |
| 0 | 0 | 0 | 1 | 0 | | No-crossing limit = 750 ns | |
| 0 | 0 | 0 | 1 | 1 | | No-crossing limit = 1 μ s | |
| 0 | 1 | 0 | 0 | 0 | | No-crossing limit = 1.25 μ s | |
| 0 | 1 | 0 | 0 | 1 | | No-crossing limit = 1.5 μ s | |
| 0 | 1 | 1 | 0 | 0 | | No-crossing limit = 1.75 μ s | |
| 0 | 1 | 1 | 1 | 1 | | No-crossing limit = 2 μ s | |
| 1 | 0 | 0 | 0 | 0 | | No-crossing limit = 2.25 μ s | |
| 1 | 0 | 0 | 0 | 1 | | No-crossing limit = 2.5 μ s | |
| 1 | 0 | 1 | 0 | 0 | | No-crossing limit = 2.75 μ s | |
| 1 | 0 | 1 | 1 | 1 | | No-crossing limit = 3 μ s | |
| 1 | 1 | 0 | 0 | 0 | | No-crossing limit = 3.25 μ s | |
| 1 | 1 | 0 | 0 | 1 | | No-crossing limit = 3.5 μ s | |
| 1 | 1 | 1 | 1 | 0 | | No-crossing limit = 3.75 μ s | |
| 1 | 1 | 1 | 1 | 1 | | No-crossing limit = 4 μ s | |

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| Over-Current threshold configuration | OCTH2 | OCTH1 | OCTH0 | | Description | Remark |
|--------------------------------------|-------|-------|-------|--------------------|-----------------------|---|
| | 0 | 0 | 0 | default | VDS OC limit = 0.25 V | Common setting value for high side & low side |
| | 0 | 0 | 1 | | VDS OC limit = 0.5 V | |
| | 0 | 1 | 0 | | VDS OC limit = 0.75 V | |
| | 0 | 1 | 1 | | VDS OC limit = 1 V | |
| | 1 | 0 | 0 | | VDS OC limit = 1.25 V | |
| | 1 | 0 | 1 | | VDS OC limit = 1.5 V | |
| | 1 | 1 | 0 | | VDS OC limit = 1.75 V | |
| 1 | 1 | 1 | | VDS OC limit = 2 V | | |

| Bridge configuration | HALF HB | | Description | Remark |
|----------------------|---------|---------|------------------------------|---|
| | 0 | default | Full H-Bridge configuration | See PWM control page 9 |
| | 1 | | 2 Half-Bridges configuration | Controlled by SPI only PWM, FWH, FWA are ignored |

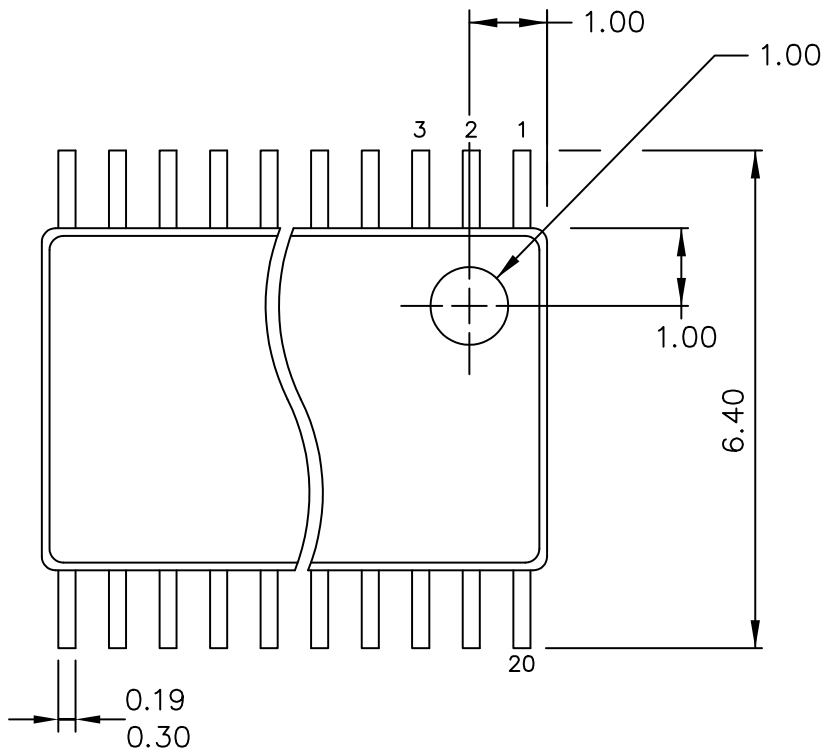
| Slew-Rate configuration | SRF | | Description | Remark |
|-------------------------|-----|---------|----------------|---|
| | 0 | default | Slow Slew Rate | Typical Slew Rate of gate driver of 5 V/ μ s |
| | 1 | | Fast Slew Rate | Typical Slew Rate of gate driver of 30 V/ μ s |

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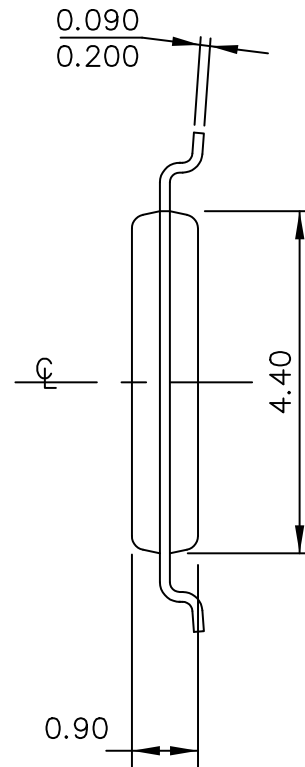
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CASE 948AD-01
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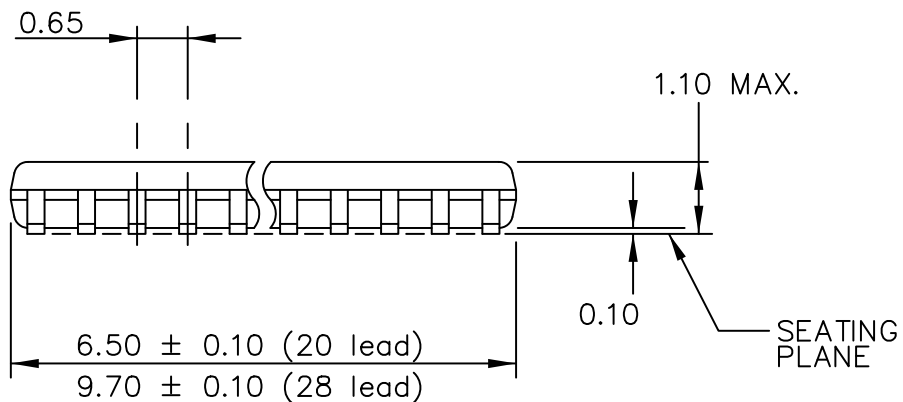
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TOP VIEW



END VIEW



SIDE VIEW

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