Tracking Regulator/Line Driver - Micropower, Low Dropout
200 mA

NCV8182C

The NCV8182C is a monolithic integrated low dropout tracking regulator designed to provides an adjustable buffered output voltage that closely tracks the reference input. The output delivers up to 250 mA while being able to be configured higher, lower or equal to the reference voltages.

The device has been designed to operate over a wide input and $V_{REF/EN}$ operating voltage range while still maintaining excellent DC characteristics. The NCV8182C is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand load dump transients and reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The $V_{REF/EN}$ lead serves two purposes. It is used to provide the input voltage as a reference for the output and it also can be pulled low to place the device in sleep mode.

Features

- Output Voltage Tracking Tolerance: max. ±10 mV
- Output Current: up to 250 mA
- Low Disable Current (Typ. 20 μA @ $V_{REF/EN}$ = 0 V)
- Low Dropout Voltage (Typ. 240 mV @ 200 mA)
- Wide Input and $V_{REF/EN}$ Operating Voltage Range
- Protection Features:
  - Current Limit
  - Thermal Shutdown
  - Reverse Polarity Protection
- Internally Fused Leads in SOIC−8 Package
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications (For safety applications refer to Figure 26)

- Engine Control Unit, Transmission Control Unit, Comfort Controls, Infotainment, Sensors, Local Controls, Tire Pressure Monitor, Machine Controls, Switch and Sensor Reading, Operator Interface Control

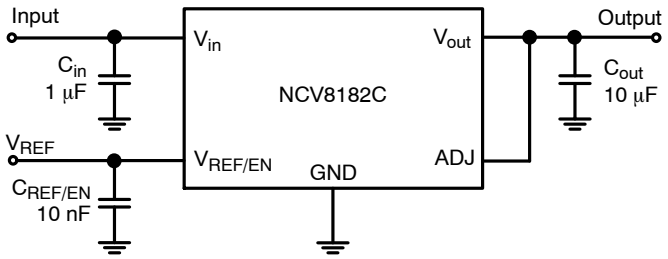

Figure 1. Application Circuit

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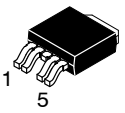
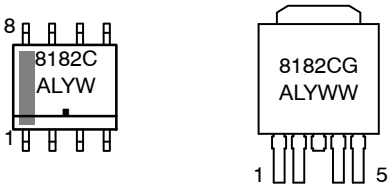
SOIC−8
CASE 751−07
(In Development)



DPAK−5
CASE 175AA

MARKING DIAGRAMS



A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

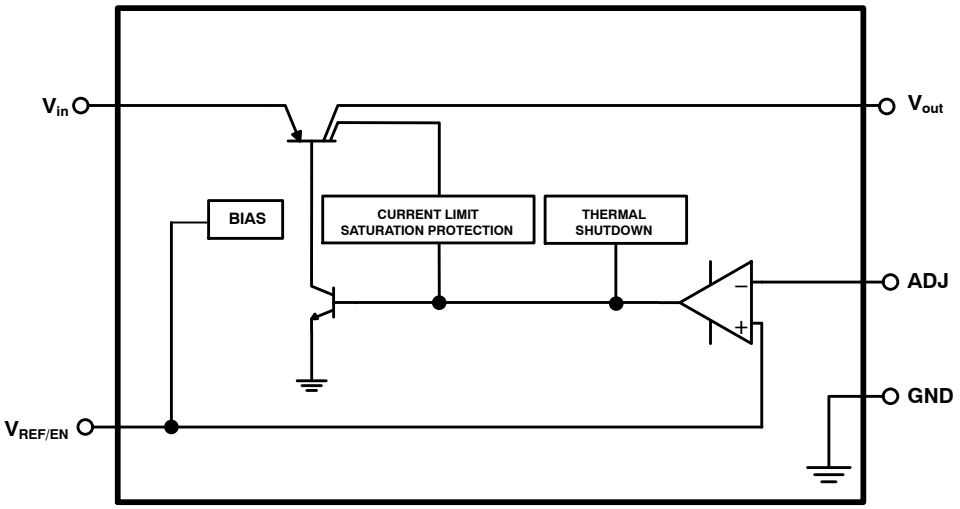
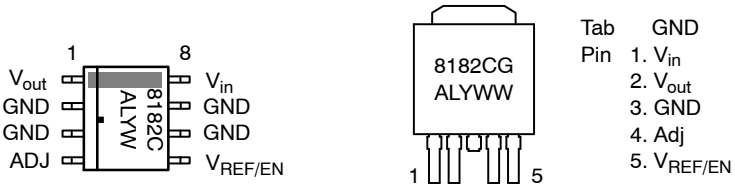


Figure 2. Simplified Block Diagram



SOIC−8 **DPAK−5**

Figure 3. Pin Connections

PIN FUNCTION DESCRIPTION

Pin No. SOIC−8	Pin No. DPAK−5	Pin Name	Description
8	1	V_{in}	Positive Power Supply Input. Connect 1.0 μF capacitor to ground.
1	2	V_{out}	Tracker Output Voltage. Connect 10 μF capacitor with ESR < 1.9 Ω to ground.
2, 3, 6, 7	3	GND	Power Supply Ground.
4	4	ADJ	Voltage Adjust Input. The adjust input can be connected directly to output pin for V_{out} = $V_{REF/EN}$ or by a voltage divider for higher/lower output voltages. The adjust pin can be also connected to ground in case of using this device as a High−Side Driver.
5	5	$V_{REF/EN}$	Reference Voltage and ENABLE Input. Connect the reference to this pin. A low signal disables the IC; a high signal switches it on. The reference voltage can be connected directly or by a voltage divider for lower output voltages. Connect 10 nF capacitor to ground.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC (Note 1) DC	V_{in}	 −16	 45	V
Input Voltage (Note 2) Load Dump − Suppressed	U_S*	 −	 60	V
Output Voltage	V_{out}	−10	40	V
Reference Voltage / Enable Input DC DC	$V_{REF/EN}$	 −10	 40	V
Adjust Input Voltage DC DC	V_{ADJ}	 −10	 40	V
Maximum Junction Temperature	$T_{J(max)}$	−40	150	°C
Storage Temperature	T_{STG}	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class B according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level SOIC−8 (Note 5) DPAK−5	MSL	 1 1		−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
5. Device is under development. Values subject to change.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 (Note 5) Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Lead (Note 6)	 $R_{\theta JA}$ $R_{\psi JL2}$	 113 16	°C/W
Thermal Characteristics, SOIC−8 (Note 5) Thermal Resistance, Junction−to−Air (Note 7) Thermal Reference, Junction−to−Lead (Note 7)	 $R_{\theta JA}$ $R_{\psi JL2}$	 88 16	°C/W
Thermal Characteristics, DPAK−5 Thermal Resistance, Junction−to−Air (Note 6) Thermal Resistance, Junction−to−Case (Note 6)	 $R_{\theta JA}$ $R_{\theta JC}$	 62.7 8.3	°C/W
Thermal Characteristics, DPAK−5 Thermal Resistance, Junction−to−Air (Note 7) Thermal Resistance, Junction−to−Case (Note 7)	 $R_{\theta JA}$ $R_{\theta JC}$	 38.2 8.3	°C/W

6. Values based on 1s0p board with copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3.
7. Values based on 2s2p board with copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. 4 layers − according to JEDEC51.7.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}	3.4	35	V
Reference Voltage / Enable Input	$V_{REF/EN}$	2.75	34	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{in} = 13.5 V, $V_{REF/EN} \geq$ 2.75 V, C_{in} = 1 μF, $C_{out} \geq$ 10 μF, $C_{VREF/EN}$ = 10 nF, for typical values T_J = 25°C; for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage Tracking (Accuracy %)	V_{in} = 4.5 V to 26 V, I_{out} = 100 μA to 200 mA, $V_{REF/EN}$ = 2.75 V to (V_{in} − 1 V) (Note 9)	ΔV_{out}	−10	–	10	mV
Output Voltage Tracking (Accuracy %)	V_{in} = 12 V, I_{out} = 30 mA, $V_{REF/EN}$ = 5 V (Note 9)	ΔV_{out}	−5	–	5	mV
Line Regulation	V_{in} = 4.5 V to 26 V, I_{out} = 100 μA, $V_{REF/EN}$ = 3.3 V (Note 9)	Reg_{line}	–	–	10	mV
Load Regulation	I_{out} = 100 μA to 200 mA, $V_{REF/EN}$ = 5 V (Note 9)	Reg_{load}	–	–	10	mV
Dropout Voltage (Note 10)	$V_{REF/EN}$ = 5 V I_{out} = 100 μA I_{out} = 30 mA I_{out} = 200 mA	V_{DO}	 – – –	 4 – 240	 50 350 500	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{in} = 12 V, $V_{REF/EN}$ = 0 V	I_{DIS}	–	20	30	μA
Quiescent Current, $I_q = I_{in} - I_{out}$	V_{in} = 12 V, I_{out} = 100 μA V_{in} = 12 V, I_{out} = 200 mA	I_q	– –	110 4	150 15	μA mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 90% of $V_{REF/EN}$, $V_{REF/EN}$ = 5 V (Note 9)	I_{LIM}	250	–	600	mA
REVERSE CURRENT PROTECTION						
Reverse Current	V_{in} = 0 V, $V_{REF/EN}$ = 0 V, V_{out} = 5 V (Note 9)	I_{out_rev}	–	0.1	1.5	mA
	V_{in} = 2.5 V, $V_{REF/EN}$ = 5 V, V_{out} = 16 V (Notes 5, 9)		–	0.09	TBD	
	V_{in} = 6 V, $V_{REF/EN}$ = 5 V, V_{out} = 16 V, T_J = 150°C (Notes 5, 9)	I_{in_rev}	TBD	−0.03	–	
PSRR						
Power Supply Ripple Rejection	f = 100 Hz, 1 V_{pp}	PSRR	–	85	–	dB
ADJUST						
Adjust Input Current	$V_{REF/EN}$ = 5 V, V_{ADJ} = 5 V	I_{ADJ}	–	0.03	0.5	μA
REFERENCE / ENABLE						
Reference / Enable Input Threshold Voltage Low (Off−State) High (On−State)	 V_{out} = 0 V $\lvert V_{REF/EN} - V_{out} \rvert$ < 10 mV	$V_{th(REF/EN)}$	 0.8 –	 1.46 1.52	 – 2.75	V
Reference / Enable Input Current	$V_{REF/EN}$ = 5 V (Note 9)	$I_{REF/EN}$	–	0.02	0.5	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 11)		T_{SD}	150	180	210	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Adjust and Output pin connected to each other.
10. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V.
11. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

$V_{REF/EN}$ = 5 V, V_{ADJ} = V_{out} (unless otherwise noted)

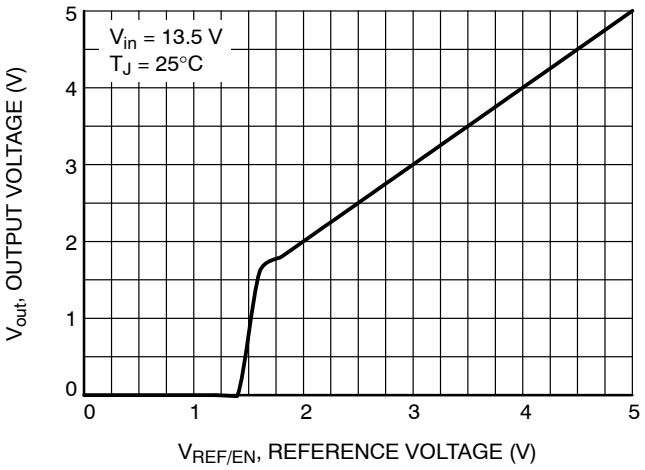


Figure 4. Output Voltage vs. Reference Voltage

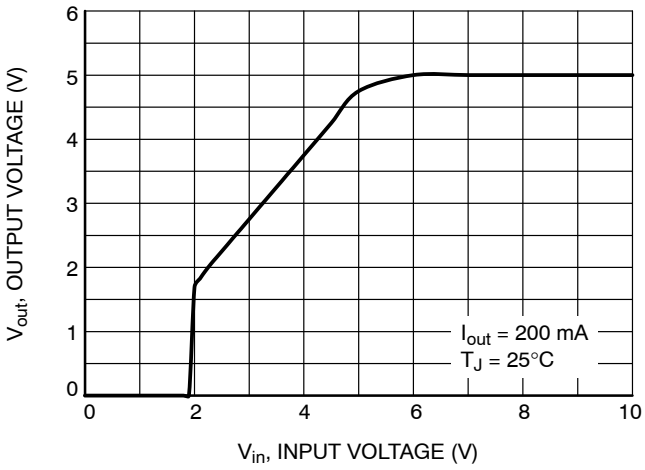


Figure 5. Output Voltage vs. Input Voltage

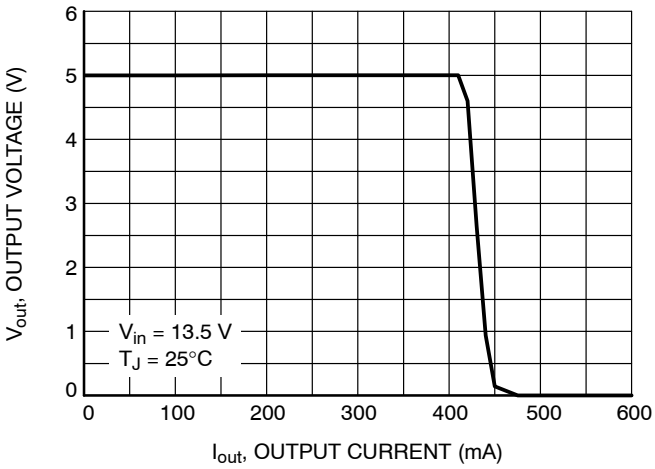


Figure 6. Output Voltage vs. Output Current

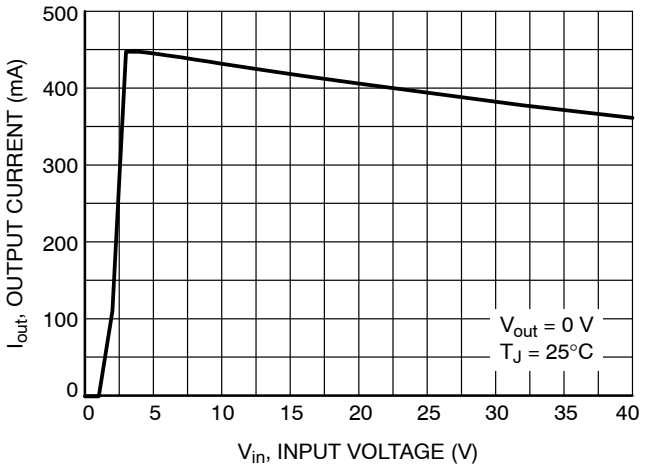


Figure 7. Maximum Output Current vs. Input Voltage

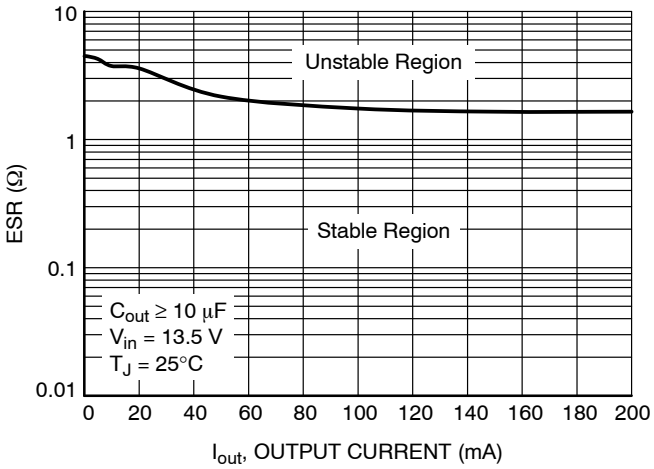


Figure 8. Output Stability vs. Output Capacitor ESR

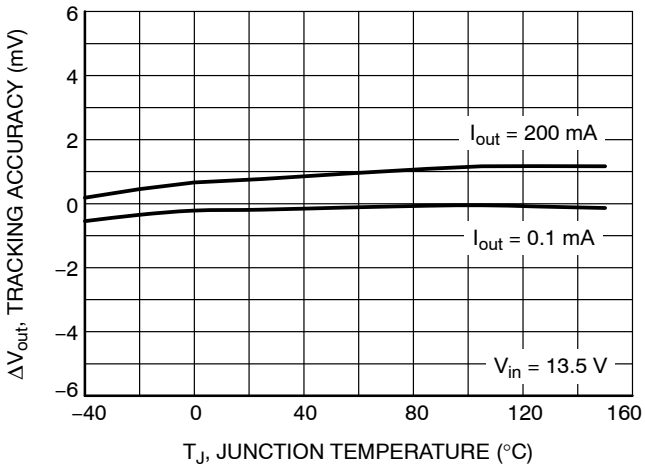


Figure 9. Tracking Accuracy vs. Junction Temperature

TYPICAL CHARACTERISTICS

$V_{REF/EN}$ = 5 V, V_{ADJ} = V_{out} (unless otherwise noted)

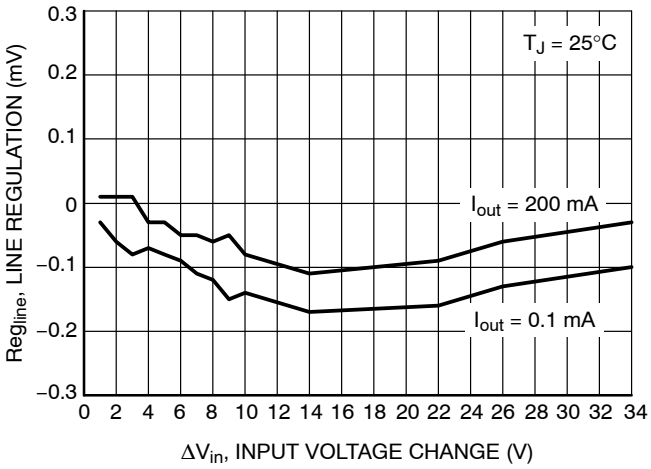


Figure 10. Line Regulation vs. Input Voltage Change

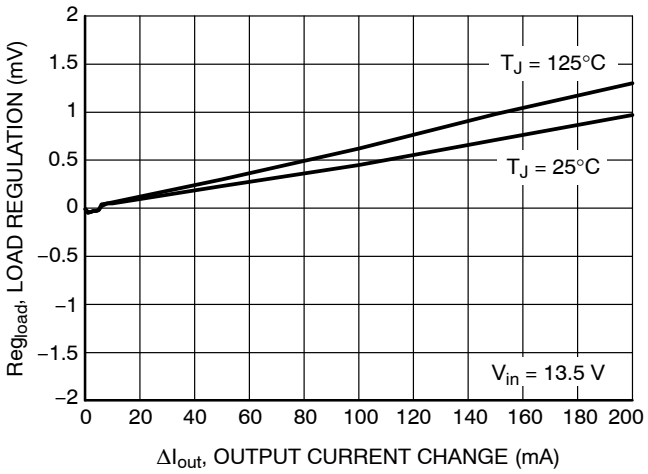


Figure 11. Load Regulation vs. Output Current Change

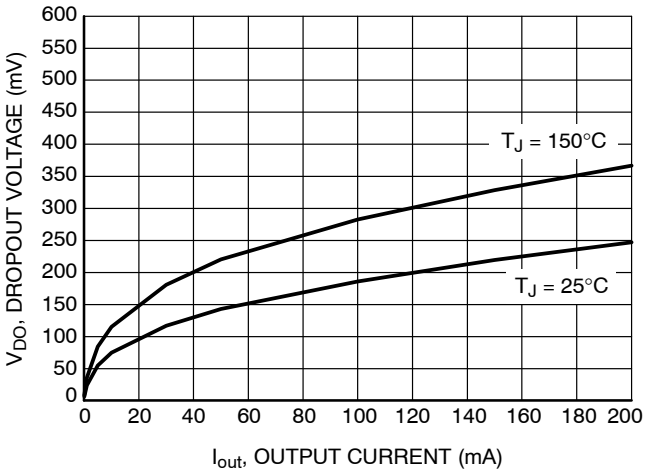


Figure 12. Dropout Voltage vs. Output Current

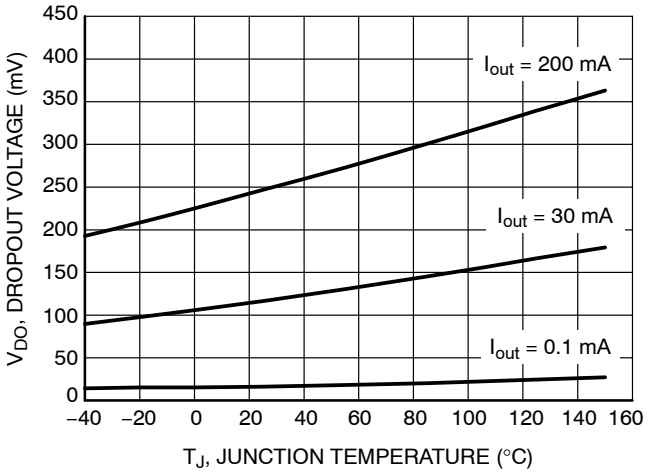


Figure 13. Dropout Voltage vs. Junction Temperature

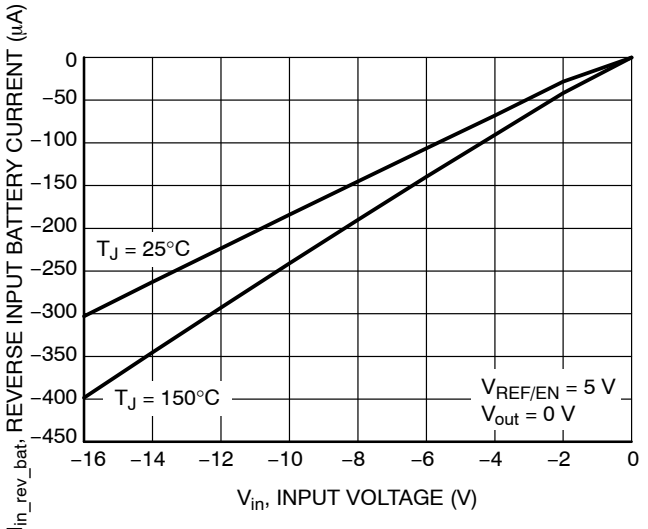


Figure 14. Reverse Current vs. Input Voltage

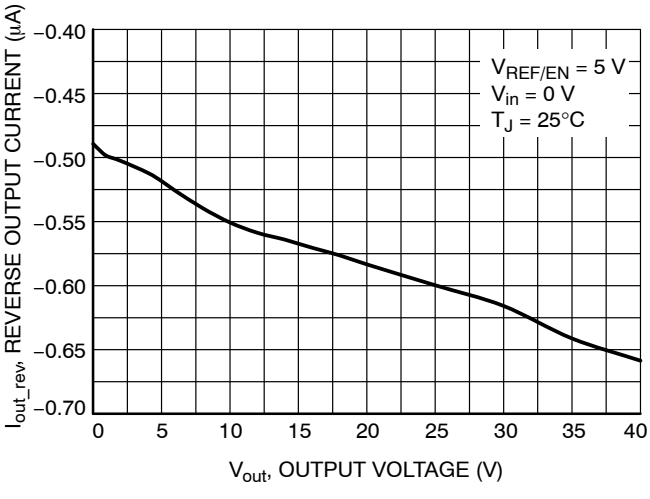


Figure 15. Reverse Output Current vs Output Voltage

TYPICAL CHARACTERISTICS

$V_{REF/EN}$ = 5 V, V_{ADJ} = V_{out} (unless otherwise noted)

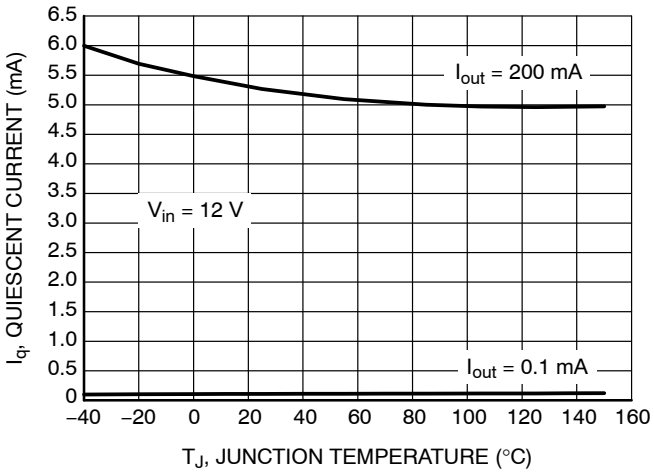


Figure 16. Quiescent Current vs. Junction Temperature

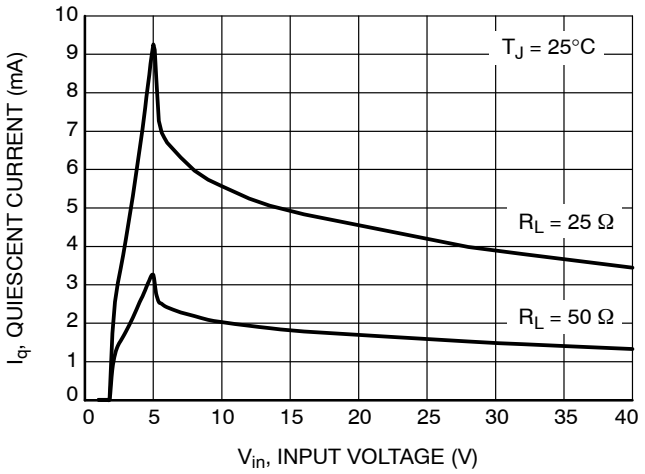


Figure 17. Quiescent Current vs. Input Voltage

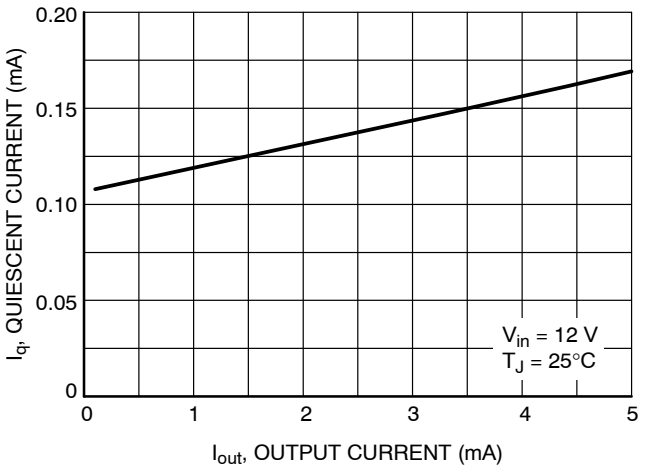


Figure 18. Quiescent Current vs. Output Current (Low Load)

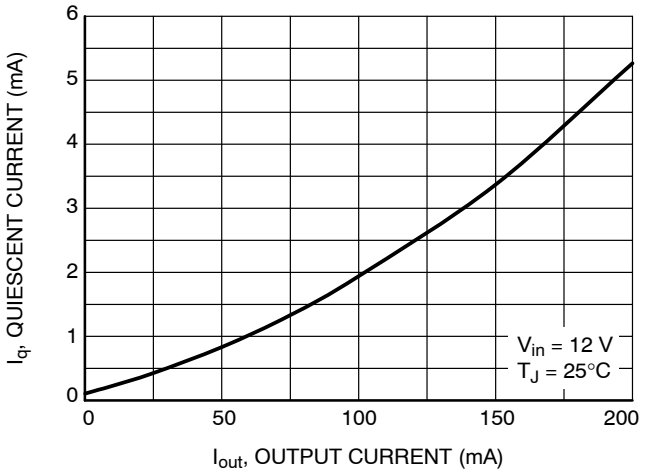


Figure 19. Quiescent Current vs. Output Current (High Load)

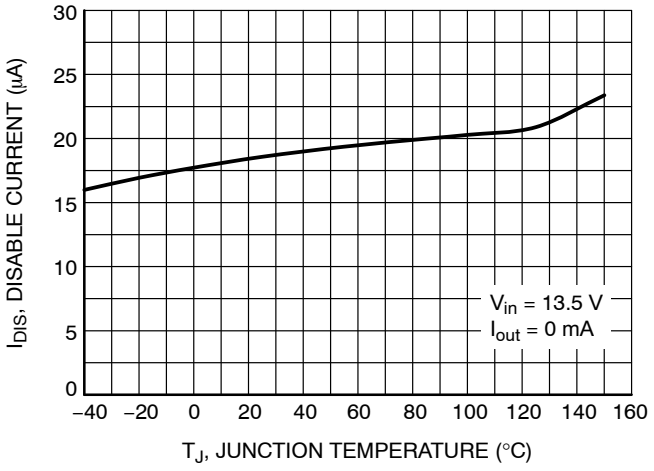


Figure 20. Disable Current vs. Junction Temperature

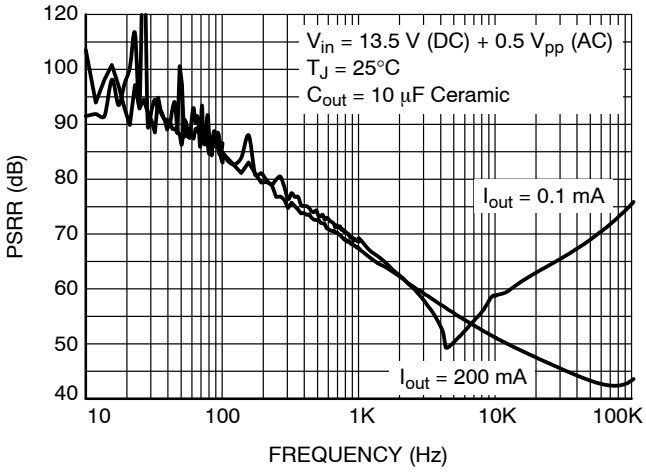


Figure 21. Power Supply Ripple Rejection

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage Tracking (Accuracy)

The output voltage tracking (accuracy) parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Current

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Reference/Enable pin is set to LOW (Off – State) the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 90% of $V_{REF/EN}$ nominal value. It means that the device is capable to supply minimum 250 mA.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 180°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8182C low dropout tracking regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 4 to Figure 21.

Input Decoupling (C_{in})

A ceramic or tantalum 1 μF capacitor is recommended and should be connected close to the NCV8182C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{out})

The NCV8182C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs. Output Current is shown in Figure 8. The minimum output decoupling value is 10 μF and can be augmented to fulfill stringent load transient requirements. The tracking regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load transient response.

Tracking Regulator Operation

The output voltage V_{out} is controlled by comparing it to the voltage applied at pin $V_{REF/EN}$ and driving a PNP pass device accordingly. The loop stability depends on the output capacitor C_{out}, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of over temperature. The over temperature protection circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short−circuited) by reducing the output current. A thermal balance below 200°C junction temperature is established. Please note that a junction temperature above 150°C is outside the maximum ratings and reduces the IC lifetime. The NCV8182C allows a negative supply voltage. However, several small currents are flowing into the IC. For details see electrical characteristics table and typical performance curves. The thermal protection circuit is not operating during reverse polarity condition.

By pulling the $V_{REF/EN}$ lead below 1.46 V typically, the IC is disabled and enters a sleep mode where the device draws less than 30 μA from power supply. When the $V_{REF/EN}$ lead is typically greater than 1.52 V, V_{out} tracks the $V_{REF/EN}$ lead normally. The output is capable of supplying 250 mA to the load while configured as a similar (Figure 22), lower (Figure 23), or higher (Figure 24) voltage as the reference lead. The ADJ lead acts as the inverting terminal of the op amp and the $V_{REF/EN}$ lead as the non−inverting. The device can also be configured as a high−side driver as displayed in Figure 25.

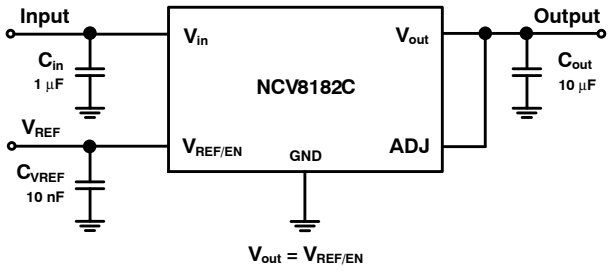


Figure 22. Tracking Regulator at the Same Voltage

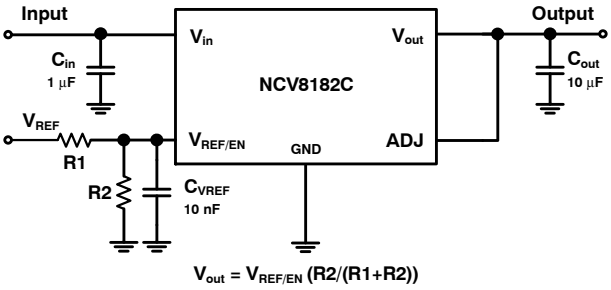


Figure 23. Tracking Regulator at Lower Voltages

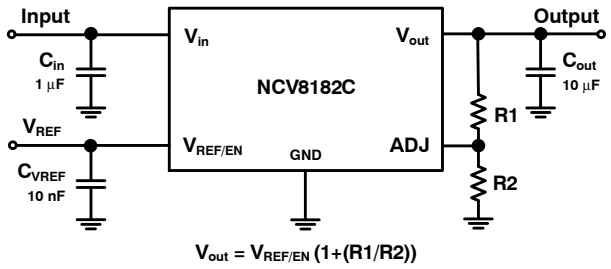


Figure 24. Tracking Regulator at Higher Voltage

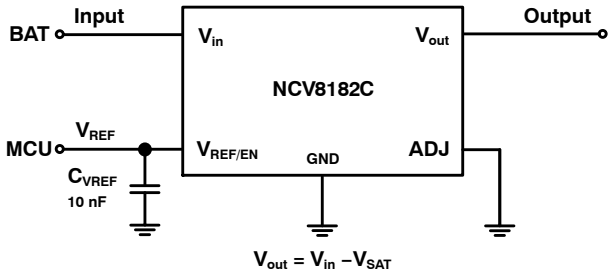


Figure 25. High−Side Driver

Thermal Considerations

As power in the NCV8182C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8182C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8182C can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8182C soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2 W for DPAK and 1.1 W for SOIC−8 when the ambient temperature (T_A) is 25°C. See Figures 26 and 27 for R_{thJA} versus PCB area. The power dissipated by the NCV8182C can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8182C and make traces as short as possible. For better EMC performance on $V_{REF/EN}$ lead it is recommended to use additional decoupling 10 nF ceramic capacitor connected between $V_{REF/EN}$ and GND. The NCV8182C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application example diagram shown in Figure 26 can be used.

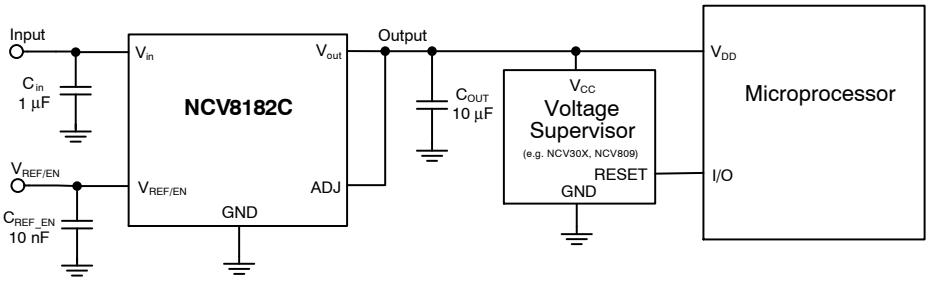


Figure 26. NCV8182C Application Diagram

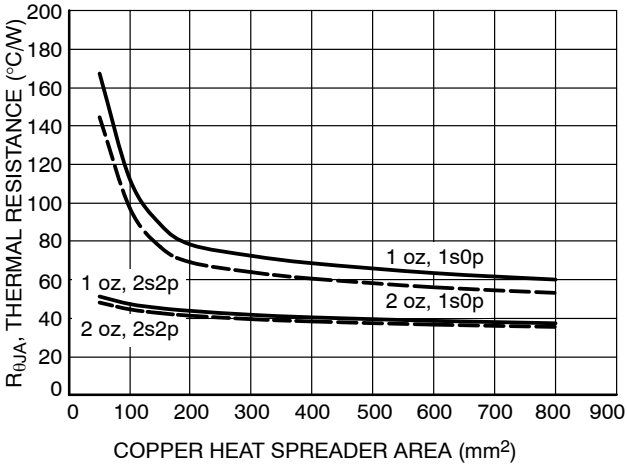


Figure 27. Thermal Resistance vs. PCB Copper Area (DPAK−5)

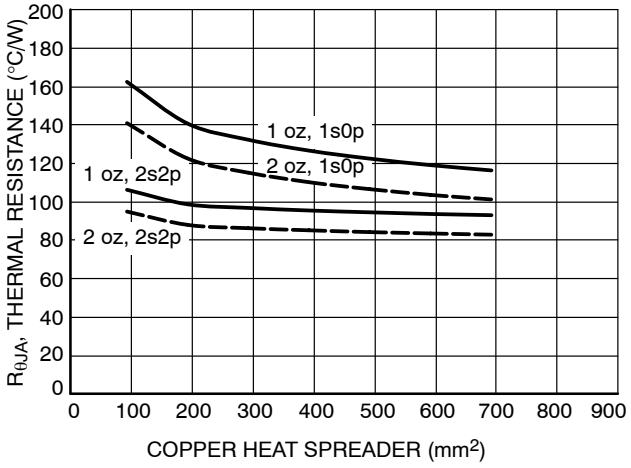


Figure 28. Thermal Resistance vs. PCB Copper Area (SOIC−8)

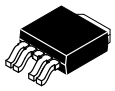
ORDERING INFORMATION

Device	Package	Shipping†
NCV8182CDR2G (In Development)	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV8182CDTRKG	DPAK, 5−PIN (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

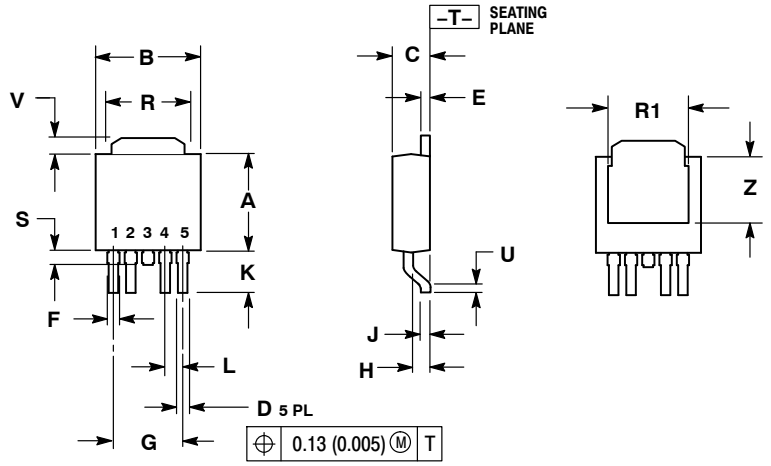
ON Semiconductor®



DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014

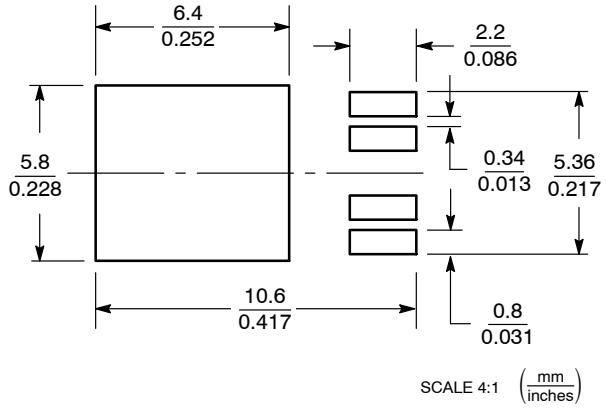
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

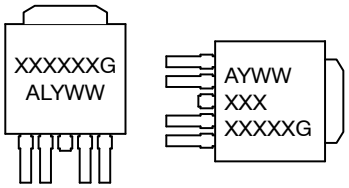
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

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