Self-Protected Very Low I_Q High Side Driver with Analog Current Sense

NCV84003F

The NCV84003F is a fully protected single channel high side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids, and other actuators. The device incorporates advanced protection features such as active inrush current management, over-temperature shutdown with latch-off. A dedicated Current Sense pin provides precision analog current monitoring of the output as well as fault indication in case of output short circuit to Supply, overload, over-temperature, OUT short circuit to GND, and OFF state open load detection. A Diagnostic Enable pin allows all diagnostic and current sense features to be enabled or disabled during device operation.

Features

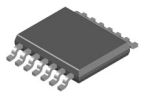
- 5 V/3.3 V Compatible Control Input
- Low Standby Current
- Absolute and Differential Thermal Shutdown
- Proportional Analog Current Sense Output Multiplexed with Discrete Output Levels for Fault Differentiation
- Overload and Short to Ground Protection with Active Inrush Management
- Intelligent Retry with Latch Off in Protect Mode
- OFF State Open Load (OSOL) and Short Circuit to V_{BATT} Detection
- Under-voltage Shutdown and Over-voltage Protection
- Protection against Loss of Ground and Loss of V_{BATT}
- Inverse Current Protection with FET Turn On in Inverse Mode
- ESD Protection
- Reverse Battery Protection with External Components
- AEC-Q100 Qualified and PPAP Capable

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays, Discrete Circuits and Fuses
- Automotive / Industrial

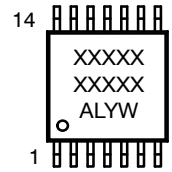
FEATURE SUMMARY

Nominal Operating Voltage Range	V_D	6 to 18	V
R_{ON} T_J = 25 °C	R_{ON}	3.6	mΩ
Output Output Current Limit (Typ)	I_{lim}	85	A
Quiescent Current	I_{Q_85}	1.5	μA



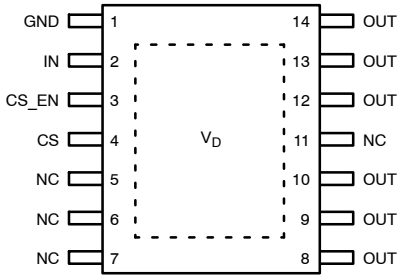
TSSOP14 EP
CASE 948BZ

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot Number
Y = Year
W = Work Week

PACKAGE PIN DESCRIPTION



(Top View)

SAFETY DESIGN – ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

ORDERING INFORMATION

Device	Package	Shipping†
NCV84003FPAR2G	TSSOP14 EP (Pb-Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. PIN DESCRIPTION

Pin #	Symbol	Description
1	GND	Ground Reference
2	IN	Logic Level Input for Output Activation
3	CS_EN	Logic Level Input for Diagnosis Enable
4	CS	Current Sense/Diagnostic Output
5–7	NC	No Connect
11	NC	No Connect
08–10, 12–14	OUT	Output
E–pad	VD	Battery Connection

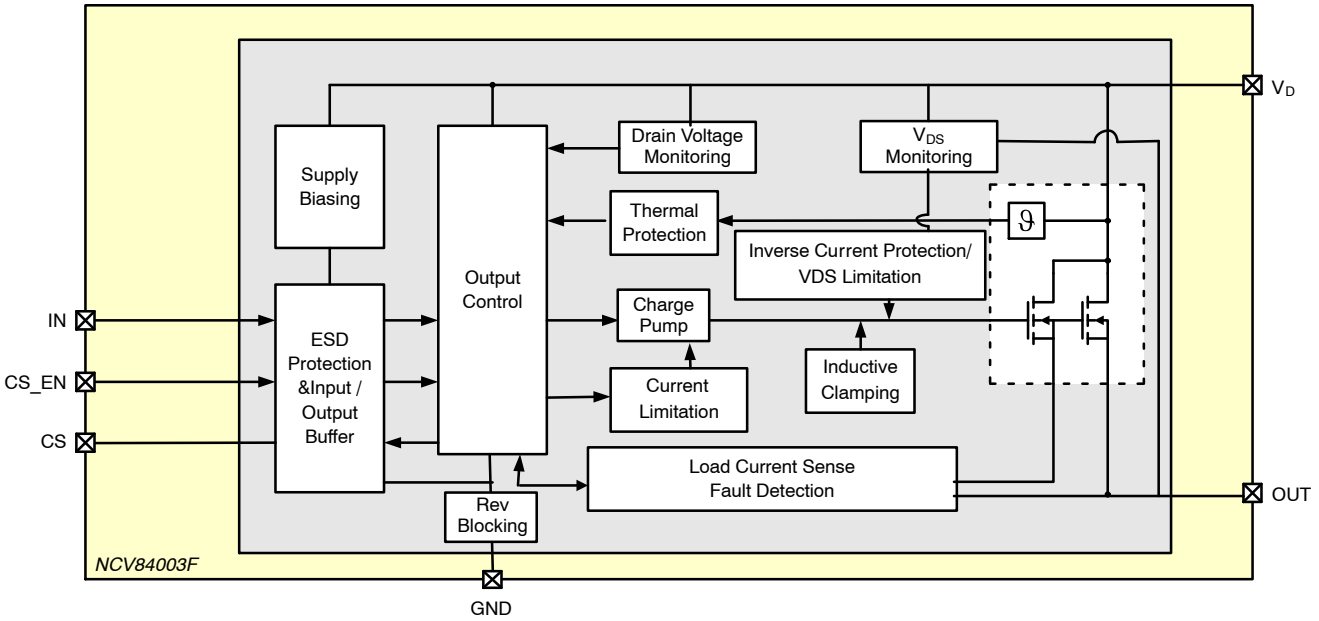


Figure 1. Block Diagram

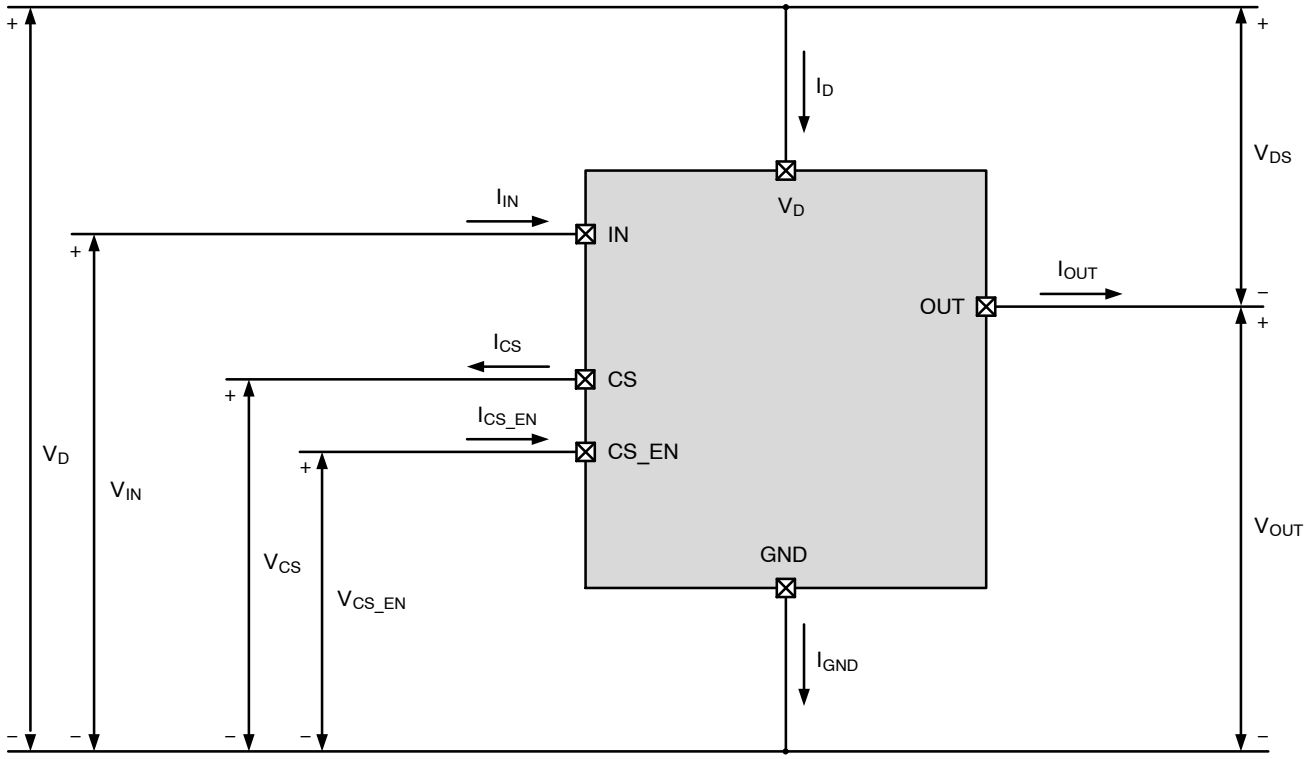


Figure 2. Voltage and Current Definitions

Electrical Specifications

Table 2. MAXIMUM RATINGS (Note 1) (−40 °C ≤ T_J ≤ 150 °C unless otherwise specified)

Rating	Symbol	Min	Max	Unit
GENERAL				
Supply Voltage (Note 2)	V_D	−0.3	28	V
Supply Voltage for Load Dump Protection	V_{D_LD}		35	V
Supply Voltage for Short Circuit Protection	V_{D_SC}	0	24	V
Reverse Polarity Voltage, t < 2 min, Load: 2 Ω, Setup: Refer to Figure 15	V_{D_REV}	0	16	V
INPUT PINS: IN, CS_EN				
Current at Input Pins	$I_{DIG_IN_MAX}$	−1	2	mA
Current at Input Pins in Rev Battery, t < 2 min	$I_{DIG_IN_MAX_REV}$	−1	10	mA
Voltage at Input Pins	$V_{DIG_IN_MAX}$	−0.3	6.5	V
CURRENT SENSE OUTPUT				
Voltage at Current Sense Output	V_{CS_MAX}	−0.3	V_D	V
Current at Current Sense Output	I_{CS_MAX}	−25	$I_{CS_Fault_ILIM}$	mA
OUTPUTS				
Power Dissipation T_A = 85 °C, T_J = 150 °C	P_{MAX}		3	W
Drain-Source Voltage at Power Transistor	V_{DS_MAX}		V_{ZCL}	V
Single Pulse Inductive Load Switching Energy (L = 1 mH, V_D = 13.5 V, I_L = 6.4 A, T_{JSTART} = 150 °C)	E_{AS}		30	mJ
GROUND TERMINAL				
Current through GND Pin	I_{GND}	−50	50	mA
TEMPERATURES				
Operating Junction Temperature	T_J	−40	150	°C
Storage Temperature	$T_{J_storage}$	−55	150	°C
ESD				
ESD Susceptibility All Pins to Ground HBM	V_{ESD_HBM}	−2	+2	kV
ESD Susceptibility All Pins − Pin to Pin and Pin to Supply HBM	V_{ESD_HBM}	−1	1	kV
ESD Susceptibility OUTx to GND, V_D Connected, HBM	$V_{ESD_OUT_HBM}$	−4	4	kV
ESD Susceptibility All Pins CDM	V_{ESD_CDM}	−500	500	V
ESD Susceptibility Pin (Corner Pins), CDM	V_{ESD_NC}	−750	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Not subject to production testing.
2. For transient application only. Extended operation at absolute maximum voltage may affect device reliability.
3. HBM test setup per AEC-Q100:EIA-JESD22-A114-B.
4. CDM test setup per AEC-Q100:EIA-JESD22-C101-A.
5. Board construction based on JEDEC JESD 51-7 for a four layer 2s2p board with natural convection. Vias were added under the exposed pad as shown in Figure 3.

Table 3. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max Value	Unit
Thermal Resistance			
Junction-to-Top (Note 7)	P_{si_JT}	1.9	°C/W
Junction-to-EPAD (Note 7)	$P_{si_Je\text{-}PAD}$	1.3	°C/W
Junction-to-Ambient – 1s0p min pad (Note 6)	R_{thJA}	145	°C/W
Junction-to-Ambient – 1s0p +1 in^2 Cu (Note 6)	R_{thJA}	51	°C/W
Junction-to-Ambient – 2s2p min pad (Note 7)	R_{thJA}	35	°C/W
Junction-to-Ambient – 2s2p +1 in^2 Cu (Note 7)	R_{thJA}	22	°C/W

6. Board construction based on JEDEC JESD 51-3 for a single layer 1s0p board with natural convection.
7. Board construction based on JEDEC JESD 51-7 for a four layer 2s2p board with natural convection. Vias were added under the exposed pad as shown below.

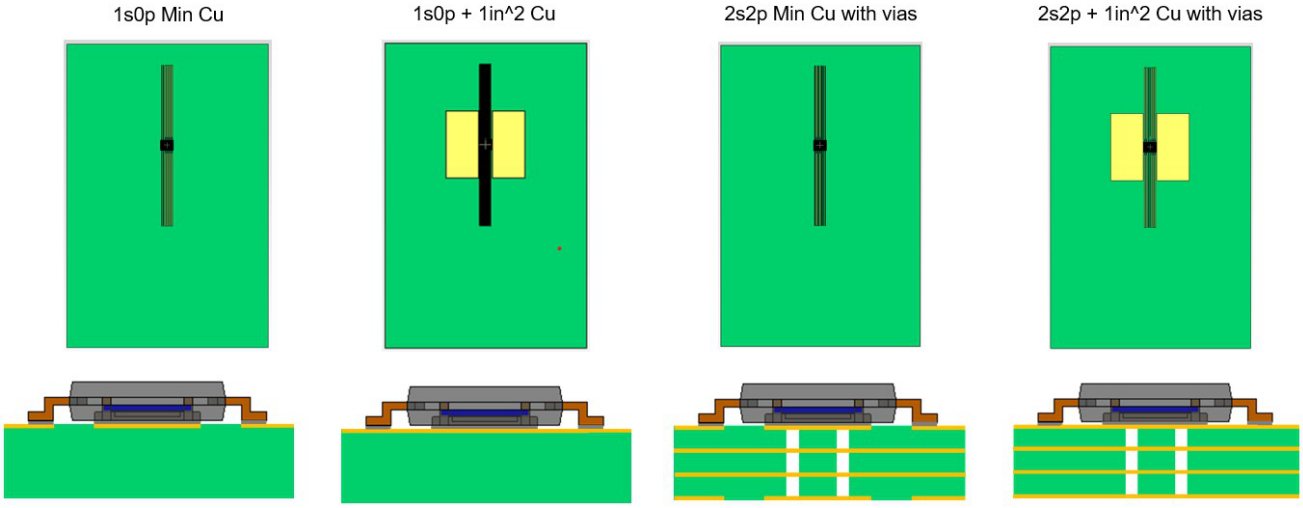


Figure 3. Board Construction for Thermal Performance

Table 4. SUPPLY ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)(Typical Values measured @ V_D = 13.5 V, T_J = 25 °C)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Nominal Supply Voltage Range (Note 8)	V_{D_NOM}		6	13.5	18	V
Extended Supply Voltage Range (Notes 8, 9)	V_{DS_EX}	V_{IN} = 5 V, R_L = 4 Ω, 3.1 V ≤ V_D ≤ 28 V Ramp down V_D from 28 V to 3.1 V			0.5	V
Under Voltage Shutdown	V_{D_UV}	V_{IN} = 5 V, V_D Falling, From V_{DS} < 0.5 V to I_{OUT} = 0	2.4	2.9	3.1	V
Minimum Operating Voltage	V_{D_MIN}	V_{IN} = 5 V, V_D Rising, From I_{OUT} = 0 to V_{DS} < 0.5 V	2.9	3.4	4.1	V
Under Voltage Shutdown Hysteresis	$V_{D_UV_HYS}$			0.5		V
Supply Undervoltage Recovery Time (Note 8)	$t_{UV_Recover}$	V_{IN} = 5 V, V_D Rising, From V_D = 0 V → $V_D \ge V_{D_MIN}$ to V_{DS} < 0.5 V (See Figure 13)	2.5	5	7.5	ms
Quiescent Current	I_{Q_85}	V_D = 18 V, $T_J \le 85$ °C, $V_{IN} = V_{CS_EN}$ = 0 V			1.5	μA
Quiescent Current	I_{Q_150}	V_D = 18 V, T_J = 150 °C, $V_{IN} = V_{CS_EN}$ = 0 V		5	26	μA
Quiescent Current, Diagnostic Active	I_{Q_DIAG}	V_D = 18 V, V_{IN} = 0 V, V_{CS_EN} = 5 V		1.8	3	mA
Normal Operating Current	I_{GND_ON}	V_D = 18 V, $V_{IN} = V_{CS_EN}$ = 5 V, V_{CS} < 5 V		5	6	mA

8. Not subject to production testing.
9. Extended operation outside the nominal supply voltage range may affect device reliability. Parametric performance not guaranteed.

Table 5. POWER OUTPUT ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (Typical Values measured @ V_D = 13.5 V, T_J = 25 °C)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
On-state Resistance	R_{ON_25}	$I_{OUT} = I_{NOM}$ = 15 A, V_{IN} = 5 V, T_J = 25 °C		3.6		mΩ
On-state Resistance	R_{ON_150}	$I_{OUT} = I_{NOM}$ = 15 A, V_{IN} = 5 V, T_J = 150 °C			7.2	mΩ
On-state Resistance – Low Voltage	R_{ON_LV}	I_{OUT} = 2 A, V_D = 3.4 V, T_J = 150 °C			8.6	mΩ
On-state Resistance – Inverse Current	$R_{ON_INV_25}$	I_{OUT} = −4 A, V_D = 13.5 V, T_J = 25 °C		3.6	–	mΩ
On-state Resistance – Inverse Current	$R_{ON_INV_150}$	I_{OUT} = −4 A, V_D = 13.5 V, T_J = 150 °C			7.2	mΩ
Output Leakage Current	I_{LEAK_85}	$V_{IN} = V_{CS_EN}$ = 0 V, V_{OUT} = 0 V, T_J < 85 °C			1	μA
Output Leakage Current	I_{LEAK_150}	$V_{IN} = V_{CS_EN}$ = 0 V, V_{OUT} = 0 V, T_J < 150 °C			25	μA
Drain-to-Source Clamping Voltage ($V_D - V_{OUT}$)	V_{ZCL}	I_{OUT} = 10 mA, V_{IN} = 5 V → 0 V	35	36	40	V
Body Diode Forward Voltage	V_F	I_{OUT} = −1 A, T_J = 150 °C, $V_F = V_{out} - V_D$			0.7	V

Input Pins

All low-voltage control inputs are compatible with 3.3 V and 5 V microcontroller supply voltages. All inputs comprise of a voltage Schmidt-trigger circuit to enable direct drive from voltage sources and prevent uncontrolled oscillations due to slow transitions at the inputs. Each input features a pull-down element to prevent uncontrolled input states in case of an open pin condition. Unused inputs should be left open or connected to device GND through a 4.7 kΩ resistor.

Table 6. DIGITAL INPUT (IN, CS_EN) CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Low Level Digital Input Voltage	$V_{DIG_IN_L}$				0.8	V
High Level Digital Input Voltage	$V_{DIG_IN_H}$		2			V
Digital Input Voltage Hysteresis	$V_{DIG_IN_HYS}$			0.25		V
Digital Input Pull-down Current	I_{IN_PD}	0.8 V ≤ V_{IN} ≤ 2 V			25	μA

Table 7. SWITCHING CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (Refer to Figure 7)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Turn ON Delay (V_{CS_EN} = Hi, V_{IN} Lo → Hi to V_{OUT} = 10% V_D)	t_{D_ON}	V_D = 13.5 V, R_L = 2 Ω	5	20	70	μs
Turn ON Delay Sleep Mode ($V_{IN} = V_{CS_EN}$ Lo → Hi to V_{OUT} = 10% V_D)	$t_{D_ON_SLEEP}$		5	75	125	μs
Turn ON Time (V_{IN} Lo → Hi to V_{OUT} = 90% V_D)	t_{ON}		35	75	150	μs
Turn ON Time Sleep Mode ($V_{IN} = V_{CS_EN}$ Lo → Hi to V_{OUT} = 90% V_D)	t_{ON_SLEEP}		35	130	200	μs
Turn OFF Delay (V_{IN} Hi → Lo to V_{OUT} = 90% V_D)	t_{D_OFF}		5	25	70	μs
Turn OFF Time (V_{IN} Hi → Lo to V_{OUT} = 10% V_D)	t_{OFF}		30	60	160	μs
Turn ON / OFF Matching $t_{ON} - t_{OFF}$	Δt_{ON-OFF}		−40	20	60	μs
Slew Rate ON (V_{OUT} = 30% to 70% V_D)	SR_{ON}		0.1	0.3	0.5	V/μs
Slew Rate OFF (V_{OUT} = 70% to 30% V_D)	SR_{OFF}		−0.5	−0.3	−0.1	V/μs
Slew Rate Matching $SR_{ON} - SR_{OFF}$	ΔnSR		−0.15	0	0.15	V/μs
Turn ON Energy (Note 10)	W_{ON}	V_D = 18 V, R_L = 4 Ω, VOUT: 10% V_D ↔ 90% V_D		1.5		mJ
Turn OFF Energy (Note 10)	W_{OFF}			1.5		mJ

10. Not Subject to Production Testing.

Protection

Table 8. PROTECTION CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Current Limitation	I_{LIM}	V_D = 13.5 V, Setup based on AECQ100-012 Load Short Circuit	75	85	95	A
Current Limitation at High V_{DS} (Note 11)	$I_{LIM(FB)}$	$V_{DS} \ge 17$ V		0.6 x I_{LIM}		A
Current Limitation at High V_D for Jump Start (Note 11)	$I_{LIM(JS)}$	$V_D > V_{D_JS}$		0.6 x I_{LIM}		A
Differential Thermal Shutdown Threshold (Note 11)	T_{DTSD}			80		°C
Thermal Shutdown Temperature Threshold (Note 11)	T_{TSD}		150	175	200	°C
Thermal Shutdown Temperature Hysteresis (Note 11)	T_{TSD_HYS}			15		°C
Over-Voltage Protection Clamp	V_{ZOV}	Current into the V_D pin, I_{OUT} = 5 mA, V_{IN} = 0 V	35	36	40	V
Drain Voltage for Current Limitation Reduction in Jump Start (Note 11)	V_{D_JS}		18.5	20.5	22.5	V

11. Not Subject to Production Testing.

Table 9. RETRY STRATEGY ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (Refer to Figure 18)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Number of Retries in Fault after Counter Reset (Note 12)	n_{COUNT}	$I_{OUT} = I_{LIM}$, or $T_{J(ABS)} > T_{TSD}$, or $T_{J(DYN)} > T_{DTSD}$		1		
EN Based Counter Reset Time (Note 12)	$t_{IN(Rst)}$		40	70	100	ms
CS_EN Based Counter Reset Time (Note 12)	$t_{CS_EN(Rst)}$	V_{IN} = 0 V, Fault Counter > 0	150			µs

12. Not Subject to Production Testing.

Diagnostic Functions

NCV84003F provides diagnostic information and dynamic current sensing on the diagnostic output pin CS.

Table 10. DIAGNOSTIC TRUTH TABLE

Operation Mode	IN	CS_EN	Output Voltage	CS Output
Normal Operation	L	H	~GND	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Short Circuit to GND			GND	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Over Temperature			~GND	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Short Circuit to V_{BATT}			V_{BATT}	I_{CS_OSOL}, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Open Load			$< V_D - V_{DS_OSOL}$	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
			$> V_D - V_{DS_OSOL}$	I_{CS_OSOL}, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Inverse Current			$> V_D$	I_{CS_OSOL}, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Normal Operation	H		$\sim V_D$	$I_{CS} = I_{OUT} / K_{NOM}$
Short Circuit to GND − Over Current Detection			~GND	$I_{CS_FAULT_ILIM}$
Over Temperature (Absolute or Differential)			~GND	$I_{CS_FAULT_TSD}$
Short Circuit to V_{BATT}			V_{BATT}	$I_{CS} < I_{OUT} / K_{NOM}$
Open Load			$\sim V_D$	$I_{CS} \le I_{CS(OL)}$
Underload			$\sim V_D$	$I_{CS_OL} < I_{CS} < I_{OUT} / K$
Inverse Current			$> V_D$	$I_{CS} \le I_{CS(OL)}$
Diagnostics Disabled	X	L	X	HiZ

Current Sense Ratio

The accuracy of IOUT to ICS ratio (K), can be improved by a calibration procedure in end of line testing. The procedure can be performed at nominal current at a single designated temperature.

Diagnostics

Table 11. CURRENT SENSE CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CS Leakage Current, CS Output Disabled	$I_{Q_CS_DIS}$	V_{IN} = 5 V, V_{CS_EN} = 0 V, I_L = 15 A			0.5	μA
CS Leakage Current, CS Output Enabled	$I_{Q_CS_EN}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I_L = 0 A			1	μA
CS Operation Voltage for Nominal Operation – ($V_D - V_{CS}$) (Note 13)	$V_{CS_SAT(NOM)}$	V_D = 6 V, $V_{IN} = V_{CS_EN}$ = 5 V, I_L = 15 A, $I_{CS} > 0.5 \times I_{CS_NOM}$		0.5	1	V
CS Operation Voltage for In-fault Operation – ($V_D - V_{CS}$) (Note 13)	$V_{CS_SAT(Fault)_ILIM}$	V_D = 6 V, $V_{IN} = V_{CS_EN}$ = 5 V, $I_{CS} > 0.5 \times I_{CS_Fault_ILIM}$	0	0.5	1	V
CS Operation Voltage for In-fault Operation – ($V_D - V_{CS}$) (Note 13)	$V_{CS_SAT(Fault)_TSD}$	V_D = 6 V, $V_{IN} = V_{CS_EN}$ = 5 V, $I_{CS} > 0.5 \times I_{CS_Fault_TSD}$	0	0.5	1	V
CS Operation Voltage for OFF State Open Load Operation – ($V_D - V_{CS}$) (Note 13)	$V_{CS_SAT(OSOL)}$	V_D = 6 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, I_L = 0 A, $I_{CS} > 0.5 \times I_{CS_Fault_OSOL}$	0	0.5	1	V
CS Saturation Current (Note 14)	I_{CS_SAT}		8	10		mA
CS Fault Indication Current: ILIM (Note 13)	$I_{CS_FAULT_ILIM}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, Fault Counter > 0, $I_{OUT} = I_{LIM}$	6.7	8.5	10	mA
CS Fault Indication Current: TSD/DTSD (Note 13)	$I_{CS_FAULT_TSD}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, Fault Counter > 0, $T_J > T_{TSD}$ or $T_{J(DYN)} > T_{DTSD}$	3.8	5	6.5	mA
CS Fault Indication Current in OFF State Open Load	$I_{CS_FAULT_OSOL}$	V_{IN} = 0 V, V_{CS_EN} = 5 V, Fault Counter = 0, $V_{DS} < V_{OL_OFF}$	1.9	2.5	3.5	mA
CS Pin Clamp to Power Supply	V_{CS_CL}	I_{CS} = 5 mA	35	36	40	V
Current Sense Ratio 1	K_1	I_{OUT} = 0.5 A	17025	22700	28375	
Current Sense Ratio 2	K_2	I_{OUT} = 0.75 A	19295	22700	26105	
Current Sense Ratio 3	K_3	I_{OUT} = 2 A	20430	22700	24970	
Current Sense Ratio 4	K_4	I_{OUT} = 8.5 A	21565	22700	23835	
Current Sense Ratio 5	K_5	I_{OUT} = 15 A	21792	22700	23608	
Max Current Sense Ratio Drift after Two-Point Calibration (Note 15)	K_{rel4}	K_3 / K_4, including temperature drift	0.97	1	1.03	

13. Not Subject to production testing.
14. Guaranteed by Design.
15. Not subjected to production testing. For more information, refer to the AND9733/D Applications Note.

Table 12. CURRENT SENSE TIMING ($6 \le V_D \le 18$ V; $-40\ °C \le T_J \le 150\ °C$ unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Current Sense Settling Time after Diagnostic Activation, Stable Output and Load Conditions – Nominal Load	$t_{S_CS_ENH}$	V_{IN} = 5 V, V_{CS_EN} = 0 V → 5 V, V_D = 13.5 V, I_L = 15 A, I_{CS} = 90% I_{CS_STATIC}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			30	μs
Current Sense Settling Time after Diagnostic Activation, Stable Output and Load Conditions – Light Load (Note 16)	$t_{S_CS_ENL}$	V_{IN} = 5 V, V_{CS_EN} = 0 V → 5 V, V_D = 13.5 V, I_L = 0.75 A, I_{CS} = 90% I_{CS_STATIC}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			60	μs
Current Sense Settling Time after Load Current Change (Note 16)	$t_{S_CS_LOAD_U}$	V_{IN} = V_{CS_EN} = 5 V, V_D = 13.5 V, I_L = 8.5 A → 15 A, I_{CS} = 90% I_{CS_STATIC}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	μs
Current Sense Settling Time after Load Current Step Down to Light Load (Note 16)	$t_{S_CS_LOAD_D}$	V_{IN} = V_{CS_EN} = 5 V, V_D = 13.5 V, I_L = 15 A → 0.75 A, I_{CS} = 90% I_{CS_STATIC}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	μs
Current Sense Output Disable Time (Note 16)	$t_{S_CS_DIS}$	V_{IN} = 5 V, V_{CS_EN} = 5 V → 0 V, V_D = 13.5 V, I_L = 15 A, I_{CS} = 10% I_{CS_STATIC}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	μs
Current Sense Output Disable Time – In Fault (Note 16)	$t_{S_CS_DIS_F}$	V_{IN} = 0 V, V_{CS_EN} = 5 V → 0 V, V_D = V_{OUT} = 13.5 V, I_{CS} = 10% I_{CS_STATIC}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	μs

16. Not Subject to production testing.

Table 13. OPEN LOAD / UNDERLOAD DETECTION AND TIMING ($6 \le V_D \le 18$ V; $-40\ °C \le T_J \le 150\ °C$ unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Open Load Detection Threshold, OFF State	V_{DS_OSOL}	V_{IN} = 0 V, V_{CS_EN} = 5 V	1.1	1.8	2.5	V
Open Load Detection Delay OFF State	t_{OSOL_Blank}	V_{IN} = 5V → 0 V, V_{CS_EN} = 5 V, V_D = V_{OUT} = 13.5 V, T_{CS} = 90 % I_{CS_FAULT}, R_{CS} = 1.2 kΩ, C_{CS} < 100 pF	70	150	250	μs
Open Load Detection Threshold, ON State	I_{OL_ON}	V_{IN} = 5 V, V_{CS_EN} = 5 V, I_{CS} = $I_{CS(OL)}$ = 4 μA	50		275	mA

Application Diagram and Pin Description

NCV84003F is a single channel smart high-side driver with a very low resistance n-channel output transistor. The required gate overdrive voltage for the transistor is generated by a charge pump that is integrated into the device. The output driver's protection scheme is designed to support linear resistive loads as well as loads with high inrush current, e.g. lighting bulbs. The embedded control and protection functions provide full protection to the device as well as full-featured load diagnostic for open load, underload and short circuit through a current sense output that delivers a fraction of the load current in nominal operation multiplexed with a fixed current output in a fault state. An accurate slew rate control is provided to minimize conducted EMI in case of a constant PWM operation. The device features an ultra-low quiescent current in standby mode to address quiescent current requirements of modern ECU designs.

The device provides direct control input (IN) and a diagnostic enable input (CS_EN) to control the information to be provided at the current sense output.

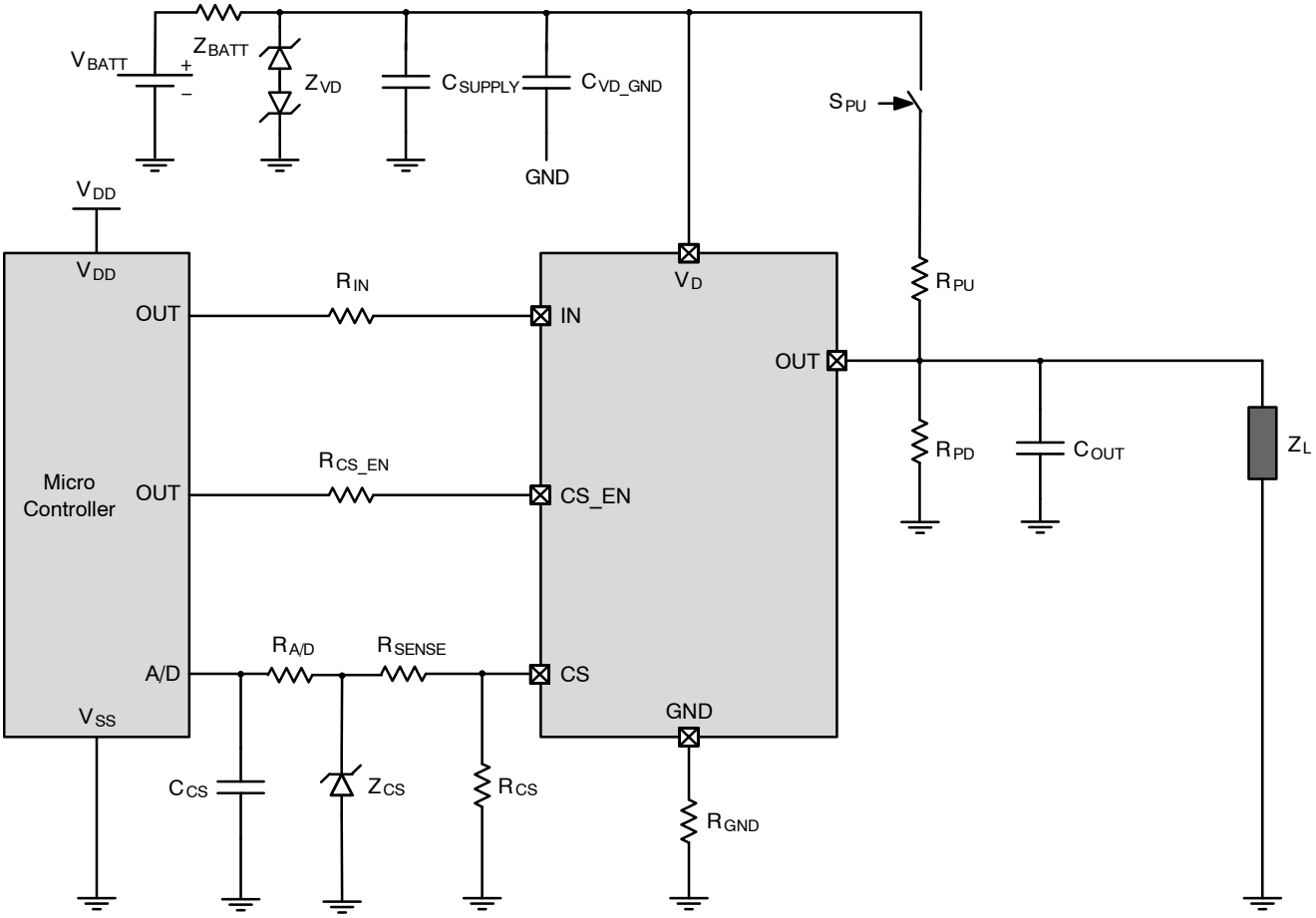


Figure 4. Application Diagram

NCV84003F is supplied by the V_D pin, which can be directly connected to the vehicle's battery net. The V_D pin is used as power supply to the control circuitry as well as the common drain supply for output channels. In order to support all board net transients following ISO7637-1, an external protection concept as shown in Figure 4 is recommended.

The zener diode Z_{VD} is used to clamp overvoltage events as well as to provide a free-wheeling path in the event of loss of battery (V_D) with charged inductive loads. R_{GND} is required to limit the maximum current flowing through Z_{VD} (refer to Figure 14) in case of an over-voltage event. Since all low-voltage I/O pins feature input protection diodes, it is required to insert series resistances into the connection lines between the controlling device (e.g. microcontroller) and NCV84003F.

Table 14. RECOMMENDED EXTERNAL COMPONENTS

Reference	Value	Function
R_{IN}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{CS_EN}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{CS}	1.2 kΩ	Current Sense resistor.
R_{SENSE}	4.7 kΩ	Provides protection against overvoltage, reverse polarity, and loss of GND. The value of this resistor should be selected with the micro controller specification.
C_{SENSE}	100 pF	Current Sense signal filtering.
$R_{A/D}$	4.7 kΩ	Current Sense signal filtering.
Z_{CS}	10 V Zener Diode	Provides protection micro controller during overvoltage at CS. Should be selected with the micro controller specification.
R_{PU}	1.5 kΩ	Polarizes the NCV84003F output during OFF state open load diagnosis.
R_{PD}	47 kΩ	Output polarization. Improves the NCV84003F immunity to electromagnetic noise and also used for short to V_{BATT} detection.
S_{PU}	BC807	Switches the battery voltage for OFF state open load diagnostic.
R_{GND}	47 Ω	Provides protection during over-voltage.
Z_{VD}	30 V Zener Diode	Provides protection of the device during overvoltage.
C_{SUPPLY}	100 nF	Filtering of voltage spikes on the battery line.
C_{VD_GND}	47 nF	Provides drain voltage stability during fast transients such as overload.
C_{OUT}	10 nF	Protection during ESD and BCI on output.

Modes of Operation

NCV84003F is designed to operate in the following distinct modes of operation as stated below. Irrespective of the modes below, it should be noted that if $V_D < V_{D(UV)}$, then the internal logic may be reset to default, and values of timers/counters cannot be guaranteed.

a. *Sleep Mode*
If IN and CS_EN have been observed as low for a duration longer than $t_{IN(Rst)}$ and, then the device enters sleep mode. The output FET is off. The internal reference blocks are shut down and digital logic is reset (as in case of supply-based reset) in this mode to offer extremely low quiescent current (Refer Table 4).

b. *Standby Mode*
If IN has been observed low for a duration more than $t_{IN(Rst)}$ and CS_EN is high then device operates in standby mode. The output FET is off. Off state diagnosis for open load and short circuit to V_{BATT} are available. If CS_EN continues to be high, device stays in standby mode.

c. *Normal Mode*
Once IN is set to High, the device transitions to normal mode. The turn on timing and slew in this mode are internally controlled and defined per Table 7. The device can be driven DC or in PWM operation while allowing for the switching delays. The CS pin outputs a current proportional to the load current if CS_EN is set to high. If diagnosis is desired, then CS response times per Table 12 need to be accounted for.

d. *Protect Mode*
While operating in normal mode, the device may observe either of the fault conditions described in Protection Features, that trigger protect mode and lead to latching-off of the output stage. A fault current output on the CS pin will be provided if CS_EN is enabled. The reset conditions for the fault counter are described in section ON State Fault Retry Strategy. If any of the reset conditions are met, device exits protect mode. ON state fault takes precedence over OSOL in off state if fault counter is greater than zero.

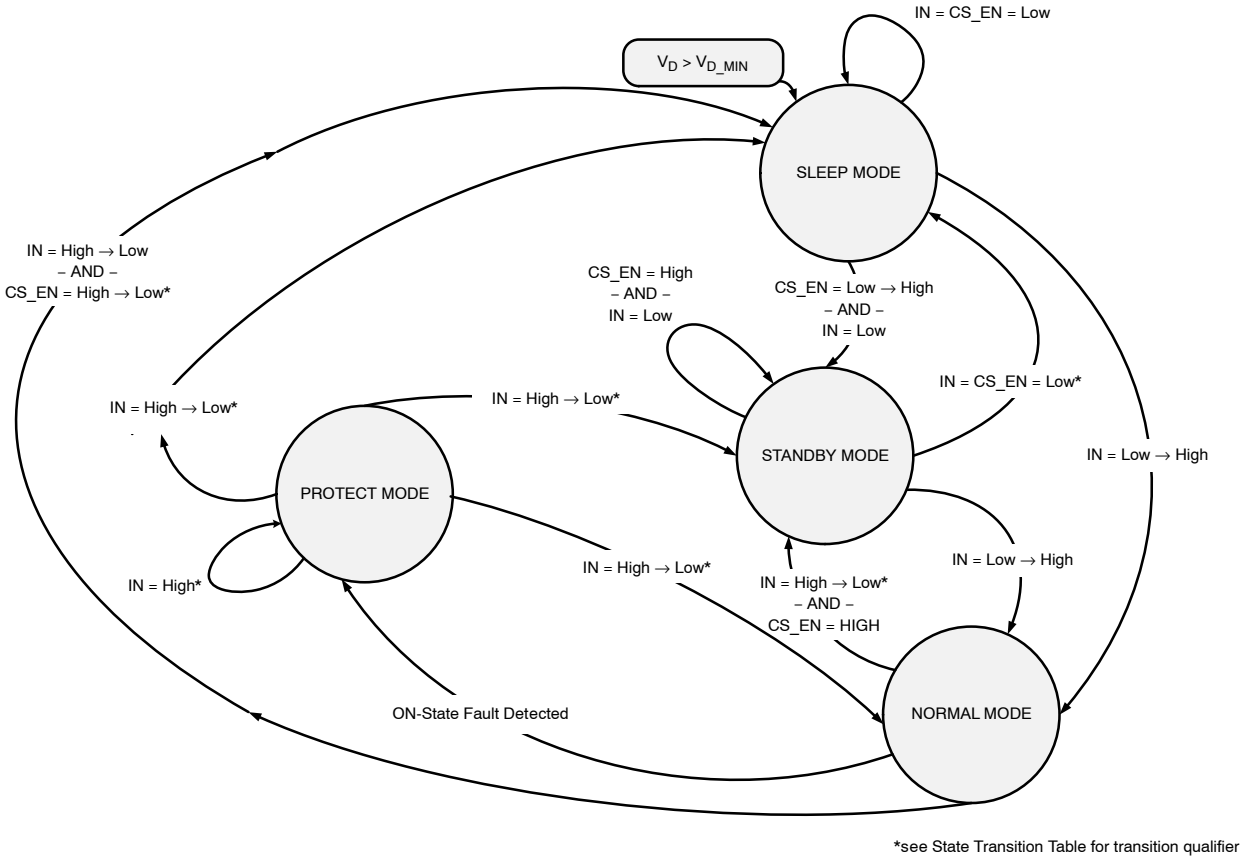


Figure 5. NCV84003F Operation Modes and Transitions

Table 15. STATE TRANSITION TABLE

Present State	Target State	Transition Criteria	Transition Qualifier
UNPOWERED	SLEEP MODE	$V_D > V_{D_MIN}$	
SLEEP MODE	STANDBY MODE	CS_EN = Low → High – AND – IN = Low	
SLEEP MODE	NORMAL MODE	IN = Low → High	
NORMAL MODE	PROTECT MODE	ON-State Fault Detected	
NORMAL MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired
NORMAL MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$
STANDBY MODE	NORMAL MODE	IN = Low → High	
STANDBY MODE	SLEEP MODE	IN = CS_EN = Low	$t_{IN(Rst)}$ Expired
PROTECT MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = High/CS_EN = Low for $t < t_{IN(Rst)}$
PROTECT MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$
PROTECT MODE	NORMAL MODE	IN = High → Low	$t_{IN(Rst)}$ Not Expired – AND – $t_{CS_EN(Rst)}$ Expired

Power Stage

NCV84003F provides output power through an integrated N-channel vertical power MOSFET. The gate overdrive is provided by an integrated charge pump.

Output ON-state Resistance

Like any MOSFET, the output's ON-state resistance R_{ON} increases with the junction temperature T_J. R_{ON} also depends on the supply voltage V_D (Figure 6).

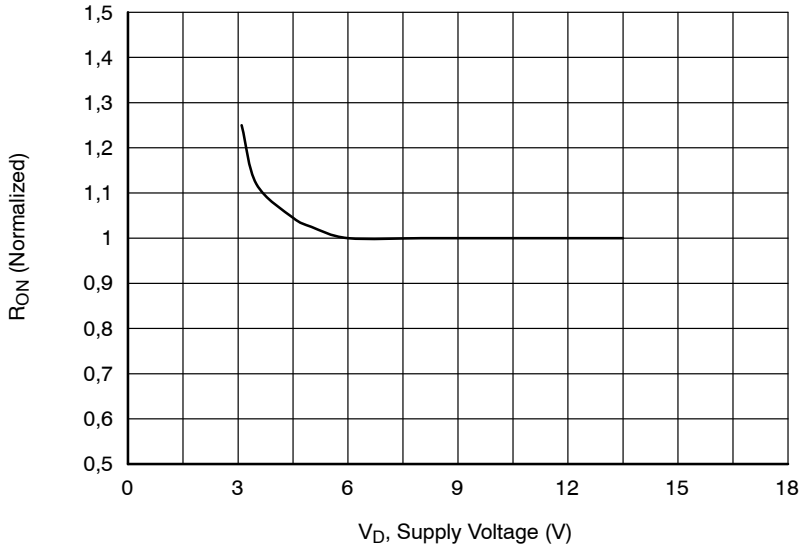


Figure 6. ON-state Resistance

Resistive Load Switching Characteristics

NCV84003F provides an integrated slew-rate control mechanism to minimize EMC in case of PWM operation. The turn on delay time and the consequent turn on time while switching on the device from sleep mode is specified longer (refer to Table 7) to allow configuration of internal circuits. A faster turn−on time from Standby Mode allows PWM of the output stage (Refer Table 7).

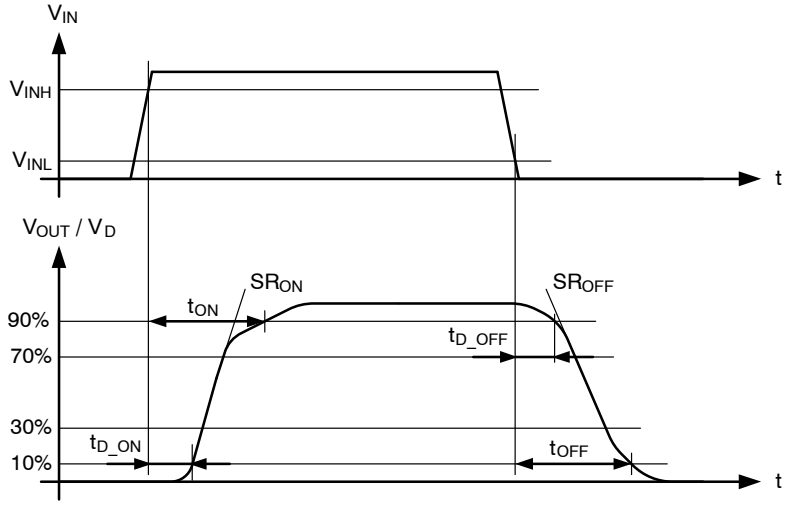


Figure 7. Resistive Load Switching Timing

Output Clamping with Inductive Load Switch Off

The output voltage V_{OUT} drops below GND potential when switching off inductive loads. This is because the inductance develops a negative voltage across the load in response to a decaying current. The integral clamp diode (Z_{CL}) clamps the negative output voltage to a certain level relative to the supply voltage V_D. During output clamping with inductive load switch off, the energy stored in the inductance is rapidly dissipated in the device resulting in high power dissipation. This is a stressful condition for the device and the maximum energy allowed for a given load inductance should not be exceeded in any application.

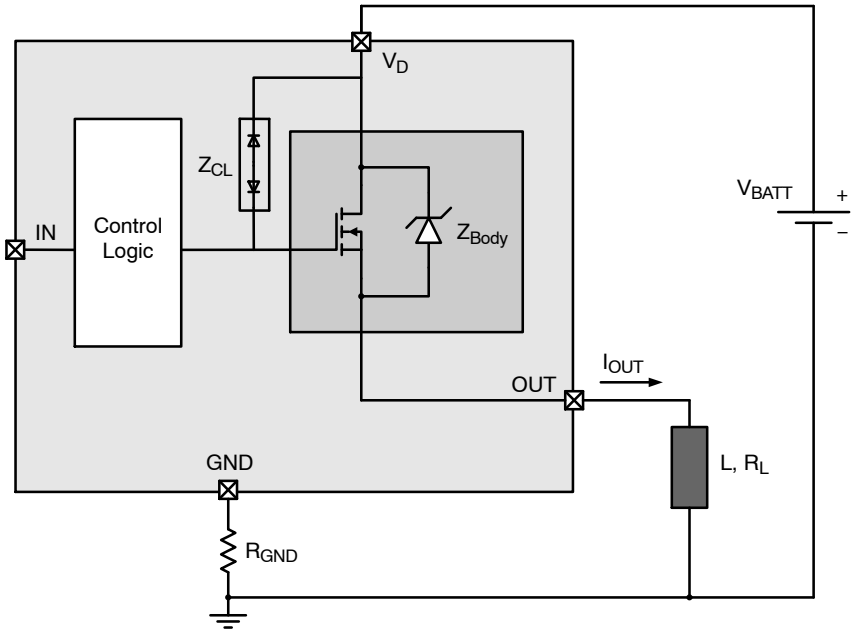


Figure 8. Output Clamping

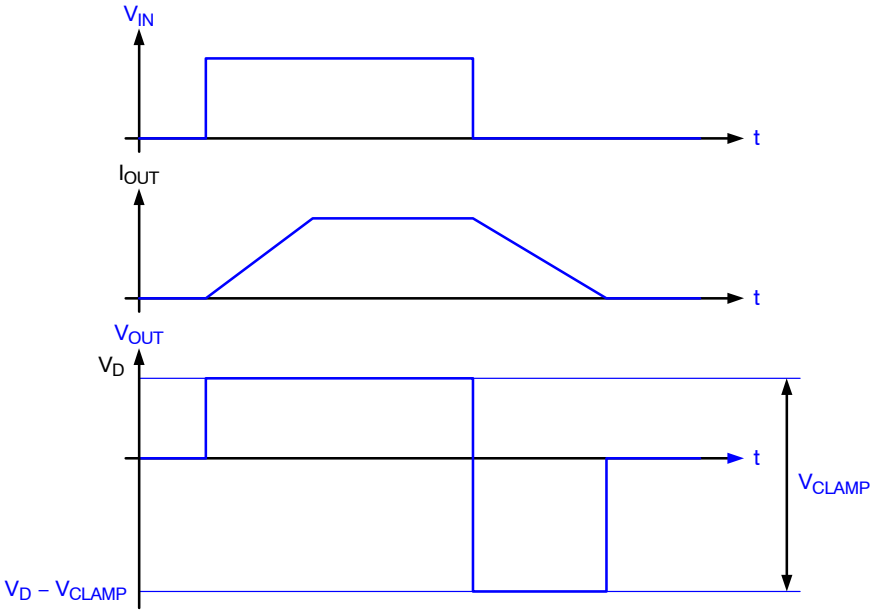


Figure 9. Inductive Load Switching Timing

The channel's energy capability [J] for inductive switching is given as follows, referring to Figure 8:

$$E = V_{ZCL} \cdot \left[\frac{V_D - V_{ZCL}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_{OUT}}{V_D - V_{ZCL}}\right) + I_{OUT} \right] \cdot \frac{L}{R_L} \quad \text{(eq. 1)}$$

Protection Features

In application, the device can be subject to stressful conditions which are outside of normal operating range. To prevent damage and destruction of the device from these fault conditions, several protection functions are integrated in device design. It is important to diagnose and remove any fault condition that may exist since the protection functions cannot prevent damage over sustained fault state operation.

Inverse Current

If an inverse current is applied in the application, V_{OUT} observes a potential greater than V_D. In such case, if the device was OFF initially, the control logic allows the output stage to be turned on if V_{IN} is asserted Low → High. Such an operation limits the power dissipation across the device during inverse current as the body diode losses are succeeded by output FET R_{ON}. In case the device was initially switched ON, it is allowed to stay ON during inverse current mode. The parameter R_{ON_INV} (Refer Table 4) specifies the resistance offered by the output stage in an inverted configuration. The current sense output stays low during inverse current conduction at the output stage. Further, during inverse current operation, protection features as discussed in the ON State Fault Retry Strategy section may not be available.

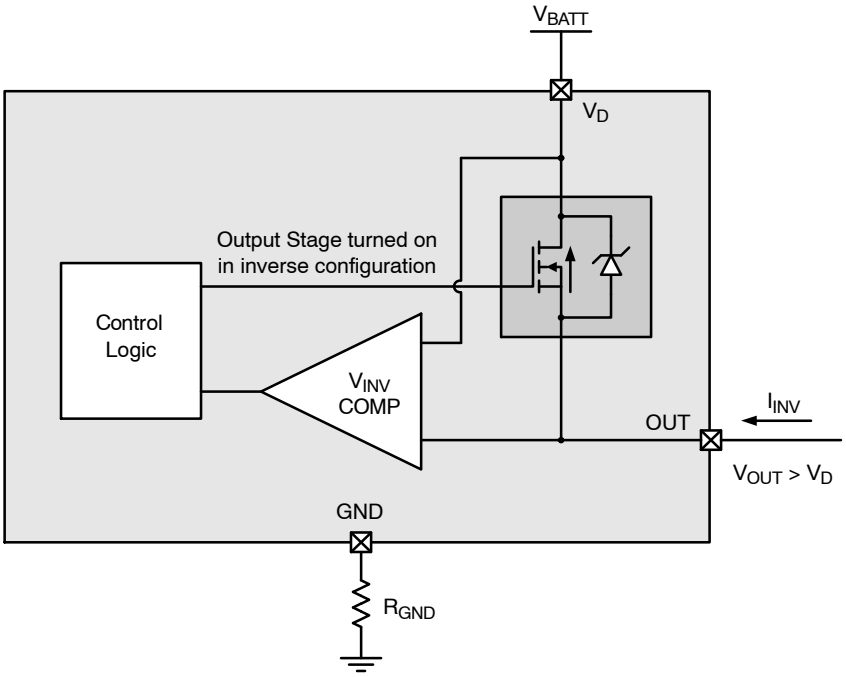


Figure 10. Inverse Current

Loss of Ground Protection

When device or ECU ground connection is lost and the load is still connected to ground, the device will turn the output OFF. In loss of ground state, the output stage is held OFF independent of the state of the input. Protection mechanisms and current sense output of the device will not be available during loss of device ground. Series resistors are recommended between the device and microcontroller to prevent the I/O pins from providing a parasitic GND path through microcontroller.

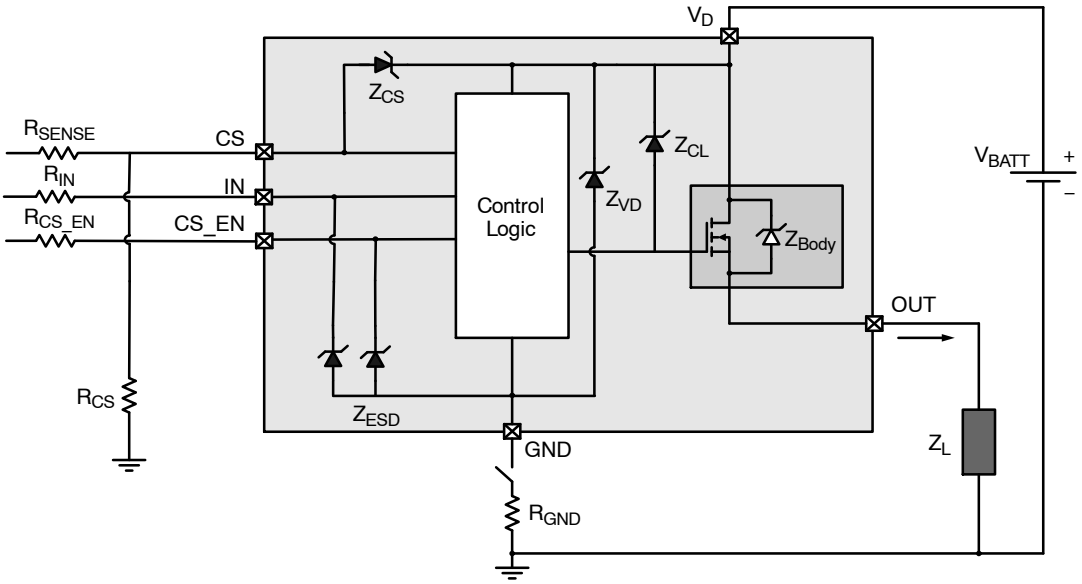


Figure 11. Loss of Ground Protection

Undervoltage Protection

The device has two under voltage threshold levels, V_{D_MIN} and V_{D_UV}. Switching function (ON/OFF) requires supply voltage to be at least V_{D_MIN}. The device features a lower supply threshold V_{D_UV}, above which the output can remain in ON state, if already ON. The protection and diagnostic features are available and functional down to V_{D_UV} (if switch already ON), however, may deviate from the nominally specified parametric performance.

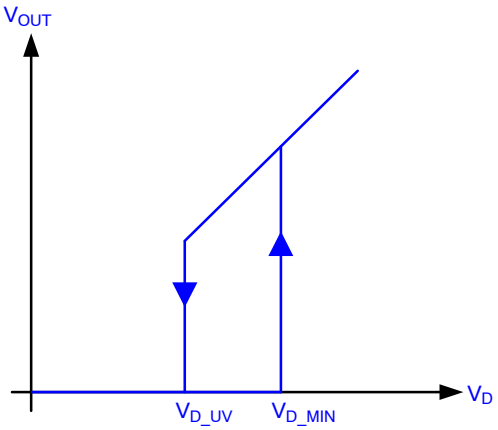


Figure 12. Under-voltage Behavior

In case the supply voltage drops below V_{D_UV} while the channel is ON (V_{IN} = High), the output stage shuts off and a delay time $t_{UV_Recover}$ is incorporated before turning on the output again once the supply increases more than V_{D_MIN}. Such a protection scheme precludes fast repetitive turn on and turn off events and reduces the transient stress on the device as the supply periodically increases or decreases around the under-voltage threshold while conducting high currents. Once initiated, this delay timer is independent of the transitions at the IN pin as shown in Figure 13 below. The delay $t_{UV_Recover}$ is not present if the power supply voltage is greater than V_{D_MIN} at the time of turning the channel ON (V_{IN}: Low → High).

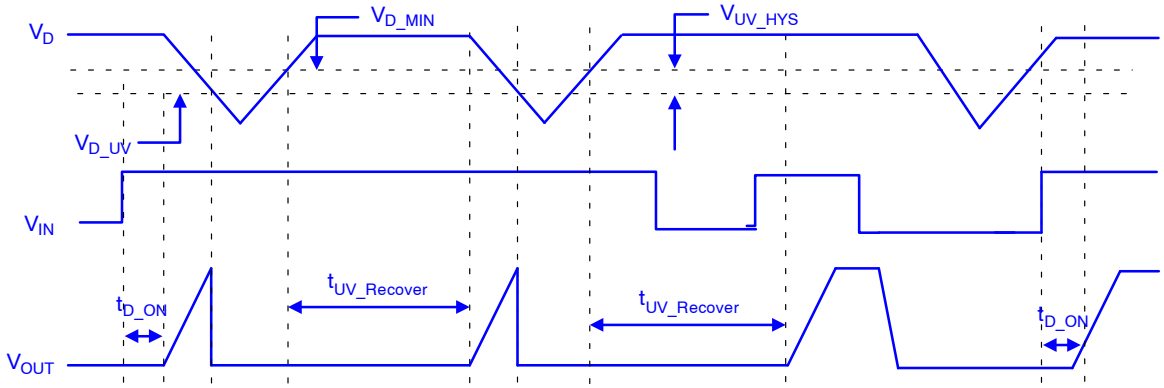


Figure 13. Under-voltage Recovery Timing

Overvoltage Protection

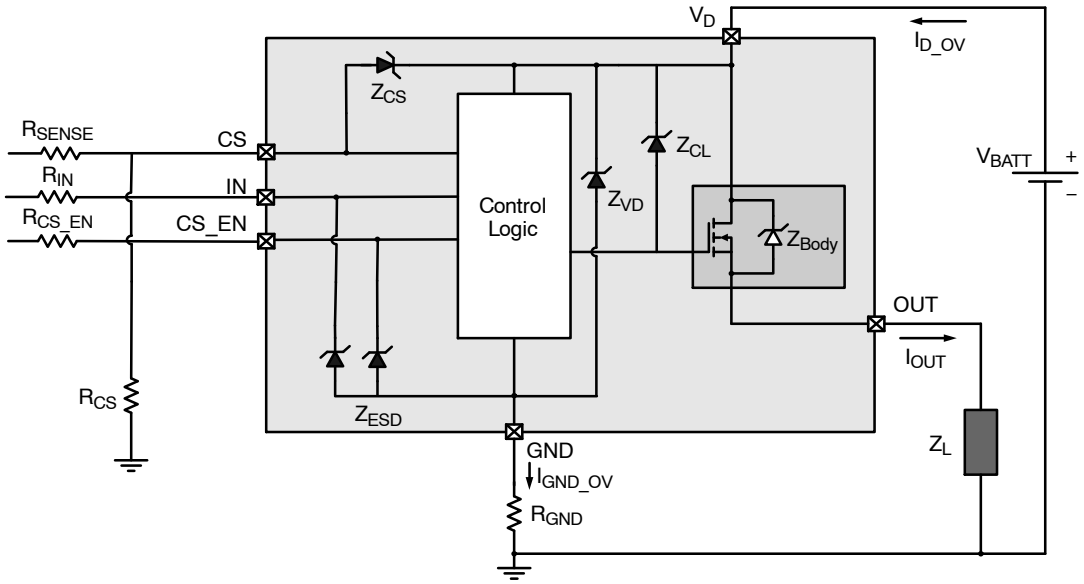


Figure 14. Overvoltage Protection Circuit

The NCV84003F employs a set of over-voltage protection Zener clamp diodes – Z_{VD}, Z_{CL}, Z_{ESD} and Z_{CS}, which protect the device against abnormal high voltage events. Z_{VD} protects the logic part by clamping the voltage between supply pin V_D and ground pin GND to V_{ZVD}. Z_{CS} limits voltage at current sense pin IS to $V_D - V_{ZCS}$. The output power MOSFET's integral body diode Z_{CL} provides protection by clamping the voltage across the MOSFET (between V_D pin and OUT pin) to ~V_{ZCL}. During overvoltage protection, current flowing through Z_{VD}, Z_{CS} and Z_{CL} must be limited. Load impedance Z_L limits the current in output clamp. In order to limit the current in Z_{VD}, a resistor, R_{GND}, is required in the GND path. External resistors R_{CS} and R_{SENSE} limit the current flowing through Z_{IS} and out of the IS pin into the micro-controller I/O pin. With R_{GND}, GND pin voltage is elevated to $V_D - V_{ZVD}$ when the drain potential V_D rises above V_{ZVD}. ESD diodes Z_{ESD} clamp the voltage at logic pins IN and CS_EN close to the GND pin voltage $V_D - V_{ZVD}$. External resistors R_{IN} and R_{CS_EN} are required to limit the current flowing out of the logic pins into the micro-controller I/O pins. During overvoltage exposure, the device transitions into a self-protection state, with automatic recovery after the supply voltage comes back to the normal operating range. The parametric spec, diagnostic capability as well as short circuit robustness and energy capability cannot be guaranteed during overvoltage exposure.

Reverse Battery Protection

In case of Reverse Battery connection, the external load limits the current through the body diode of the output FET. An integrated blocking mechanism blocks the reverse current flowing into the GND and reduces the constraints on the value of R_{GND}. The diagnostic output stays OFF in a reverse battery configuration and no protection feature such as current limitation or over-temperature shutdown is available. A typical application setup for reverse battery protection is shown in Figure 15. The current in the logic

pins' ESD protection diodes are limited by resistors R_{IN} and R_{CS_EN}. Resistors R_{CS} and R_{SENSE} limit the current flowing in the CS pin. The resistor values have to be chosen to limit the current within the current ratings specified in the absolute maximum rating section.

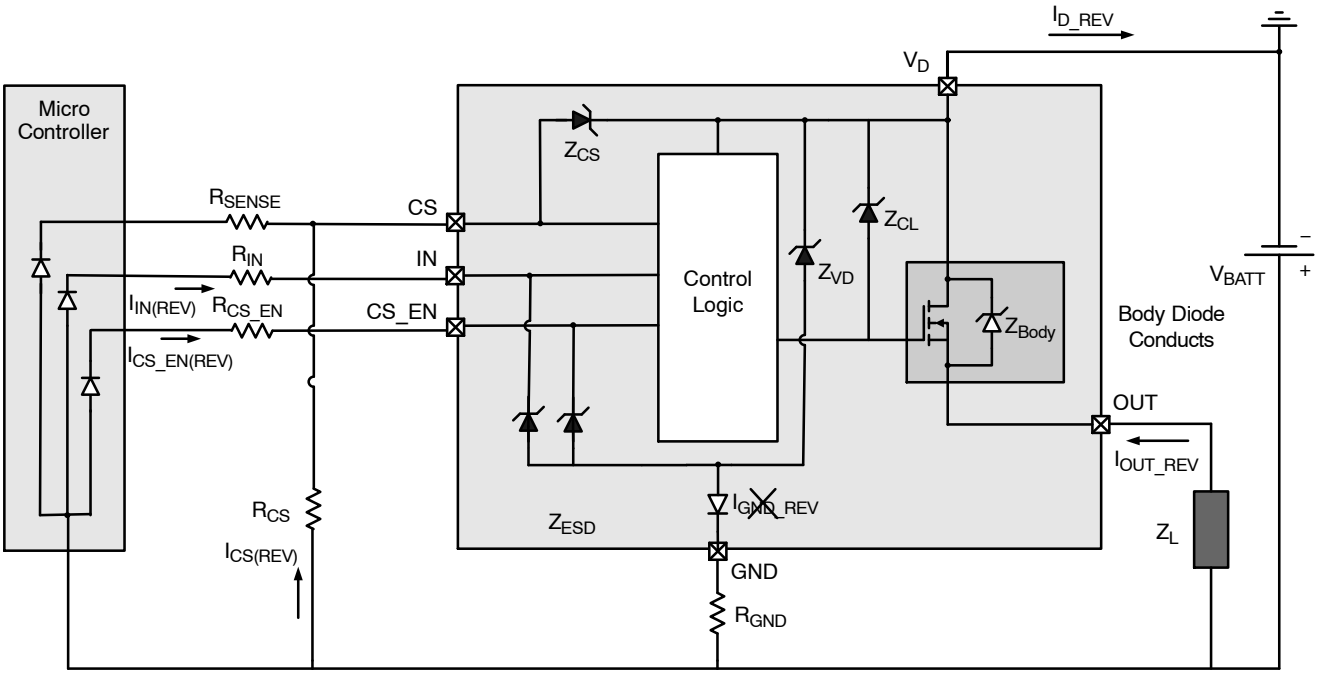


Figure 15. Reverse Battery Protection Circuit

Overload Protection

Over-current detection as well as over temperature shutdown mechanisms is integrated into NCV84003F to provide protection from overload conditions such as bulb inrush or output short to ground.

Over-Current Shutdown

In case of overload, NCV84003F limits the current in the output power MOSFET to a safe value (Refer Table 8). The device is immediately turned off once a peak current equal to I_{LIM} is detected thereby preventing any further power dissipation. To ensure the inrush requirements of bulb/capacitive loads, a re-try strategy is defined in the section On-State Fault Retry Strategy.

It's possible for the current profile to observe overshoots beyond the specified I_{LIM} threshold such as in case of transient short circuits with extremely low impedance because of the delay between current detection and consequent shut-off of the output stage. It should be noted that the overcurrent detection thresholds specified in Table 8 are specific to turning the device on into a short circuit with output impedance per AEC Q100-012 Load Short Circuit. Any increase in the load/supply inductance may overstress the device and an external freewheeling path is recommended to discharge the short circuit current in such case.

The over-current detection threshold of the device is reduced to a lower value in case of high drain-source voltage. This is done to limit the amount of power dissipation and consequential thermal transients. The curve below depicts the trend in normalized I_{LIM} where the value "1" represents the peak measured at V_{DS} = 5 V.

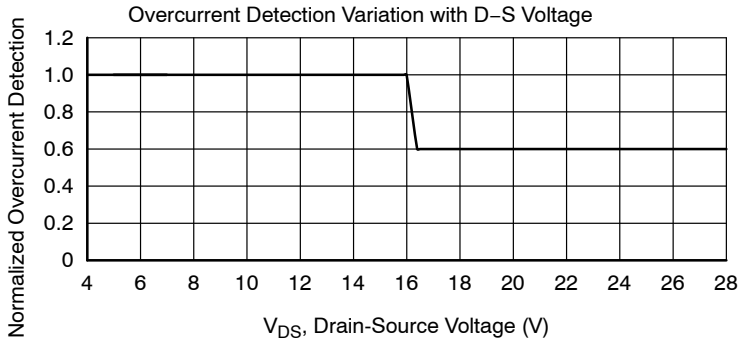


Figure 16. Over-Current Detection Variation with Drain-Source Voltage

A similar protection logic is applied at high Drain voltages, specifically for conditions such as Jump Start (Refer Table 8).

Over Temperature Protection

NCV84003F has two over temperature shutdown mechanisms. They are implemented by incorporating an absolute and a differential temperature sensor. To prevent damage and/or destruction, when either of the two sensors is activated, the output will be switched OFF. In case of a prolonged high power dissipation condition, a rapid increase in the junction temperature creates a severe temperature gradient within the device. When this differential temperature swing reaches the defined threshold (T_{DTSD}, per Table 8), the differential temperature sensor is activated thereby switching OFF the device. In case if the junction temperature reaches thermal shutdown temperature T_{TSD}, the absolute temperature sensor is activated, and the output stage will be switched OFF. The output will be allowed to turn back ON when the differential temperature drops to a safe value determined by the hysteresis T_{TSD_HYS} (Refer Table 8) with a retry strategy presented in the next section.

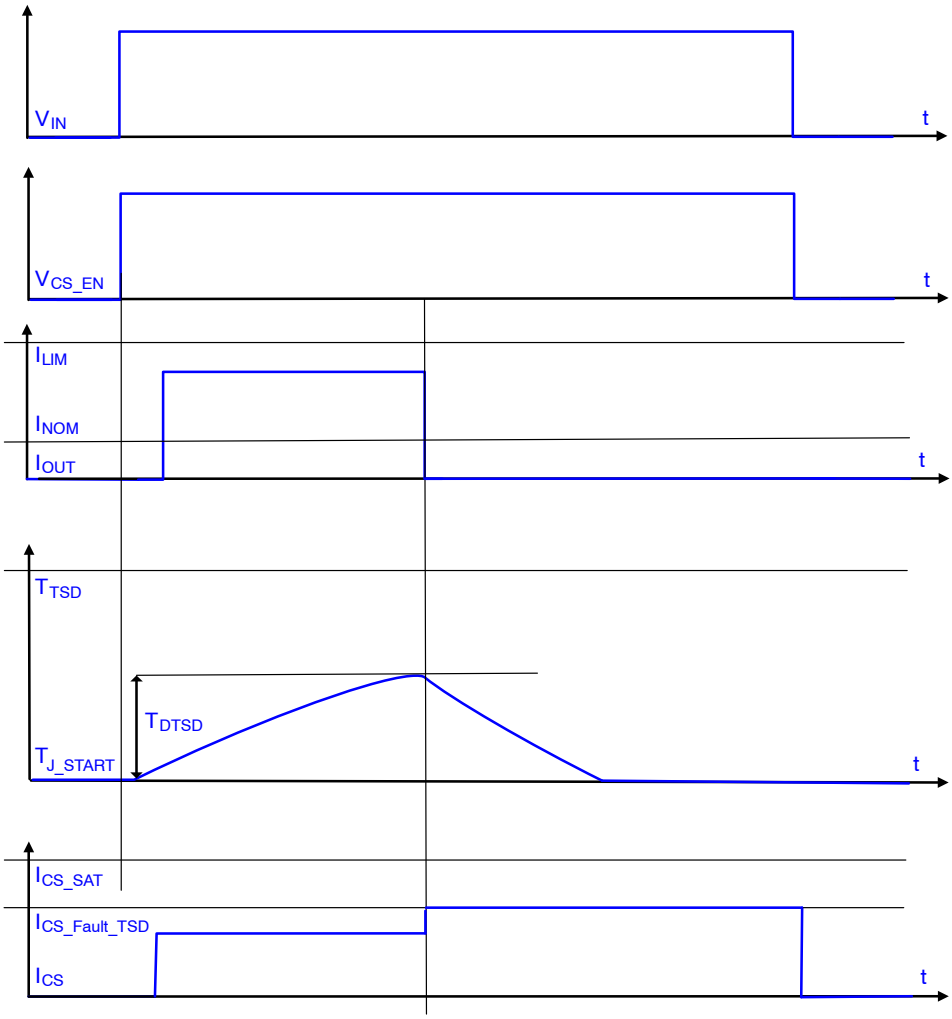


Figure 17. Over-Temperature Protection

ON State Fault Re-try Strategy

The timing diagram below explains the re-try strategy in case of a current limit and/or over-temperature fault state. It should be noted that while the particular example below considers a short circuit to GND, or a current limit condition, the same philosophy can be applied to re-tries in case of an over-temperature event.

When exposed to the fault conditions mentioned above, the output stage is latched off after incrementing the fault counter once to protect the device from subsequent high power re-try pulses. The fault counter can be reset to zero (default) by forcing IN low for a time period $t > t_{IN(Rst)}$, or by forcing a diagnostic enable pulse while IN = low as shown above. If the IN pin is switched Low → High before the $t_{IN(Rst)}$ timer expires, then the output stage stays off. The timer is reset and starts over again when the input goes low the next time. A current sense enable based reset provides a faster solution to reset the counter (typically used in cases where the application microcontroller detects a normal operating condition, and a quick re-start is desired).

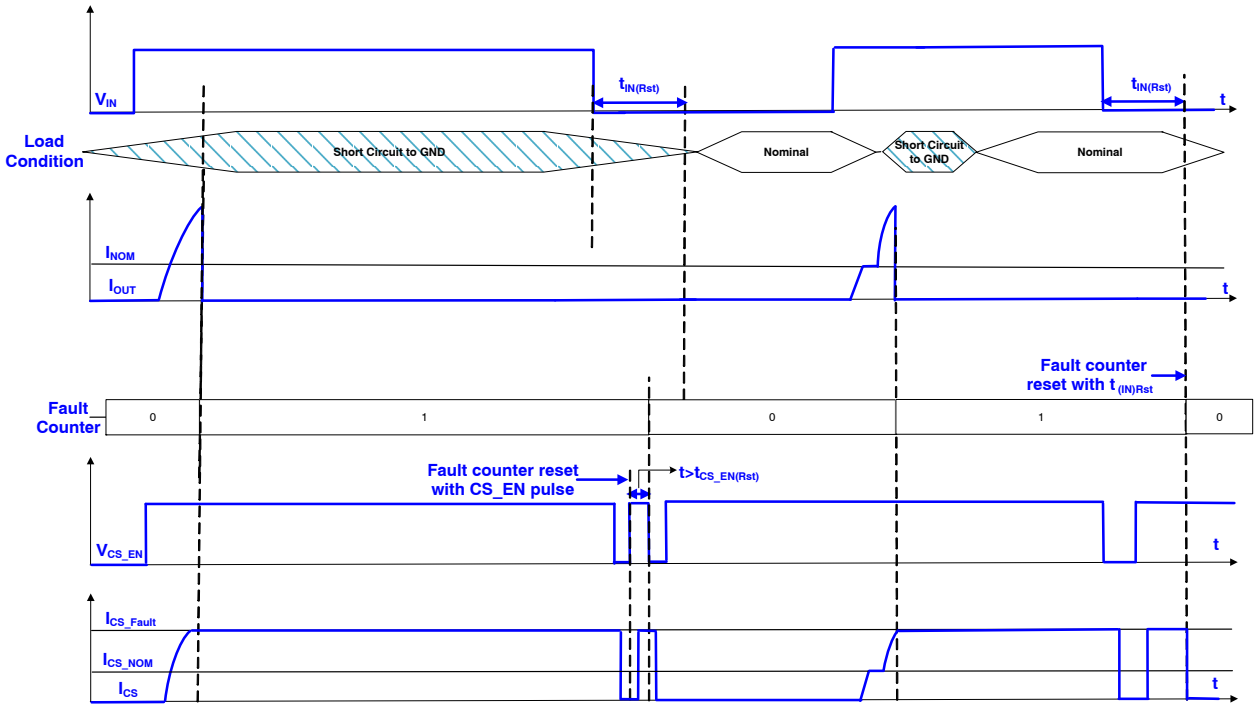


Figure 18. Re-try Strategy in Case of Current Limit and/or Over-Temperature

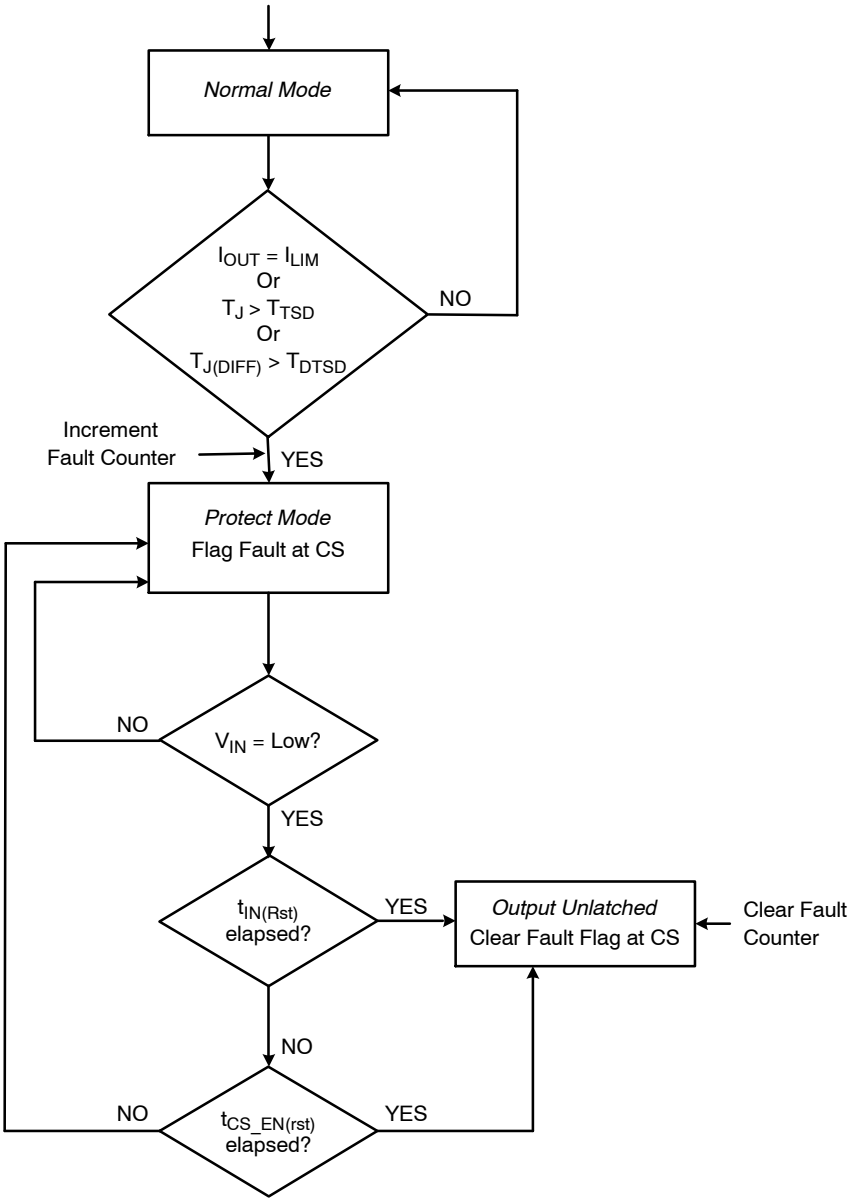


Figure 19. On-State Re-try Strategy Flowchart

Current Sense Output Timing

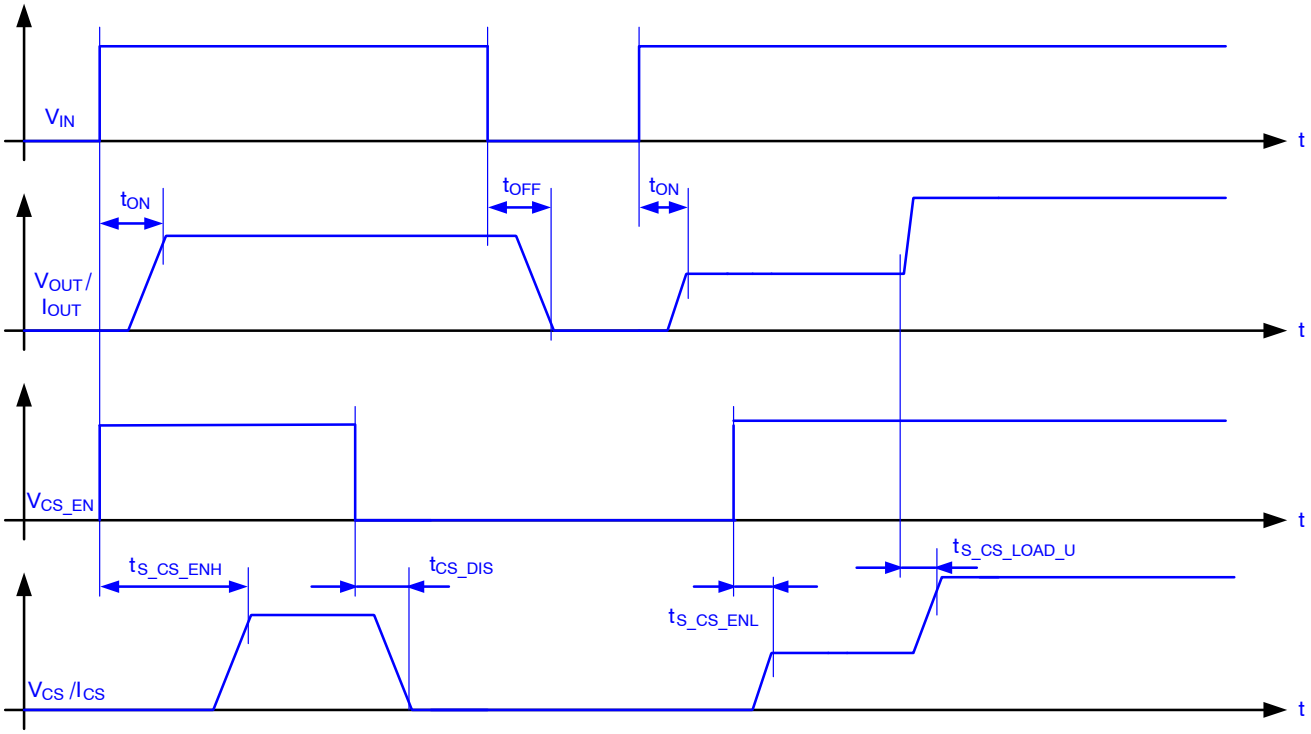


Figure 20. Current Sense Timings

Open Load/Short to V_{BATT} Detection in OFF State

Open load diagnosis in OFF state can be performed by activating an external resistive pull-up path (R_{PU}) to V_{BATT}. To calculate the pull-up resistance, external leakage currents (designed pull-down resistance, humidity-induced leakage etc) as well as the open load threshold voltage V_{DS_OSOL} have to be taken into account. A switch can be used open the battery connection to R_{PU} to prevent undesired leakage through this path in case an open load diagnostics is not required.

A short circuit to V_{BATT} in off state is also detected by the same analog circuit block.

It should be noted that OSOL Fault current range is exclusive to and lower than other fault conditions such as a TSD or a current limit. This segregation of fault levels will help user to distinguish an OSOL fault from a case where a fault is being flagged high in OFF state due to an un-expired Fault counter (Refer to Table 10 – Diagnostic Truth Table).

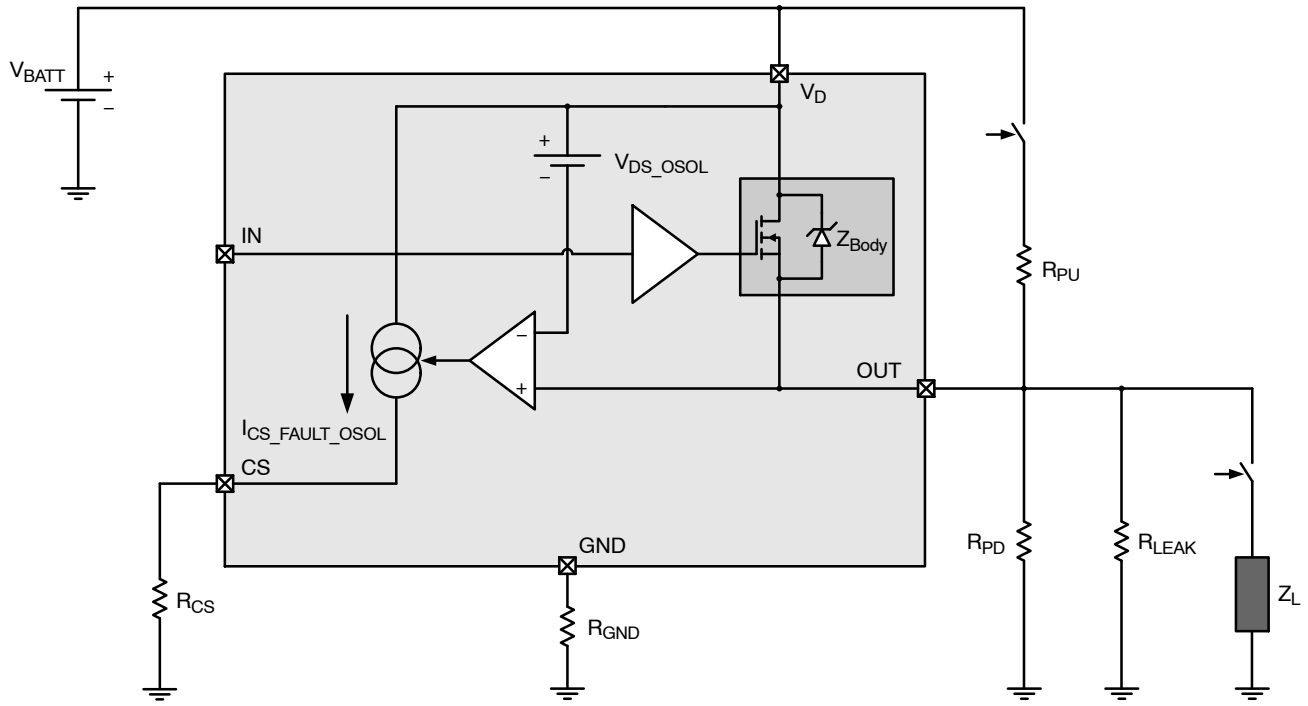


Figure 21. OFF State Open Load Detection Circuit

Typical Characteristic Curves

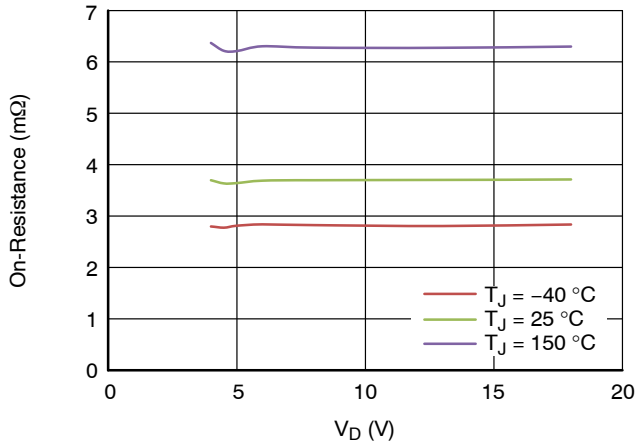


Figure 22. On-Resistance vs. V_D

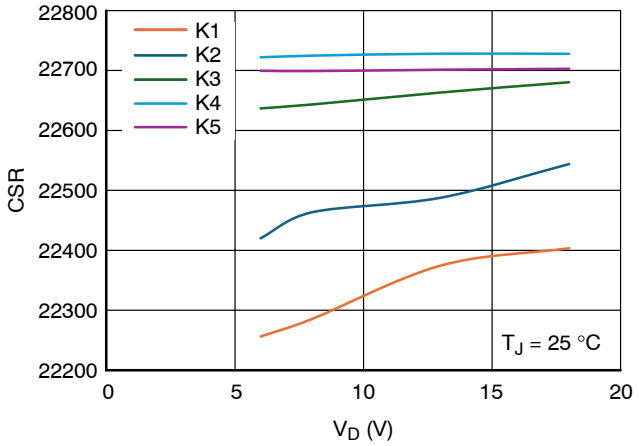


Figure 23. Current Sense Ratio vs. V_D

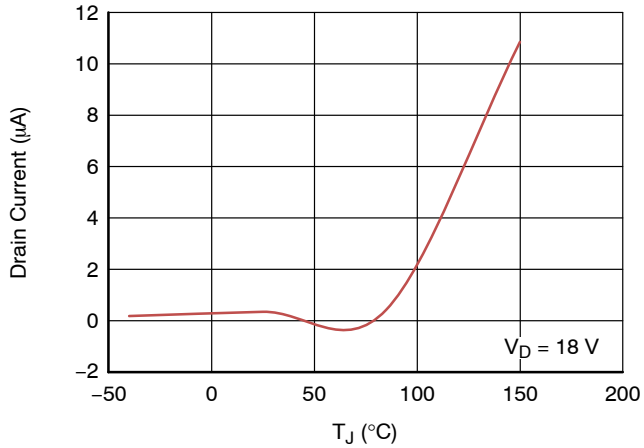


Figure 24. Quiescent Current vs. T_J

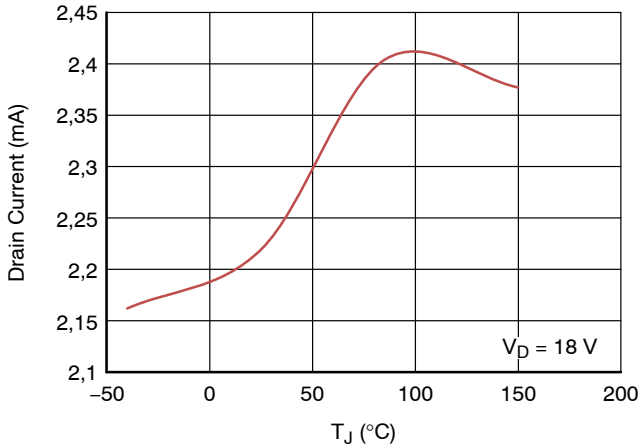


Figure 25. Quiescent Current, Diagnostic Active vs. T_J

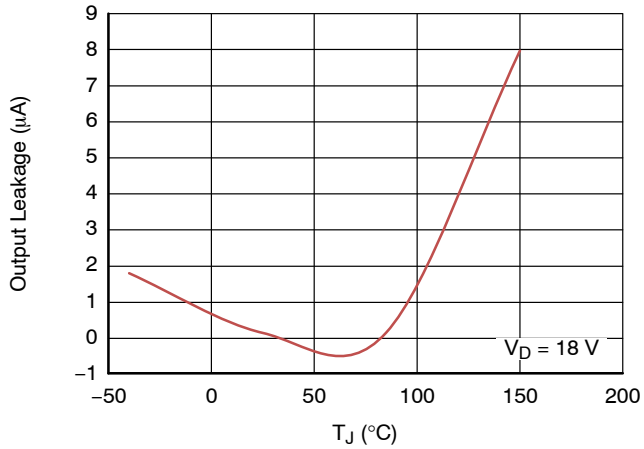


Figure 26. Output Leakage vs. T_J

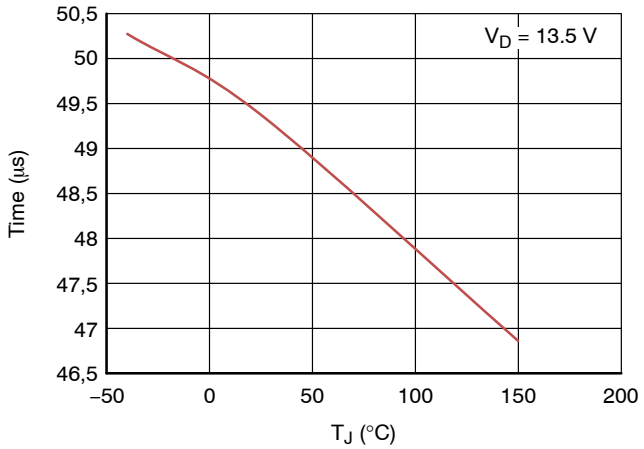


Figure 27. Turn Off Delay vs. T_J

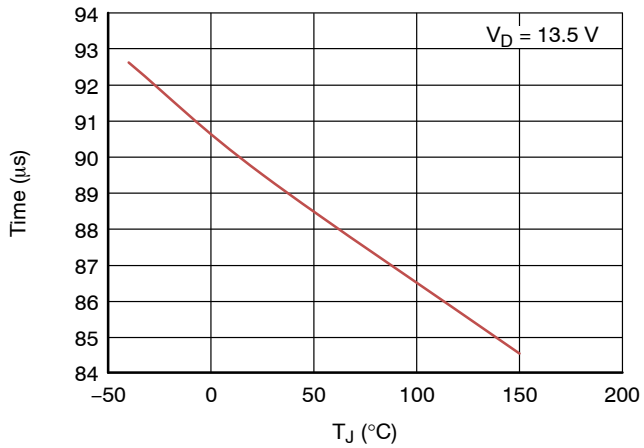


Figure 28. Turn Off Time vs. T_J

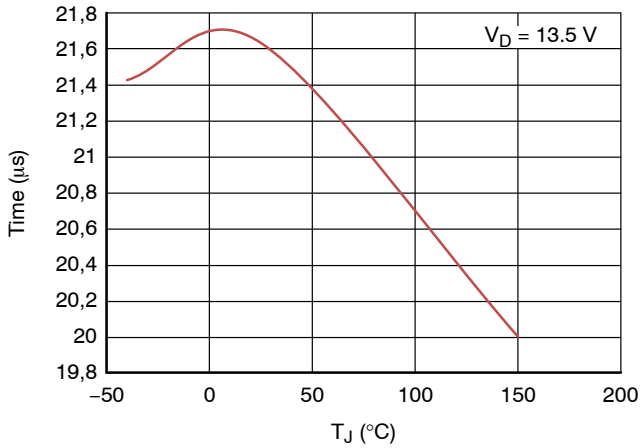


Figure 29. Turn On Delay Normal Mode vs. T_J

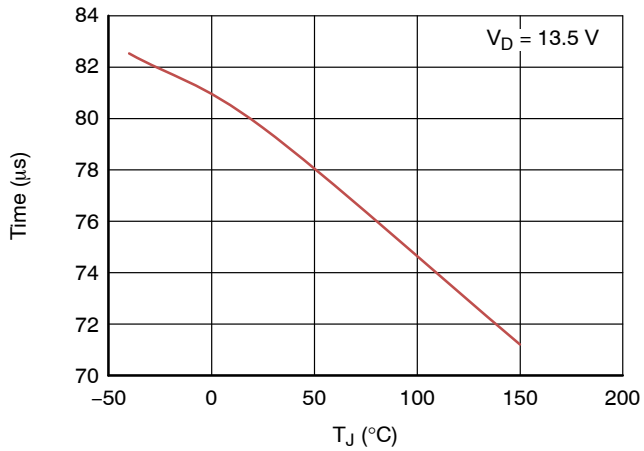


Figure 30. Turn On Time Normal Mode vs. T_J

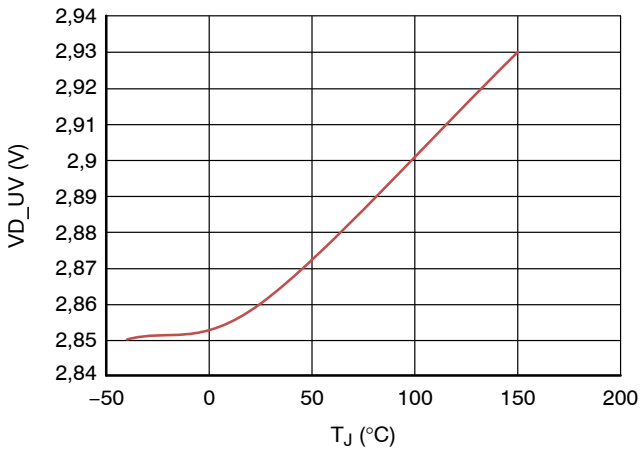


Figure 31. Undervoltage Shutdown (Turn-Off) vs. T_J

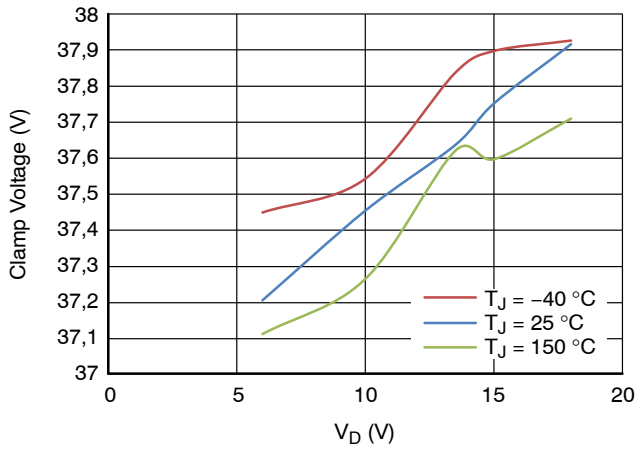


Figure 32. Drain-to-Source Clamping vs. T_J

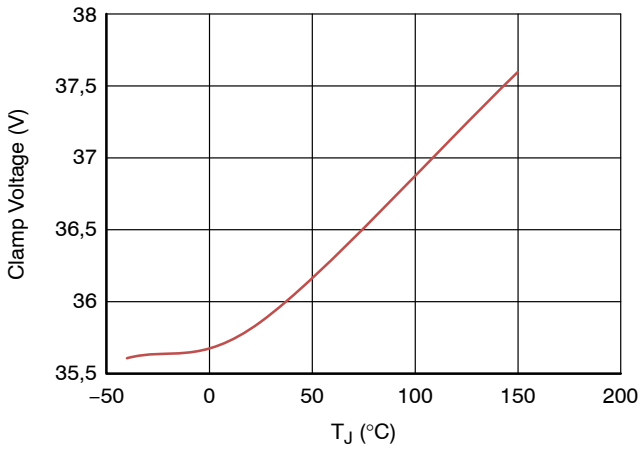


Figure 33. CS Clamp vs. T_J

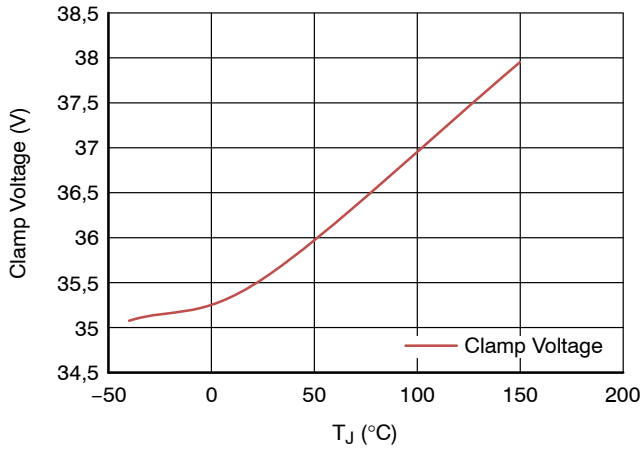


Figure 34. Overvoltage Clamp vs. T_J

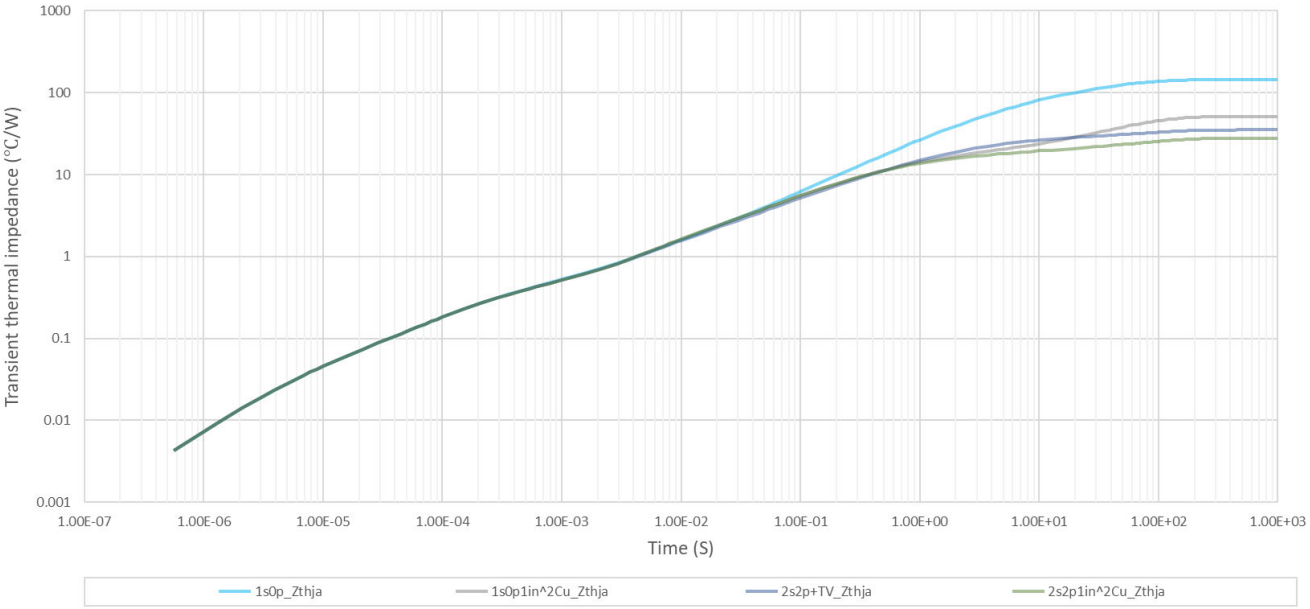
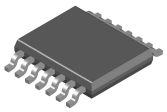


Figure 35. Transient Thermal Response

REVISION HISTORY

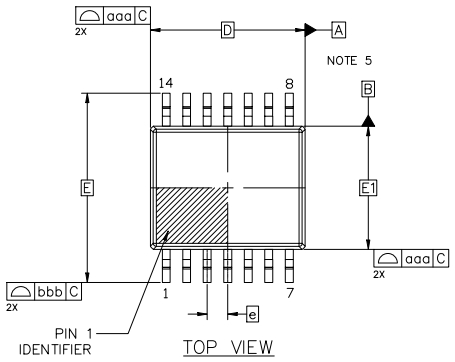
Revision	Description of Changes	Date
0	Initial datasheet release.	4/16/2026
1	Add notes 3,4,5, edits to table 3 and notes 6,7, edit header and rearrange columns on tables 4−9 and 11−13, text edit tables 10,13, text edit page 24, replace figure 16.	5/4/2026
2	Updated Typical Characteristics layout to 6-chart standard.	5/26/2026
3	Corrected marking information code.	8/11/2026

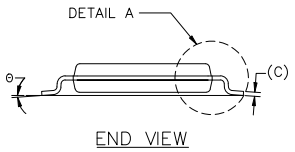


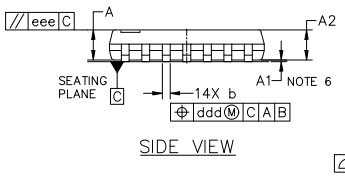
TSSOP14 4.90x3.90x0.95, 0.65P
CASE 948BZ
ISSUE C

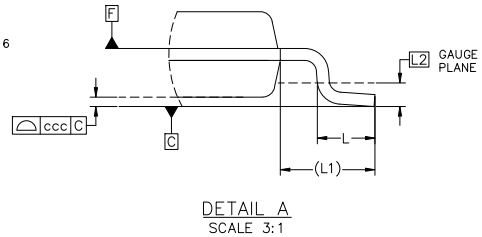
DATE 10 JUL 2025

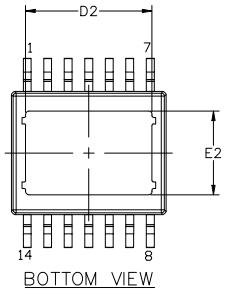
NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M, 2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLE IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.127 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY INCLUDING THE THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGUARATIONS.
7. LEAD THICKNESS (c) AND LEAD WIDTH (b) INCLUDE PLATING THICKNESS.

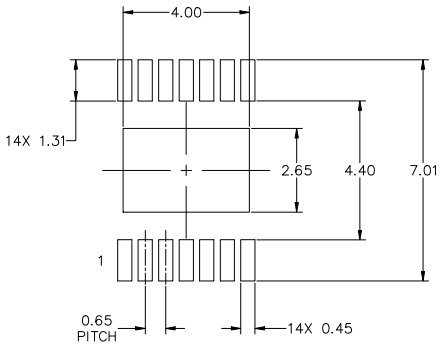










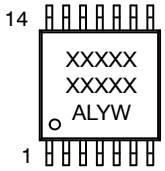


MILLIMETERS			
DIM	MIN	NOM	MAX
A	---	---	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.20	0.25	0.30
c		0.20 REF.	
D		4.90 BSC	
D2	3.90	4.00	4.10
E		6.00 BSC	
E1		3.90 BSC	
E2	2.55	2.65	2.75
e		0.65 BSC	
L	0.42	0.52	0.62
L1		1.05 REF.	
L2		0.25 BSC	
θ	0°	4°	8°
TOLERANCE FOR FEATURE CONTROL FRAME			
aaa		0.10	
bbb		0.20	
ccc		0.08	
ddd		0.10	
eee		0.08	

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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