Self-Protected High Side Driver With IDLE Mode & Analog Current Sense

NCV84003G

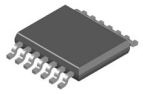
The NCV84003G is a fully protected single channel high side driver that can replace mechanical fuses and provide power in a smart power distribution architecture. It can also switch a wide variety of loads, such as bulk capacitors, bulbs, solenoids, and other actuators. The device incorporates advanced features designed for zonal applications such as a smart low power IDLE mode, a dedicated capacitive load charging mode, adjustable overcurrent thresholds and built-in I^2t profiles for replacing conventional melting fuses. The device also features over-temperature shutdown with automatic latch-off. A Current Sense pin provides precision analog current monitoring, fault indication, as well as readback of internal configuration and I^2t status.

Features

- 5 V/3.3 V Compatible Control Input
- Low Standby Current
- Smart Low Power IDLE Mode with Extremely Low Operating Current & Auto Transition to Normal Mode
- Dual-purpose IDLE Status Feedback and Control
- Capacitive Charge Mode for Active Inrush Management with Auto-entry and Exit
- Adjustable Overcurrent Threshold
- Adjustable Intelligent I^2t Profile for Replacing Melting Fuses
- Absolute and Differential Thermal Shutdown
- Intelligent Retry with Latch Off in Protect State
- Proportional Analog Current Sense Output Multiplexed with Discrete Fault Output Levels for Fault Differentiation
- Configuration and Status Readback on CS
- Off State Open Load and Short Circuit to V_{BATT} Detection
- Under-voltage Shutdown and Over-voltage Protection
- Protection against Loss of Ground and Loss of V_{BATT}
- Inverse Current Protection with FET Turn On in Inverse Mode
- ESD Protection
- Reverse Battery Protection with External Components
- AEC-Q100 Qualified and PPAP Capable

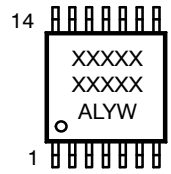
FEATURE SUMMARY

Nominal Operating Voltage Range	V_D	6 to 18	V
R_{ON} @ T_J = 25 °C	R_{ON}	3.6	mΩ
Default Output Current Limit (typ)	I_{lim}	85	A
IDLE mode GND Operating Current @ T_J = 85 °C	I_{GND}	88	μA



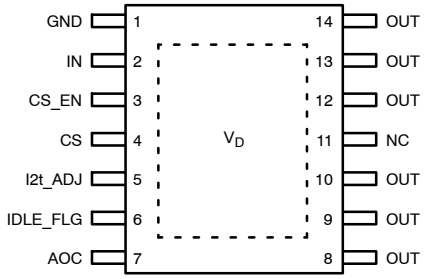
TSSOP14 EP
CASE 948BZ

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot Number
Y = Year
W = Work Week

PACKAGE PIN DESCRIPTION



(Top View)

SAFETY DESIGN – ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

ORDERING INFORMATION

Device	Package	Shipping†
NCV84003GPAR2G	TSSOP14 EP (Pb-Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Applications

- Replace Fuses Rated between 20 A to 5 A in Zonal Platforms
- Power on Bulk Capacitors, Resistive, and Inductive Loads
- Automotive / Industrial

© Semiconductor Components Industries, LLC, 2024

Table 1. PIN DESCRIPTIONS

Pin #	Symbol	Description
1	GND	Ground Reference
2	IN	Logic Level Input for Output Activation
3	CS_EN	Logic Level Input for Diagnosis Enable
4	CS	Current Sense/Diagnostic Output
5	I2t_ADJ	Adjustable I^2t Profile Input
6	IDLE_FLG	IDLE State Flag for MCU
7	AOC	Adjustable Over-Current Threshold Input
11	NC	No Connect
08−10, 12−14	OUT	Output
E-pad	VD	Battery Connection

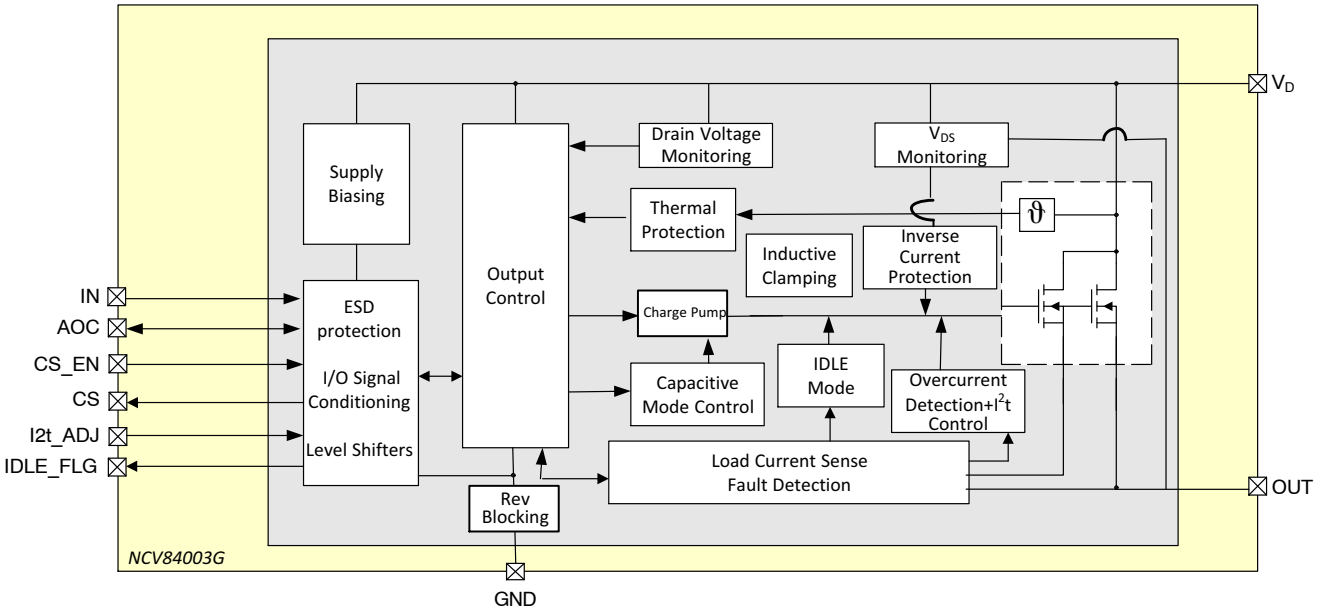


Figure 1. Block Diagram

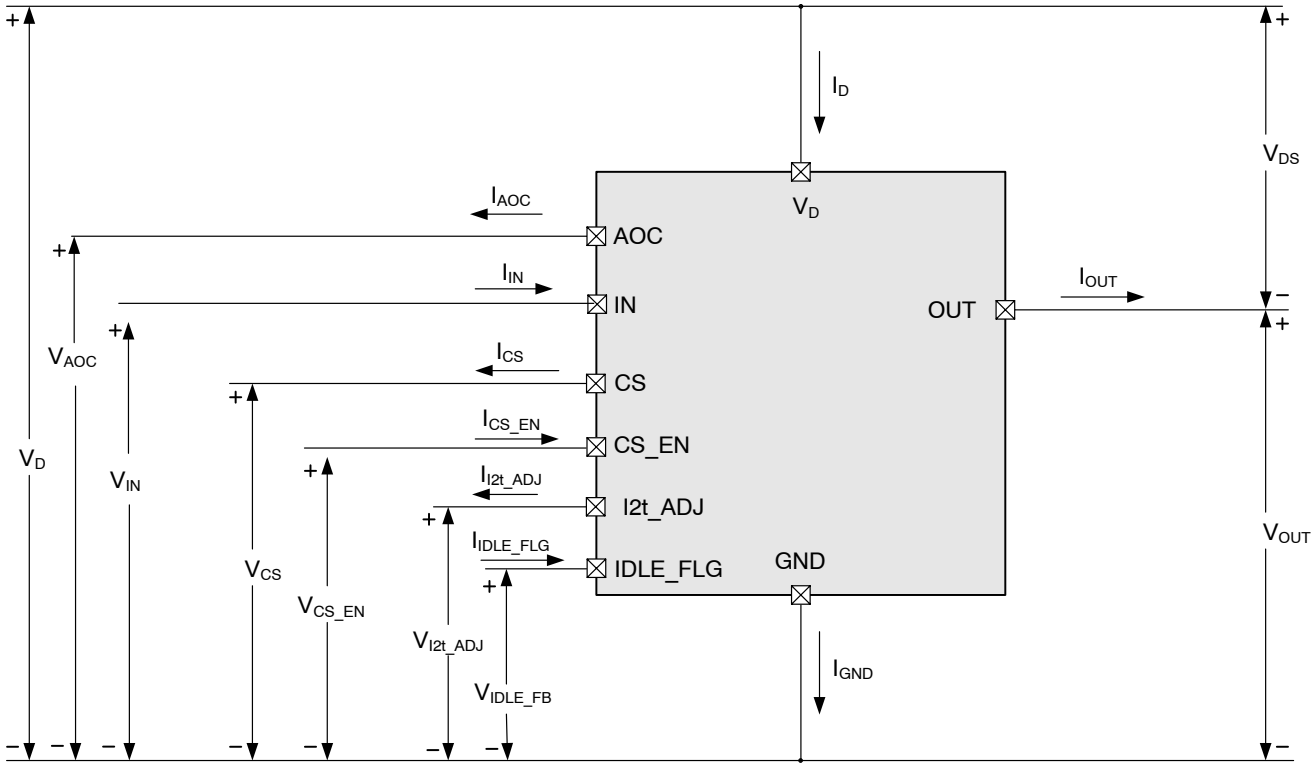


Figure 2. Voltage and Current Definitions

Electrical Specifications

Table 2. MAXIMUM RATINGS (Note 1)
−40 °C ≤ T_J ≤ 150 °C unless otherwise specified

Rating	Symbol	Value		Unit
		Min	Max	
GENERAL				
Supply Voltage (Note 2)	V_D	−0.3	28	V
Supply Voltage for Load Dump Protection	V_{D_LD}		35	V
Supply Voltage for Short Circuit Protection	V_{D_SC}	0	24	V
Reverse Polarity Voltage, t < 2 min, Load : 2 Ω, Setup : Refer to Figure 21	V_{D_REV}	0	16	V
DIGITAL INPUT PINS: IN, CS_EN				
Current at Input Pins	$I_{DIG_IN_MAX}$	−1	1	mA
Current at Input Pins in Rev Battery, t < 2 min	$I_{DIG_IN_MAX_REV}$	−1	10	mA
Voltage at Input Pins	$V_{DIG_IN_MAX}$	−0.3	6.5	V
IDLE_FLG PIN				
Current at IDLE_FLG Pin	I_{IDLE_MAX}	−1	1	mA
Current at IDLE_FLG Pin in Rev Battery, t < 2 min	$I_{IDLE_MAX_REV}$	−1	10	mA
Voltage at IDLE_FLG Pin	V_{IDLE_MAX}	−0.3	6.5	V
CURRENT SENSE OUTPUT				
Current at Current Sense Output	I_{CS_MAX}	−25	$I_{CS_Fault_ILIM}$	mA
Voltage at Current Sense Output	V_{CS_MAX}	−0.3	V_D	V
ANALOG INPUT PINS: AOC PIN, I2T_ADJ PIN				
Current at Input Pin	$I_{ANA_IN_MAX}$	−1	1	mA
Voltage at Input Pin	$V_{ANA_IN_MAX}$	−0.3	6.5	V
OUTPUTS				
Power Dissipation T_A = 85 °C, T_J = 150 °C (Note 5)	P_{MAX}		3	W
Drain-Source Voltage at Power Transistor	V_{DS_MAX}		V_{ZCL}	V
Single Pulse Inductive Load Switching Energy (L = 1 mH, V_D = 13.5 V, I_{L_PEAK} = 6.4 A, T_{JSTART} = 150 °C)	E_{AS}		30	mJ
GROUND TERMINAL				
Current through GND Pin	I_{GND}	−50	50	mA
TEMPERATURES				
Operating Junction Temperature	T_J	−40	150	°C
Storage Temperature	$T_{J_storage}$	−55	150	°C
ESD				
ESD Susceptibility All Pins to Ground HBM	V_{ESD_HBM}	−2	+2	kV
ESD Susceptibility All Pins − Pin to Pin and Pin to Supply HBM	V_{ESD_HBM}	−1	1	kV
ESD Susceptibility OUTx to GND, V_D connected, HBM	$V_{ESD_OUT_HBM}$	−4	4	kV
ESD Susceptibility All Pins CDM	V_{ESD_CDM}	−500	500	V
ESD Susceptibility Pin (Corner Pins), CDM	V_{ESD_NC}	−750	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Not subject to production testing.
2. For transient application only. Extended operation at absolute maximum voltage may affect device reliability.
3. HBM test setup per AEC-Q100:EIA-JESD22-A114-B.
4. CDM test setup per AEC-Q100:EIA-JESD22-C101-A.
5. Board construction based on JEDEC JESD 51-7 for a four layer 2s2p board with natural convection. Vias were added under the exposed pad as shown in Figure 3.

Table 3. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max Value	Unit
Thermal Resistance			
Junction-to-Top (Note 7)	P_{si_JT}	1.9	°C/W
Junction-to-EPAD (Note 7)	$P_{si_Je\text{-}PAD}$	1.3	°C/W
Junction-to-Ambient – 1s0p Min Pad (Note 6)	R_{thJA}	145	°C/W
Junction-to-Ambient – 1s0p +1in^2 Cu (Note 6)	R_{thJA}	51	°C/W
Junction-to-Ambient – 2s2p Min Pad (Note 7)	R_{thJA}	35	°C/W
Junction-to-Ambient – 2s2p +1in^2 Cu (Note 7)	R_{thJA}	22	°C/W

6. Board construction based on JEDEC JESD 51-3 for a single layer 1s0p board with natural convection.
7. Board construction based on JEDEC JESD 51-7 for a four layer 2s2p board with natural convection. Vias were added under the exposed pad as shown below.

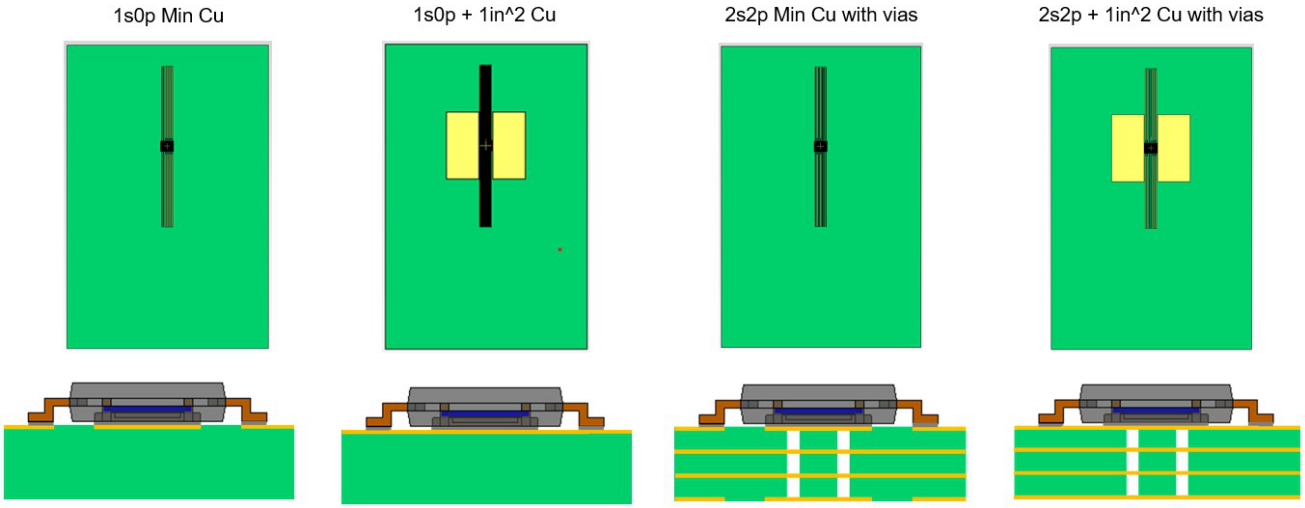


Figure 3. Board Construction for Thermal Performance

Table 4. SUPPLY ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) Typical Values measured @ V_D = 13.5 V, T_J = 25 °C

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Nominal Supply Voltage Range (Note 8)	V_{D_NOM}		6	13.5	18	V
Extended Supply Voltage Range (Notes 8, 9)	V_{DS_EX}	V_{IN} = 5 V, R_L = 4 Ω, 3.1 V ≤ V_D ≤ 28 V Ramp down V_D from 28 V to 3.1 V			0.5	V
Under Voltage Shutdown	V_{D_UV}	V_{IN} = 5 V, V_D Falling, From V_{DS} < 0.5 V to I_{OUT} = 0	2.4	2.9	3.1	V
Minimum Operating Voltage	V_{D_MIN}	V_{IN} = 5 V, V_D Rising, From I_{OUT} = 0 to V_{DS} < 0.5 V	2.9	3.4	4.1	V
Under Voltage Shutdown Hysteresis	$V_{D_UV_HYS}$			0.5		V
Supply Undervoltage Recovery Time – Normal Mode (Note 8)	$t_{UV_Recover_Norm}$	V_{CS_EN} = 5 V, V_{IN} = 0 V → 5 V after t > t_{Norm}, V_D Rising, From V_D = 0 V → $V_D \ge V_{D_MIN}$ to V_{DS} < 0.5 V (See Figure 18)	2.5	5	7.5	ms
Supply Undervoltage Recovery Time – CL Mode (Note 8)	$t_{UV_Recover_CL}$	V_{CS_EN} = V_{IN} = 0 V → 5 V, V_D Rising, From V_D = 0 V → $V_D \ge V_{D_MIN}$ to V_{OUT} = 10% V_D (See Figure 18)	300	600	900	μs
IDLE Mode Exit Threshold for Low V_D Operation	$V_{D_IDLE_Ext}$	V_{IN} = 5 V, I_L = 0.5 A V_D Falling, V_{IDLE_FLG} = High → Low	2.85	3.5	4.1	V
IDLE Mode Supply POR Threshold	$V_{D_IDLE_POR}$	Refer Figure 19	2.55	3.05	3.65	V
Supply Voltage to Block IDLE Entry from Normal Mode – Falling	$V_{D_IDLE_Block_F}$	Refer Figure 19	4.0	4.5	4.85	V
Supply Voltage to Allow IDLE Entry from Normal Mode – Rising	$V_{D_IDLE_Allow_R}$	V_{IN} = 5 V, I_L = 0.5 A V_D Rising, V_{IDLE_FLG} = Low → High	4.25	4.6	5.0	V
Quiescent Current	I_{Q_85}	V_D = 18 V, T_J ≤ 85 °C, V_{IN} = V_{CS_EN} = 0 V, V_{OUT} = 0 V			1.5	μA
Quiescent Current	I_{Q_150}	V_D = 18 V, T_J = 150 °C, V_{IN} = V_{CS_EN} = 0 V, V_{OUT} = 0 V		5	26	μA
Quiescent Current, Diagnostic Active	I_{Q_DIAG}	V_D = 18 V, V_{IN} = 0 V, V_{CS_EN} = 5 V		1.8	3	mA
Normal Operating Current	I_{GND_ON}	V_D = 18 V, V_{IN} = V_{CS_EN} = 5 V, V_{CS} < 5 V		5	6	mA
Operating Current in IDLE Mode	I_{GND_IDLE}	V_D = 18 V, V_{IN} = 5 V, V_{CS_EN} = 0 V, I_{OUT} = 0.5 A, T_J ≤ 85 °C			88	μA

8. Not subject to production testing.
9. Extended operation outside the nominal supply voltage range may affect device reliability. Parametric performance not guaranteed.

Table 5. POWER OUTPUT ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) Typical Values measured @ V_D = 13.5 V, T_J = 25 °C

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
On-state Resistance	R_{ON_25}	$I_{OUT} = I_{NOM}$ = 15 A, V_{IN} = 5 V, T_J = 25 °C		3.6		mΩ
On-state Resistance	R_{ON_150}	$I_{OUT} = I_{NOM}$ = 15 A, V_{IN} = 5 V, T_J = 150 °C			7.2	mΩ
On-state Resistance – Low Voltage	R_{ON_LV}	I_{OUT} = 2 A, V_D = 3.4 V, T_J = 150 °C			8.6	mΩ
On-state Resistance – Inverse Current	$R_{ON_INV_25}$	I_{OUT} = −4 A, V_D = 13.5 V, T_J = 25 °C		3.6		mΩ
On-state Resistance – Inverse Current	$R_{ON_INV_150}$	I_{OUT} = −4 A, V_D = 13.5 V, T_J = 150 °C			7.2	mΩ
On-state Resistance – IDLE Mode	$R_{ON_IDLE_85}$	I_{OUT} = 0.5 A, V_D = 13.5 V, $T_J \le 85$ °C			15	mΩ
Normal Mode Threshold	V_{DS_Norm}	V_{IN} = 5 V	0.5	1	2	V
Output Leakage Current	I_{LEAK_85}	$V_{IN} = V_{CS_EN}$ = 0 V, V_{OUT} = 0 V, T_J < 85 °C			1	μA
Output Leakage Current	I_{LEAK_150}	$V_{IN} = V_{CS_EN}$ = 0 V, V_{OUT} = 0 V, T_J < 150 °C			25	μA
IDLE Mode Enable Threshold – Falling	I_{IDLE_TF}	V_{IN} = 5 V, V_{IDLE_FLG} = Low → High	1	2	3	A
IDLE Mode Disable Threshold – Rising	I_{IDLE_TR}	V_{IN} = 5 V, V_{IDLE_FLG} = High → Low	1.25	2.5	3.75	A
Drain-to-Source Clamping Voltage ($V_D - V_{OUT}$)	V_{ZCL}	I_{OUT} = 10 mA, V_{IN} = 5 V → 0 V	35	36	40	V
Body Diode Forward Voltage	V_F	I_{OUT} = −1 A, T_J = 150 °C, $V_F = V_{OUT} - V_D$			0.7	V

10. Not subject to production testing.

Input Pins

All low-voltage inputs are compatible with 3.3 V and 5 V microcontroller supply voltages. All inputs comprise of a voltage Schmitt-trigger circuit to enable direct drive from voltage sources and prevent uncontrolled oscillations due to slow transitions at the inputs. Each input features a pull-down element to prevent uncontrolled input states in case of an open pin condition. In addition, the IN control provides an intelligent latch feature that allows the microcontroller in the application to observe a high−impedance output once the device is commanded on (IN = Low → High). For details, refer to the Digital Input Latch section. Unused inputs should be left open or connected to device GND through a 4.7 kΩ resistor.

Table 6. DIGITAL INPUT (IN, CS_EN), AND IDLE_FLG PIN CHARACTERISTICS
($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Low Level Digital Input Voltage	$V_{DIG_IN_L}$				0.8	V
High Level Digital Input Voltage	$V_{DIG_IN_H}$		2			V
Digital Input Voltage Hysteresis	$V_{DIG_IN_HYS}$			0.25		V
Digital Input Current at IN Pin – Input Latch Inactive	I_{IN_LI}	$0.8\ V \le V_{IN} \le 2\ V$, $V_{CS_EN} = 5\ V$			25	μA
Digital Input Current at IN Pin – Input Latch Active	I_{IN_LA}	$V_{IN} = 1.4V$, $V_{CS_EN} = 0\ V$	−25		−1	μA
Digital Input Current at CS_EN Pin	I_{CS_EN}	$0.8\ V \le V_{CS_EN} \le 2\ V$			25	μA
IDLE_FLG Pin Output Voltage Low	V_{IDLE_low}	$I_{IDLE_FLG} = 0.5$ mA		0.2	0.5	V
IDLE_FLG Pin Leakage Current	$I_{IDLE_leakage}$	$V_{IDLE_FLG} = 5\ V$, $V_{IN} = V_{CS_EN} = 0\ V$		0.5	2	μA

Table 7. SWITCHING CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (See Figure 12)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Turn ON Delay – CL Mode (V_{IN} Lo → Hi to V_{OUT} = 10% V_D)	$t_{D_ON_CL}$	$V_D = 13.5\ V$, $R_L = 2\ \Omega$	75	200	400	μs
Turn ON Time – CL Mode (V_{IN} Lo → Hi to V_{OUT} = 90% V_D)	t_{ON_CL}		200	700	1200	μs
Turn ON Delay – Normal Mode (V_{IN} Lo → Hi to V_{OUT} = 10% V_D)	$t_{D_ON_Norm}$		5	20	70	μs
Turn ON Time – Normal Mode (V_{IN} Lo → Hi to V_{OUT} = 90% V_D)	t_{ON_Norm}		35	75	150	μs
Turn OFF Delay (V_{IN} Hi → Lo to V_{OUT} = 90% V_D)	t_{D_OFF}		5	25	70	μs
Turn OFF time (V_{IN} Hi → Lo to V_{OUT} = 10% V_D)	t_{OFF}		30	60	160	μs
Turn ON / OFF Matching – Normal Mode: $t_{ON} - t_{OFF}$	Δt_{ON-OFF}		−40	20	60	μs
Slew Rate ON – CL Mode (V_{OUT} = 30% to 70% V_D)	SR_{ON_CL}		0.015	0.03	0.045	V / μs
Slew Rate ON – Normal Mode (V_{OUT} = 30% to 70% V_D)	SR_{ON_Norm}		0.1	0.3	0.5	V / μs
Slew Rate OFF (V_{OUT} = 70% to 30% V_D)	SR_{OFF}		−0.5	−0.3	−0.1	V / μs
Slew Rate Matching Normal Mode: $SR_{ON_Norm} - SR_{OFF}$	ΔSR		−0.15	0	0.15	V / μs
Turn ON Energy – Normal Mode (Note 11)	W_{ON}	$V_D = 18\ V$, $R_L = 2\ \Omega$, VOUT: 10 % V_D ↔ 90 % V_D		1.5		mJ
Turn OFF Energy– Normal Mode (Note 11)	W_{OFF}			1.5		mJ

11. Not subject to production testing.

Protection

Table 8. PROTECTION CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Over-current Detection (Adjustable) (Note 12)	I_{LIM}	V_D = 13.5 V, R_{AOC} = 4.7 kΩ, Setup based on AECQ100-012 Load Short Circuit	75	85	95	A
		V_D = 13.5 V, R_{AOC} = 30 kΩ, Setup based on AECQ100-012 Load Short Circuit	54	64	73	
		V_D = 13.5 V, R_{AOC} = 20 kΩ, Setup based on AECQ100-012 Load Short Circuit	34	43	51	
		V_D = 13.5 V, R_{AOC} = 10 kΩ, Setup based on AECQ100-012 Load Short Circuit	14	21	29	
Normalized Over-current Detection at High V_{DS} (Note 12)	$I_{LIM(FB)}$	$V_{DS} \ge 17$ V		0.6 x I_{LIM}		A
Normalized Over-current Detection at High V_D for Jump Start (Note 12)	$I_{LIM(JS)}$	$V_D > V_{D_JS}$		0.6 x I_{LIM}		A
Differential Thermal Shutdown Threshold – Normal Mode (Note 12)	T_{DTSD}			80		°C
Differential Thermal Shutdown Threshold – Capacitive Load Mode (Note 12)	T_{DTSD_CL}			30		°C
Max Allowed Time in Capacitive Switching Mode (Note 12)	t_{max_Cap}			50		ms
Thermal Shutdown Threshold (Note 12)	T_{TSD}		150	175	200	°C
Thermal Shutdown Hysteresis (Note 12)	T_{TSD_HYS}			15		°C
Over-Voltage Protection Clamp	V_{ZOV}	Current into the V_D pin, I_D = 5 mA, V_{IN} = 0 V	35	36	40	V
Drain Voltage for Current Limitation Reduction in Jump Start (Note 12)	V_{D_JS}		18.5	20.5	22.5	V

12. Not Subject to production testing.

Table 9. RETRY STRATEGY (See Figure 18)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Number of Retries in Fault after Counter Reset (Notes 13, 14)	n_{COUNT}	$I_{OUT} = I_{LIM}$, or $T_{J(ABS)} > T_{TSD}$, or $T_{J(DIFF)} > T_{DTSD}$, I^2t Monitor = 100%		1		
IN Based Counter Reset Time (Note 13)	$t_{IN(Rst)}$	V_{IN} = 0 V, Fault Counter > 0	40	70	100	ms
CS_EN based Counter Reset Time (Note 13)	$t_{CS_EN(Rst)}$	V_{IN} = 0 V, Fault Counter > 0	150	200	250	μs

13. Not Subject to production testing.
14. Not valid in Capacitive load mode.

Table 10. I^2t PROTECTION THRESHOLDS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I^2t Current Thresholds (Note 15, 16)	I_{I2t_1}	R_{I2t_ADJ} = 4.7 kΩ		0.2 x I_{I2t_9}		A
	I_{I2t_2}			0.25 x I_{I2t_9}		A
	I_{I2t_3}			0.3 x I_{I2t_9}		A
	I_{I2t_4}			0.35 x I_{I2t_9}		A
	I_{I2t_5}			0.4 x I_{I2t_9}		A
	I_{I2t_6}			0.5 x I_{I2t_9}		A
	I_{I2t_7}			0.6 x I_{I2t_9}		A
	I_{I2t_8}			0.8 x I_{I2t_9}		A
	I_{I2t_9}		75	85	95	A
	I_{I2t_9}	R_{I2t_ADJ} = 30 kΩ	54	64	73	A
	I_{I2t_9}	R_{I2t_ADJ} = 20 kΩ	34	43	51	A
	I_{I2t_9}	R_{I2t_ADJ} = 10 kΩ	14	21	29	A

15. Not Subject to production testing.
16. R_{AOC} = 4.7 kΩ to ensure full I^2t range.

Table 11. I^2t PROTECTION TIMERS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I^2t Time Control (Notes 17, 18)	t_{I2t_1}	$I_{OUT} = I_{I2t_1}$		20		s
	t_{I2t_2}	$I_{OUT} = I_{I2t_2}$		4		s
	t_{I2t_3}	$I_{OUT} = I_{I2t_3}$		1		s
	t_{I2t_4}	$I_{OUT} = I_{I2t_4}$		0.52		s
	t_{I2t_5}	$I_{OUT} = I_{I2t_5}$		0.3		s
	t_{I2t_6}	$I_{OUT} = I_{I2t_6}$		0.18		s
	t_{I2t_7}	$I_{OUT} = I_{I2t_7}$		0.11		s
	t_{I2t_8}	$I_{OUT} = I_{I2t_8}$		0.05		s
I^2t Time Control Accuracy (Note 17)	t_{I2t_acc}		−15		15	%

17. Not Subject to production testing.
18. R_{AOC} = 4.7 kΩ to ensure full I^2t range.

Diagnostic Functions

NCV84003G provides diagnostic information and dynamic current sensing on the diagnostic output pin CS. The below table describes the standard behavior of the CS output, assuming a CS readback sequence has not been initiated as detailed in the Configuration and Status Readback with Intelligent Current Sense section.

Table 12. DIAGNOSTIC TRUTH TABLE

Operating Condition	IN	CS_EN	IDLE MODE	Output Voltage	CS Output
Normal Operation	L	H	X	~ GND	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Short Circuit to GND – Overcurrent				GND	HiZ, if Fault Counter = 0 $I_{CS_FAULT_ILIM}$ if Fault Counter > 0
Over Temperature				~ GND	HiZ, if Fault Counter = 0 $I_{CS_FAULT_TSD}$ if Fault Counter > 0
Short Circuit to V_{BATT}				V_{BATT}	$I_{CS_FAULT_OSOL}$, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Open Load				< V_D – V_{DS_OSOL}	HiZ, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
				> V_D – V_{DS_OSOL}	$I_{CS_FAULT_OSOL}$, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Inverse Current				> V_D	$I_{CS_FAULT_OSOL}$, if Fault Counter = 0 I_{CS_FAULT} if Fault Counter > 0
Normal Operation	H		Disabled	~ V_D	$I_{CS} = I_{OUT} / K_{NOM}$
			Enabled		$I_{CS} = I_{OUT} / K_{NOM}$ if $I_{OUT} > I_{IDLE_TF}$, HiZ if $I_{OUT} \le I_{IDLE_TF}$
Short Circuit to GND – Over Current Detection			X	~ GND	$I_{CS_FAULT_ILIM}$
Over Temperature (Absolute or Differential)			X	~ GND	$I_{CS_FAULT_TSD}$
Short Circuit to V_{BATT}			Disabled	V_{BATT}	$I_{CS} < I_{OUT} / K_{NOM}$
			Enabled	V_{BATT}	HiZ
Open Load			Disabled	~ V_D	$I_{CS} \le I_{CS(OL)}$
			Enabled	~ V_D	HiZ
Underload			Disabled	~ V_D	$I_{CS(OL)} < I_{CS} < I_{OUT} / K_{NOM}$
			Enabled	~ V_D	HiZ
Inverse Current			X	> V_D	HiZ
Diagnostics Disabled	X	L	X	X	HiZ

Current Sense Ratio K

The accuracy in load current estimation through sensed current can be improved by performing a calibration routine during end of line (EOL) testing. The calibration procedure can be performed at the nominal load current at one single temperature (25 °C).

Diagnostics

Table 13. CURRENT SENSE CHARACTERISTICS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
CS Leakage Current, CS Output Disabled	$I_{Q_CS_DIS}$	V_{IN} = 5 V, V_{CS_EN} = 0 V, I_L = 15 A			0.5	μA
CS Leakage Current, CS Output Enabled	$I_{Q_CS_EN}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I_L = 0 A			1	μA
CS Operation Voltage for Nominal Operation (Note 19)	$V_{CS_SAT(NOM)}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, I_L = 15 A, I_{CS} > 0.5 x I_{CS_NOM}	0	0.5	1	V
CS Operation Voltage for In-fault Operation (Note 19)	$V_{CS_SAT(Fault)_ILIM}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, I_{CS} > 0.5 x $I_{CS_Fault_ILIM}$	0	0.5	1	V
CS Operation Voltage for In-fault Operation (Note 19)	$V_{CS_SAT(Fault)_TSD}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, I_{CS} > 0.5 x $I_{CS_Fault_TSD}$	0	0.5	1	V
CS Operation Voltage for In-fault Operation (Note 19)	$V_{CS_SAT(Fault)_I2t}$	V_D = 6 V, V_{IN} = V_{CS_EN} = 5 V, I_{CS} > 0.5 x $I_{CS_Fault_I2t}$	0	0.5	1	V
CS Operation Voltage for OFF State Open Load Operation (Note 19)	$V_{CS_SAT(Fault)_OSOL}$	V_D = 6 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, I_L = 0 A, I_{CS} > 0.5 x $I_{CS_Fault_OSOL}$	0	0.5	1	V
CS Saturation Current in Normal Mode (Note 19)	I_{CS_SAT}		8	10		mA
CS Fault Indication Current: Overcurrent Detection (Note 19)	$I_{CS_FAULT_ILIM}$	V_{IN} = 5 V, V_{CS_EN} = 5 V Fault Counter > 0, I_{OUT} = I_{LIM}	6.7	8.5	10	mA
CS Fault Indication Current: TSD/DTSD (Note 19)	$I_{CS_FAULT_TSD}$	V_{IN} = 5 V, V_{CS_EN} = 5 V Fault Counter > 0, T_J > T_{TSD} or $T_{J(DIFF)}$ > T_{DTSD}	3.8	5	6.5	mA
CS Fault Indication Current: I^2t Activation (Note 19)	$I_{CS_FAULT_I2t}$	V_{IN} = 5 V, V_{CS_EN} = 5 V Fault Counter > 0, I^2t Monitor = 100%	1	1.5	1.8	mA
CS Fault Indication Current in OFF State Open Load	$I_{CS_FAULT_OSOL}$	V_{IN} = 0 V, V_{CS_EN} = 5 V Fault Counter = 0, V_{DS} < V_{DS_OSOL}	1.9	2.5	3.5	mA
CS Pin Clamp to Power Supply	V_{CS_CL}	I_{CS} = 1 mA	35	36	40	V
Current Sense Ratio 1	K_1	I_{OUT} = 0.5 A	17025	22700	28375	
Current Sense Ratio 2	K_2	I_{OUT} = 0.75 A	19295	22700	26105	
Current Sense Ratio 3	K_3	I_{OUT} = 2 A	20430	22700	24970	
Current Sense Ratio 4	K_4	I_{OUT} = 8.5 A	21565	22700	23835	
Current Sense Ratio 5	K_5	I_{OUT} = 15 A	21792	22700	23608	
Max Current Sense Ratio Drift After Two-Point Calibration (Note 20)	K_{rel4}	K_4 / K_5, including temperature drift	0.97	1	1.03	

19. Not Subject to production testing.
20. Not subjected to production testing. For more information, refer to the AND9733/D Applications Note.

Table 14. CURRENT SENSE TIMING ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (See Figure 31)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Current Sense Settling Time after Diagnostic Activation, Stable Output and Load Conditions – Nominal Load (Note 21)	$t_{S_CS_ENH}$	V_{IN} = 5 V, V_{CS_EN} = 0 V → 5 V V_D = 13.5 V, I_L = 15 A, I_{CS} = 90% I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			30	µs
Current Sense Settling Time after Diagnostic Activation, Stable Output and Load Conditions – Light Load (Note 21)	$t_{S_CS_ENL}$	V_{IN} = 5 V, V_{CS_EN} = 0 V → 5 V V_D = 13.5 V, V_{IDLE_FLG} = 0 V, I_L = 0.75 A, I_{CS} = 90 % I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			60	µs
Current Sense Settling Time after Load Current Change (Note 21)	$t_{S_CS_LOAD_U}$	V_{IN} = V_{CS_EN} = 5 V, V_D = 13.5 V I_L = 8.5 A → 15 A, I_{CS} = 90 % I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Current Sense Output Disable Time (Note 21)	$t_{S_CS_DIS}$	V_{IN} = 5 V, V_{CS_EN} = 5 V → 0 V V_D = 13.5 V, I_L = 15A, I_{CS} = 10% I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Current Sense Output Disable Time – In Fault (Note 21)	$t_{S_CS_DIS_F}$	V_{IN} = 0 V, V_{CS_EN} = 5 V → 0 V V_D = V_{OUT} = 13.5 V, I_{CS} = 10% I_{CS_STATIC} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF			20	µs
Standby Mode Activation after Diagnostic Activation (Note 21)	t_{Norm}	V_{CS_EN} = 0 V → 5 V to V_{IN} = 0 V → 5 V for normal mode entry (See Figure 12)	200			µs

21. Not Subject to production testing.

Table 15. CS STATUS AND CONFIGURATION READBACK TIMING ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (See Figure 31)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Current Sense Enable Pulse Width for Configuration Readback (Note 22)	$t_{CS_EN(CR)}$	V_{IN} = 0 V, V_{CS_EN} = 0 V → 5 V to 5 V → 0 V (See Figure 33)	480	600	750	µs
Current Sense Output Configuration Readback Blank Time (Note 22)	t_{CR_Blank}	V_{IN} = 0 V, V_{CS_EN} = 5 V (See Figure 33)	480	600	750	µs
Current Sense Output Configuration Readback Time (Note 22)	t_{CS_Rd}	V_{IN} = 0 V, V_{CS_EN} = 5 V (See Figure 33)	480	600	750	µs

22. Not Subject to production testing.

Table 16. CS CONFIGURATION READBACK ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (See Figure 31)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
CS Current in Configuration Readback – Overcurrent Detection – 100% Setting (Note 23)	$I_{CS_CR_OC_100\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	4.25	5	6.0	mA
CS Current in Configuration Readback – Overcurrent Detection – 75% Setting (Note 23)	$I_{CS_CR_OC_75\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	3.1	3.75	4.7	mA
CS Current in Configuration Readback – Overcurrent Detection – 50% Setting (Note 23)	$I_{CS_CR_OC_50\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	2.0	2.5	3.2	mA
CS Current in Configuration Readback – Overcurrent Detection – 25% Setting (Note 23)	$I_{CS_CR_OC_25\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	1.0	1.25	1.6	mA
CS Current in Configuration Readback – I^2t Detection – 100% Setting (Note 23)	$I_{CS_CR_I2t_100\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	4.25	5.0	6.0	mA
CS Current in Configuration Readback – I^2t Detection – 75% Setting (Note 23)	$I_{CS_CR_I2t_75\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	3.1	3.75	4.7	mA
CS Current in Configuration Readback – I^2t Detection – 50% Setting (Note 23)	$I_{CS_CR_I2t_50\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	2.0	2.5	3.2	mA
CS Current in Configuration Readback – I^2t Detection – 25% Setting (Note 23)	$I_{CS_CR_I2t_25\%}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	1.0	1.25	1.6	mA
Current Sense Verification Current (Note 23)	$I_{CS(Ver)}$	V_D = 13.5 V, V_{IN} = 0 V, V_{CS_EN} = 5 V, T_a = 25 °C, See Figure 34	0.4	0.5	0.6	mA

23. Not Subject to production testing.

Table 17. I^2t STATUS READBACK LEVELS ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified) (See Figure 31)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
CS Current in Status Readback – 10% Status (Note 24)	$I_{CS_SR_10\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 0%–10%	0.4	0.5	0.6	mA
CS Current in Status Readback – 20% Status (Note 24)	$I_{CS_SR_20\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 10%–20%	0.8	1	1.2	mA
CS Current in Status Readback – 30% Status (Note 24)	$I_{CS_SR_30\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 20%–30%	1.2	1.5	1.8	mA
CS Current in Status Readback – 40% Status (Note 24)	$I_{CS_SR_40\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 30%–40%	1.6	2	2.4	mA
CS Current in Status Readback – 50% Status (Note 24)	$I_{CS_SR_50\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 40%–50%	2	2.5	3	mA
CS Current in Status Readback – 60% Status (Note 24)	$I_{CS_SR_60\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 50%–60%	2.4	3	3.6	mA
CS Current in Status Readback – 70% Status (Note 24)	$I_{CS_SR_70\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 60%–70%	2.8	3.5	4.2	mA
CS Current in Status Readback – 80% Status (Note 24)	$I_{CS_SR_80\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 70%–80%	3.2	4	4.8	mA
CS Current in Status Readback – 90% Status (Note 24)	$I_{CS_SR_90\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 80%–90%	3.6	4.5	5.4	mA
CS Current in Status Readback – 100% Status (Note 24)	$I_{CS_SR_100\%}$	V_{IN} = 5 V, V_{CS_EN} = 5 V, I^2t Monitor: 90%–100%	4	5	6	mA

24. Not Subject to production testing.

Table 18. OPEN LOAD / UNDERLOAD DETECTION AND TIMING
($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Open Load Detection Threshold, OFF State (Note 25)	V_{DS_OSOL}	V_{IN} = 0 V, V_{CS_EN} = 5 V	1.1	1.8	2.5	V
Open Load Detection Delay OFF State	t_{OSOL_Blank}	V_{IN} = 5 V → 0 V, V_{CS_EN} = 5 V $V_D = V_{OUT}$ = 13.5 V, I_{CS} = 90% I_{CS_FAULT} R_{CS} = 1.2 kΩ, C_{CS} < 100 pF	70	150	250	μs
Open Load Detection Threshold, ON State (IDLE Mode Disabled) (Note 26)	I_{OL_ON}	V_{IN} = 5 V, V_{CS_EN} = 5 V $I_{CS} = I_{CS(OL)}$ = 4 μA	30		275	mA

25. Not subject to production testing.
26. Limits may be widened.

Table 19. IDLE MODE DETECTION AND TIMING ($6 \le V_D \le 18$ V; -40 °C $\le T_J \le 150$ °C unless otherwise specified)

Parameter Characteristic	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
IDLE Mode Exit Detection Delay	t_{IDLE_Ext}	V_{IN} = 5 V, I_{OUT} = 0.5 A → 15 A to V_{IDLE_FLG} = 10% max V_{IDLE_FLG}		15		μs
IDLE Mode Entry Detection Delay	t_{IDLE_Ent}	V_{IN} = 5 V, I_{OUT} = 15 A → 0.5 A to V_{IDLE_FLG} = 90% max V_{IDLE_FLG}, I^2t Monitor = 0%		250		μs
IDLE Mode Entry Blanking Time	t_{IDLE_Blk}	V_{IN} = 0 → 5V, V_{CS_EN} = 5 V, I_{OUT} = 0.5 A V_{IDLE_FLG} = 90% max V_{IDLE_FLG}		350		μs

Application Diagram and Pin Description

NCV84003G is a single channel smart high-side driver with a very low resistance n-channel output transistor. The required gate overdrive voltage for the transistor is generated by a charge pump that is integrated into the device. The output driver's protection scheme is designed to support linear resistive loads as well as loads with high inrush current, e.g. bulk capacitors and lighting bulbs. The embedded control and protection functions provide full protection to the device as well as full-featured load diagnostic for open load, underload and short circuit through a current sense output that delivers a fraction of the load current in nominal operation multiplexed with a fixed current output in a fault state. An accurate slew rate control is provided to minimize conducted EMI in case of a constant PWM operation. The device features an ultra-low operating current in IDLE mode to address system leakage requirements in zonal applications.

The device provides direct control input (IN) and a diagnostic enable input (CS_EN) to control the information to be provided at the current sense output.

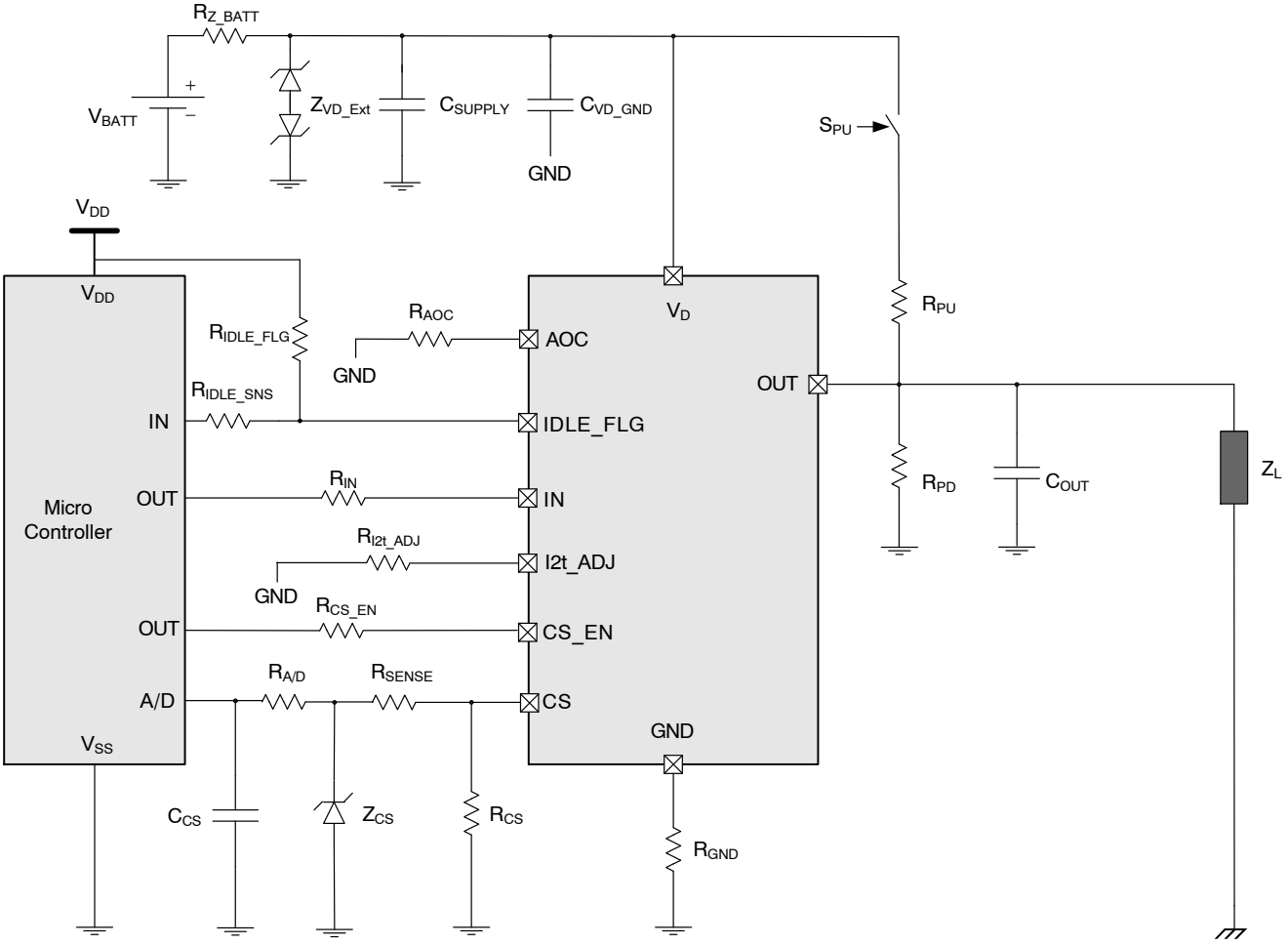


Figure 4. Application Diagram

NCV84003G is supplied by the V_D pin, which can be directly connected to the battery net. The V_D pin is used as power supply to the control circuitry as well as the common drain supply for output channels. In order to support all board net transients following ISO7637-1, an external protection concept as shown in Figure 4 is recommended.

The zener diode Z_{VD_Ext} is used to clamp overvoltage events as well as to provide a free-wheeling path in the event of loss of battery (V_D) with charged inductive loads. R_{GND} is required to limit the maximum current flowing through Z_{VD} (see Figure 20) in case of an over-voltage event. Since all low-voltage I/O pins feature input protection diodes, it is required to insert series resistances into the connection lines between the controlling device (e.g. microcontroller) and NCV84003G.

Table 20. RECOMMENDED EXTERNAL COMPONENTS

Reference	Value	Function
R_{IN}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{CS_EN}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{I2t_ADJ}	4.7 kΩ ~ 30 kΩ	Recommended range for selecting I^2t. Open circuit and short to GND not recommended (Refer Overcurrent Shutdown).
R_{IDLE_FLG}	10 kΩ	Open drain resistor to logic level voltage.
R_{IDLE_SNS}	4.7 kΩ	Provides protection of the micro controller during overvoltage and reverse polarity. Ensures the channel is OFF during loss of GND.
R_{AOC}	4.7 kΩ ~ 30 kΩ	Recommended range for selecting overcurrent threshold. Open circuit and short to GND not recommended (Refer Overcurrent Shutdown).
R_{CS}	1.2 kΩ	Current Sense resistor.
R_{SENSE}	4.7 kΩ	Provides protection against overvoltage, reverse polarity, and loss of GND. The value of this resistor should be selected with the micro controller specification.
C_{CS}	100 pF	Current Sense signal filtering.
$R_{A/D}$	4.7 kΩ	Current Sense signal filtering.
Z_{CS}	10 V Zener Diode	Provides protection micro controller during overvoltage at CS. Should be selected with the micro controller specification.
R_{PU}	1.5 kΩ	Polarizes the NCV84003G output during OFF state open load diagnosis.
R_{PD}	47 kΩ	Output polarization. Improves the NCV84003G immunity to electromagnetic noise and also used for short to V_{BATT} detection.
S_{PU}	BC807	Switches the battery voltage for OFF state open load diagnostic.
R_{GND}	47 Ω	Provides protection during overvoltage.
Z_{VD_Ext}	30 V Zener Diode	Provides protection of the device during overvoltage.
C_{SUPPLY}	100 nF	Filtering of voltage spikes on the battery line.
C_{VD_GND}	47 nF	Provides drain voltage stability during fast transients such as overload.
C_{OUT}	10 nF	Protection during ESD and BCI on output.

Modes of Operation

NCV84003G is designed to operate in the following distinct modes of operation as stated below. Irrespective of the modes below, it should be noted that if $V_D < V_{D(UV)}$, then the internal logic may be reset to default, and values of timers/counters cannot be guaranteed.

a. Sleep Mode

If IN and CS_EN have been observed as low for a duration longer than $t_{IN(Rst)}$ and I^2t Monitor is zero, then the device enters sleep mode. The output FET is off, and the internal reference blocks are shut down and digital logic is reset (as in case of supply-based reset) in this mode to offer extremely low quiescent current (Refer Table 4).

b. Standby Mode

If IN has been observed low for a duration more than $t_{IN(Rst)}$ and CS_EN is high then device operates in standby mode. The output FET is off, and the off state diagnosis for open load and short circuit to V_{BATT} are available and I^2t monitor is active in this mode. A device configuration readback, if desired, can be requested in standby mode as described in the Configuration and Status Readback with Intelligent Current Sense section. If CS_EN continues to be high, device stays in standby mode.

c. Capacitive Load (CL) Mode

If IN is set to high, the output stage is powered on, and device enters normal or CL mode of operation depending on the state prior to turn on. In case of turn on (IN = Lo → Hi) from sleep mode, the device automatically transitions into CL (capacitive load) mode where the turn on slew rate is reduced and corresponding turn on time is increased. This allows for a delayed turn on profile to charge any capacitive loads connected to the output of the device. The retry strategy and protection features are tailored to charge a capacitive load as described in section *Capacitive Load Switching*. Further, the exit conditions from CL mode are also described in this section. In case of PWM operation, device stays in CL mode unless one of the exit conditions is met. PWM frequency and duty cycle should be set externally to ensure that load is

sufficiently charged in required time. If CS_EN stays low during CL Mode, then driving the output stage while keeping IN = Hi-Z is allowed (refer to Digital Input Latch section). If CS_EN is set to High, then diagnosis is available in CL mode. Further, I^2t status readback (refer to the Configuration and Status Readback with Intelligent Current Sense section) is also available in CL Mode.

d. Normal Mode

Once the capacitive load is fully charged, the device transitions to normal mode. The turn on timing and slew in this mode are designed to support faster switching operation. The current sense pin outputs a current proportional to the load current if CS_EN is set to high. In case the capacitive load switching is not required in the application, it is recommended to switch on CS_EN before asserting the input Lo → Hi from sleep. This ensures that device enters normal mode once input is enabled. The minimum time between CS_EN: Lo → Hi and IN: Lo → Hi should be more than $t_{Norm.}$ for the output stage to turn on in normal mode. If already in CL mode, the normal mode can still be entered by meeting one of the exit conditions described in *Capacitive Load Switching* mode. Similar to the CL mode, device can be driven in PWM operation in normal mode along with the capability of driving the output stage high while keeping IN = Hi-Z is allowed (refer to Digital Input Latch section). Further, I^2t status readout is provided in this mode (refer to the Configuration and Status Readback with Intelligent Current Sense section). If IN and CS_EN are both asserted low for a period greater than $t_{IN(Rst)}$ and I^2t monitor equals zero, then device enters sleep mode.

e. Protect Mode

While operating in normal mode, the device may observe either of the fault conditions described in Protection Features, that trigger protect mode and lead to latching-off of the output stage. A fault current output on the CS pin will be provided if CS_EN is enabled. The reset conditions for the fault counter are described in section ON State Fault Retry Strategy. If any of the reset conditions are met, device exits protect mode. Any configuration or status readback request is not allowed in Protect Mode. Further, ON state fault takes precedence over Off State Open Load (OSOL) as well as status readout if fault counter is greater than zero.

f. IDLE mode

A dedicated IDLE mode has been designed in NCV84003G for applications that require reduced operating current while the output stage is turned on (at relatively small output current levels) over extended periods. These applications may, for example, involve the SmartFET providing power to electronic modules that require a software routine to be executed while the car is parked. In such case, limiting the operating current is very critical to reduce the current consumption of the automotive system. The open drain IDLE_FLG pin allows the microcontroller to control the IDLE functionality as explained below.

If IDLE mode is desired in an application, IDLE_FLG pin needs to be supplied with logic level voltage with a pull-up resistor. As the internal logic is activated from sleep mode (by asserting either/both IN/CS_EN high), it executes an internal routine to sense the voltage referenced at this pin. If the sensed voltage is greater than the threshold described in Table 6, then IDLE mode detection is enabled. This routine is associated with a blanking time, per Table 14, during which, a decision to enable IDLE functionality is still being determined.

Once the blanking time has elapsed and IDLE functionality is enabled, NCV84003G automatically detects an entry into IDLE mode by sensing the level of output current. Current thresholds for IDLE mode entry and exit are defined in Table 5. If the output current falls below I_{IDLE_TF} while IN = Hi, then device enters IDLE mode. The R_{ON} of the output stage in this mode is higher than normal mode R_{ON} (Refer Table 5) while conducting extremely low operating current out of the GND pin (Refer Table 4). Protection mechanisms in the form of overcurrent, undervoltage and thermal shutdown are not available during operation in this mode. In addition, the current sense output, diagnosis and readback requests are turned off. The CS_EN input is recommended to be asserted low in this mode to limit the operating current. If IN observes a high-impedance state at any point after turn-on (IN = Low → High), an entry into and exit from IDLE Mode is still allowed (refer to Digital Input Latch section). Such an operation allows the microcontroller to switch off its logic outputs to reduce the overall system current consumption.

If the IDLE_FLG pin is connected to GND (via a resistor), then IDLE functionality is disabled, and device continues to operate in normal mode even if load transitions to current levels below I_{IDLE_TF} while IN = High. Current sense output and protection features also operate as usual in such case. This implementation lets the application microcontroller to decide if IDLE functionality should be present or not by controlling the reference supply to IDLE_FLG pin. It should be noted that the internal routine for activating IDLE mode detection is only performed once at exit from sleep mode, or in case of digital logic reset because of supply POR, i.e., the reference supply at IDLE_FLG pin will not be continuously sensed for in normal operation. Therefore, for applications that do require IDLE mode functionality, this pin should always be supplied with logic voltage before attempting to switch on the output or activate any diagnostics.

Further, an entry into IDLE mode is prohibited – a) in CL mode, or, b) if I^2t monitor is greater than zero, or c) if the sensed current is low because of a fault counter being latched in case of an ON-State fault (Refer ON State Fault Retry Strategy). For example, if $I_{OUT} < I_{IDLE_TF}$ as the output stage is turned on from sleep into CL mode, the decision to enter IDLE mode will not be made until the IDLE blanking time (as defined above) has elapsed and the device has transitioned to normal mode. In typical cases, this time is at-least $t_{ON_CL} + t_{IDLE_Ent}$, where t_{IDLE_Ent} is the transition time to IDLE mode from normal mode (note that IDLE blank routine executes in parallel with the output stage turn on).

The IDLE_FLG pin serves a dual purpose by also indicating the status of the IDLE mode in the application. If the IDLE mode functionality is enabled and the output current reduces below I_{IDLE_TF}, then open drain IDLE_FLG output observes a logic high voltage to indicate operation in IDLE mode, and vice versa. The state of this pin should be disregarded during the IDLE blanking time during which IDLE functionality is being sensed for.

While operating in IDLE mode, if the output current increases above I_{IDLE_TR}, such as in case of overload, short circuit to GND or normal load activation, then device exits into Normal mode and all the protection features are enabled. The voltage at IDLE_FLG pin is asserted low indicating an entry into normal mode. The response time for the device to enter normal mode is described in Table 7. When in Idle mode, it is recommended to operate the device within the nominal supply voltage range (Refer Table 4) to prevent overstress in case of a potential short circuit, if applied. Further, the output load ramp must be limited to 5 A/μs for load and terminal short circuits per AECQ100-012.

If the input is asserted high → low during operation in IDLE mode to switch off the output stage, then the device directly enters the sleep mode. In addition while utilizing the digital input latch feature, if CS_EN is asserted high at any time during IDLE Mode operation, the input latch is disengaged and the state of the IN pin will determine the subsequent mode of operation.

Besides the dependence on load level, supply voltage at the drain pin is also a determinant of transitions to and from IDLE mode. If the device is operating in IDLE mode and the supply voltage drops below $V_{D_IDLE_Ext}$ (Refer Table 4), then device safely exits IDLE mode into normal mode and re-engages the internal logic & control. Such a transition allows the device to keep the output stage ON and loads powered at extremely low supply voltages using high precision normal mode bandgap and circuits. It also allows to safely shut down the output stage in normal mode if the supply voltage drops further down and below the undervoltage threshold – V_{D_UV}. While enabling the low voltage operation, this transition to normal mode will cause the operating current to increase above I_{GND_IDLE} (Refer Table 4). Therefore, when operating the device in IDLE mode, the supply level should be greater than $V_{D_IDLE_Ext}$ to ensure desired performance with reduced operating current. In case of fast downward supply transitions in IDLE mode, a POR threshold – $V_{D_IDLE_POR}$ (Refer Table 4) has been designed to ensure that device is switched off immediately to avoid inadvertent response at low battery voltages.

Further, while operating in normal mode, an entry into IDLE mode is prohibited if the battery voltage drops below $V_{D_IDLE_Block_F}$ (even if $I_{OUT} < I_{IDLE_TF}$). In such case, the device continues to operate in normal mode. In other words, while utilizing the auto-entry feature into IDLE mode with load reduction, the supply voltage levels must be ensured to be above $V_{D_IDLE_Block_F}$ (Refer Table 4). Similarly, if the supply voltage is ramping up in normal mode, an entry into IDLE mode will only be allowed if $V_D > V_{D_IDLE_Allow_R.}$ (Refer Table 4) provided that all other conditions for IDLE entry are met as described above. These thresholds are designed to avoid continual mode transitions (between normal and IDLE modes) at low battery voltage, especially in case of noisy supply profiles. The voltage transitions are covered in more detail in Undervoltage Protection section.

Finally, the current thresholds for IDLE mode are designed considering the load levels and device capability under nominal conditions. In case it is expected for the device to observe normal mode operation at reduced loads ($I < I_{IDLE_TF}$), it is recommended to disable IDLE functionality via IDLE_FLG pin as described above. For instance, operating at high ambient temperatures with higher conduction losses in IDLE mode (than in normal mode) along with the absence of a thermal shutdown may overstress the device and IDLE mode should be disabled externally if such operation is desired.

The following timing diagram depicts the transitions in and out of IDLE mode and the block diagram in Figure 6 describes IDLE operation internal to the device.

The flowchart in Figure 8 summarizes the sequence of operations associated with IDLE functionality.

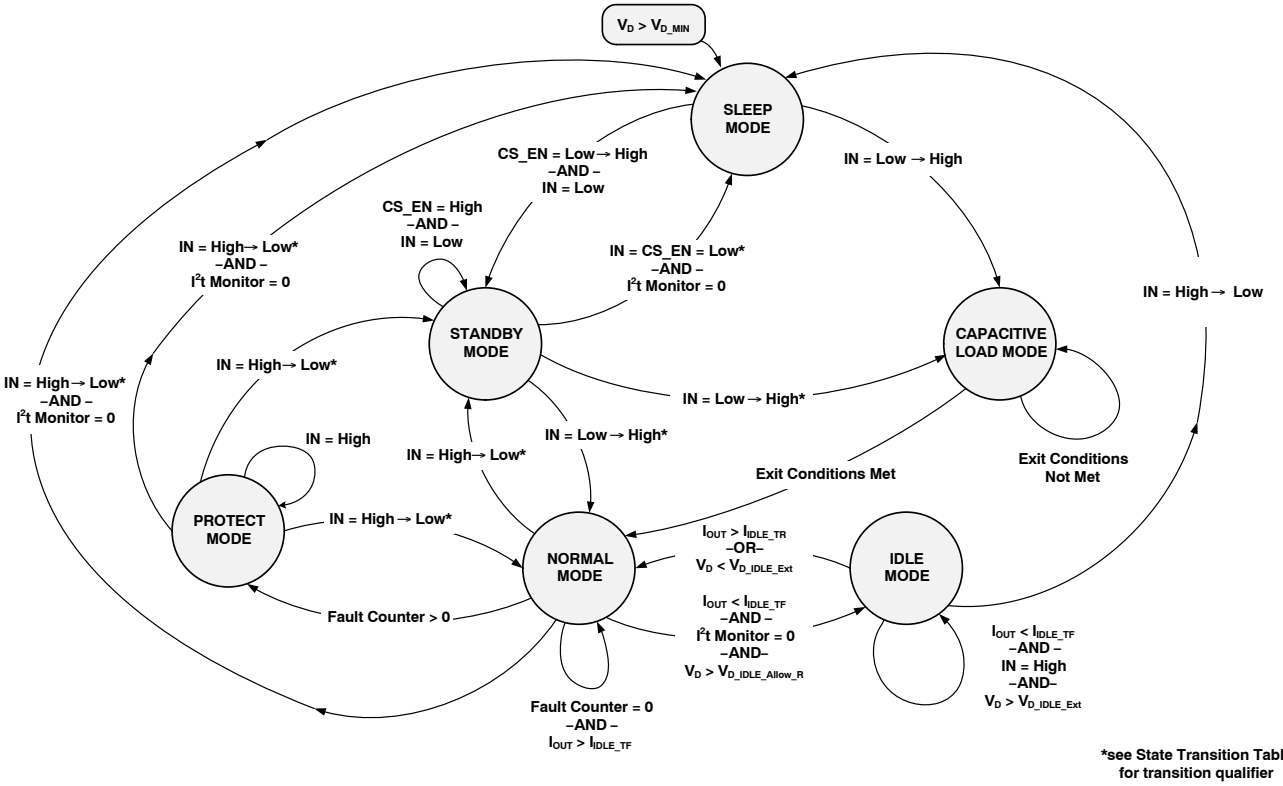


Figure 5. NCV84003G Operation Modes and Transitions

Table 21. STATE TRANSITION TABLE

Present State	Target State	Transition Criteria	Transition Qualifier
UNPOWERED	SLEEP MODE	$V_D > V_{D_MIN}$	–
SLEEP MODE	CAPACITIVE LOAD MODE	IN = Low → High	–
SLEEP MODE	STANDBY MODE	CS_EN = Low → High – AND – IN = Low	–
NORMAL MODE	IDLE MODE	$I_{OUT} < I_{IDLE_TF}$ –AND– $V_D > V_{D_IDLE_Allow_R}$	I^2t Monitor = 0
NORMAL MODE	PROTECT MODE	Fault Counter > 0	–
NORMAL MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired
NORMAL MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$ – AND – I^2t Monitor = 0
STANDBY MODE	NORMAL MODE	IN = Low → High	$t > t_{Norm}$
STANDBY MODE	SLEEP MODE	IN = CS_EN = Low	$t_{IN(Rst)}$ Expired – AND – I^2t Monitor = 0
STANDBY MODE	CAPACITIVE LOAD MODE	IN = Low → High	$t < t_{Norm}$
IDLE MODE	SLEEP MODE	IN = High → Low	–
IDLE MODE	NORMAL MODE	$I_{OUT} > I_{IDLE_TR}$ –OR– $V_D < V_{D_IDLE_Ext}$	–

Table 21. STATE TRANSITION TABLE (continued)

Present State	Target State	Transition Criteria	Transition Qualifier
PROTECT MODE	STANDBY MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = High/CS_EN = Low for $t < t_{IN(Rst)}$
PROTECT MODE	SLEEP MODE	IN = High → Low	$t_{IN(Rst)}$ Expired – AND – CS_EN = Low over $t_{IN(Rst)}$ – AND – I^2t Monitor = 0
PROTECT MODE	NORMAL MODE	IN = High → Low	$t_{IN(Rst)}$ Not Expired – AND – $t_{CS_EN(Rst)}$ Expired
CAPACITIVE LOAD MODE	NORMAL MODE	Exit Conditions Met (Note 27)	–

27. Refer to section Resistive and Capacitive Load Switching Characteristics.

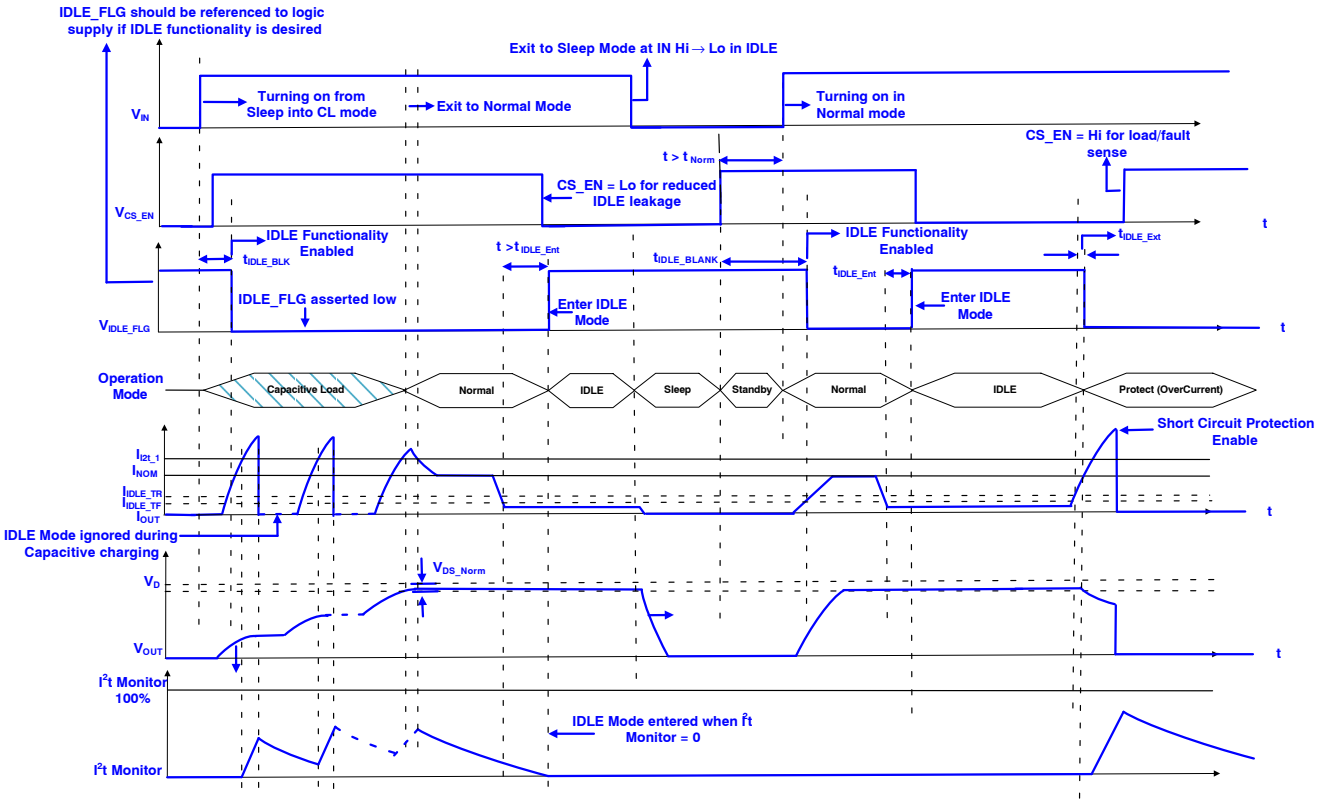


Figure 6. IDLE Mode Timing Diagram

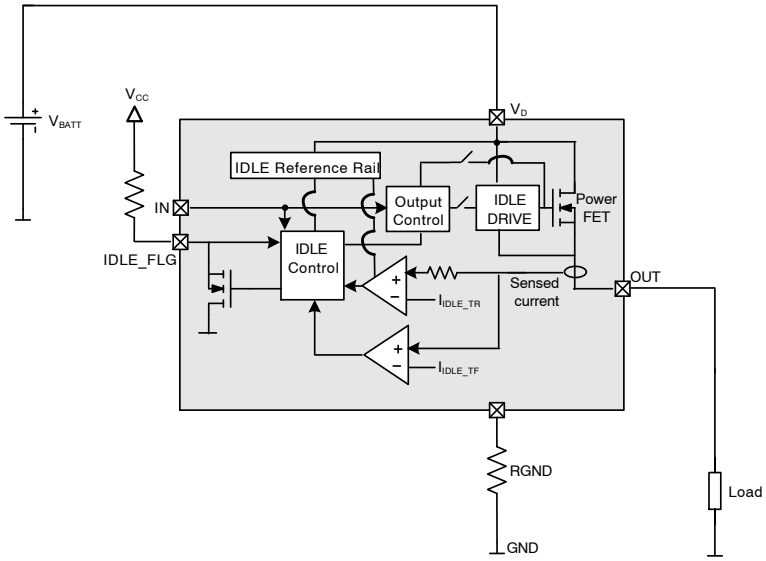


Figure 7. IDLE Mode Operational Block Diagram

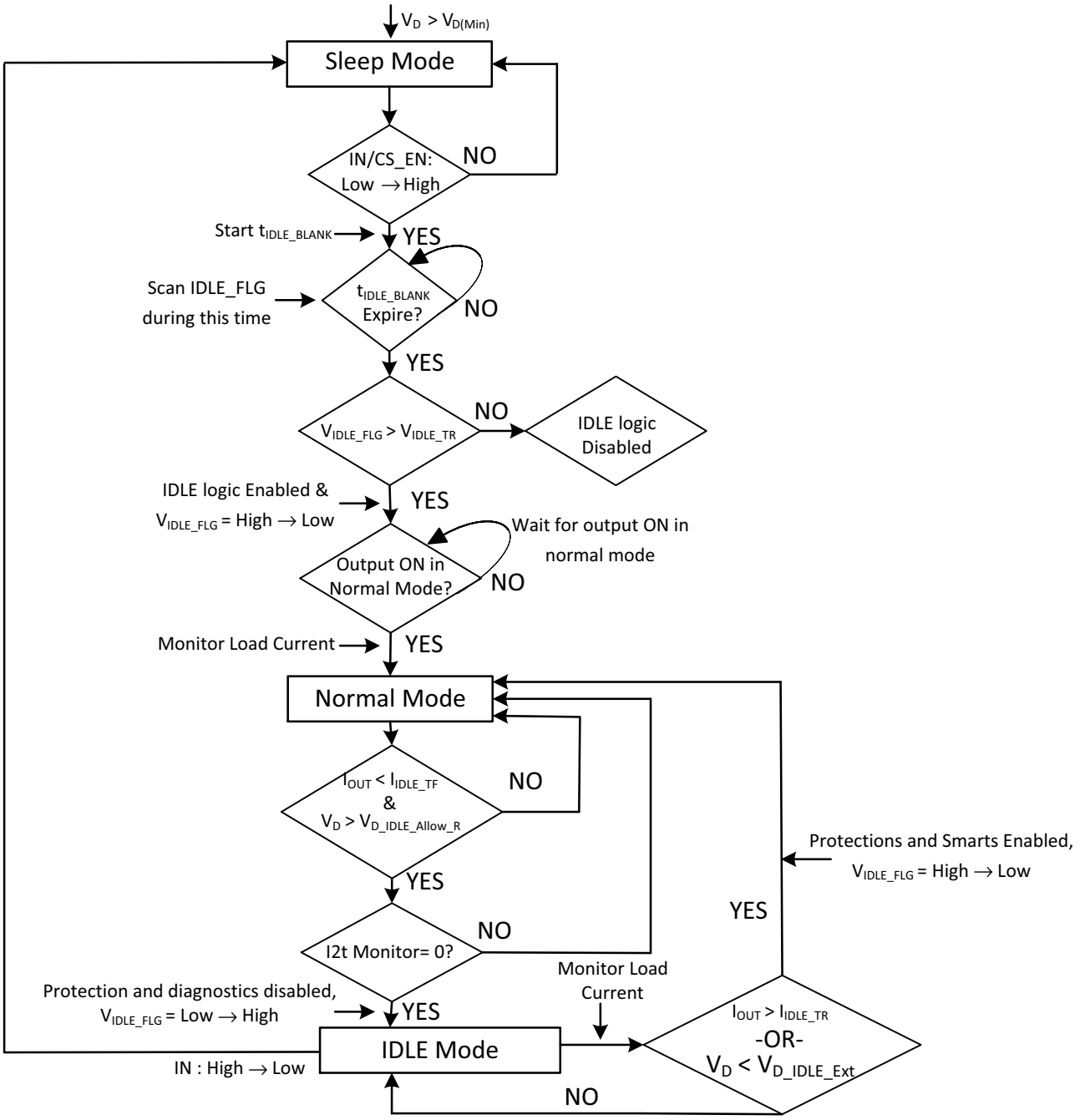


Figure 8. NCV84003G IDLE Mode Flowchart

Digital Input Latch

The control inputs in NCV84003G – namely IN and CS_EN are compatible with 5 V and 3.3 V microcontroller logic levels as described in Table 6. Each input is interfaced to a logic buffer and hysteresis control internally to avoid undesired transitions (because of any coupled noise) around the thresholds. To provide an unambiguous command to the device, the logic inputs should be sufficiently above and below the High and Low logic levels as described in Table 6. In addition to the two logic levels, the control input IN is also allowed to be set to a high-impedance (Hi-Z) state under certain conditions described below.

For applications that require an overall reduced current consumption including that through the microcontroller, providing an output control with IN as High-Z allows the microcontroller to disengage its logic output driving the IN pin and thereby, reduce system leakage. Particularly, in operations such as IDLE mode, where output stage is desired to be ON with minimal current consumption, this feature becomes crucial in reducing the leakage budget in the application.

The feature is implemented in the form of an intelligent latch at the IN pin that maintains the prior state of the IN signal provided:

a. CS_EN is observed low.
b. IN pin is not actively transitioned by the microcontroller.

If any of the two conditions are violated, then the internal pull-up reference current source at IN pin (as depicted in Figure 9) is deactivated and the current state of IN pin determines the mode of operation. It should also be noted that IN pin is interfaced with an active internal pull-down circuit that ensures IN maintains a low state in case this signal is externally driven Hi-Z and the pull-up reference is not active. Such an implementation ensures a high level of functional safety in the application, especially in cases where connection to IN pin is lost.

The block diagram below depicts the implementation of this feature.

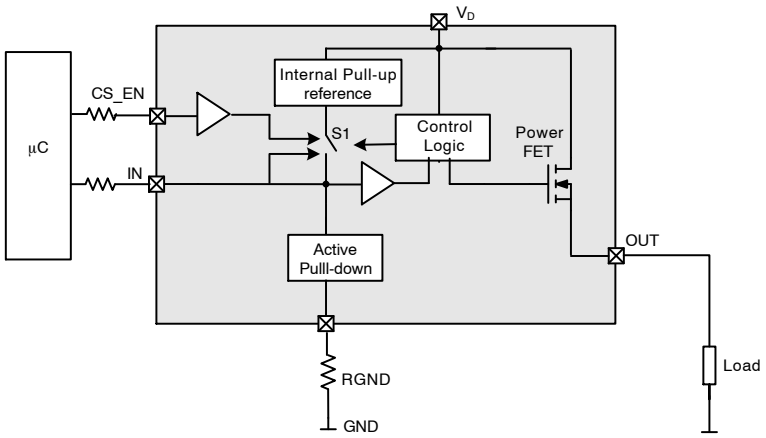


Figure 9. NCV84003G IN Latch Operational Diagram

As shown in the diagram, the voltages at IN and CS_EN pins are sensed and consequently the internal pull-up reference is enabled/disabled via switch S1. If IN pin is asserted High while CS_EN = Low, then this reference is activated and the buffered IN signal to the control logic remains High, thereby driving the output stage ON. If, now, IN signal from microcontroller becomes high-impedance, the internal reference maintains the state of the buffered IN signal to control logic and keeps the output stage ON as long as CS_EN = Low. If CS_EN is turned Low → High, or IN is asserted low externally, the pull-up reference is de-activated and the internal pull-down ensures that buffered IN is internally asserted low for device's safety. It should be noted that the pull-up reference is designed to set the voltage at IN buffer such that the output stage is driven ON with external IN = Hi-Z. Refer Table 6 for details on specifications relevant to the latched IN pin.

Finally, it should be noted that asserting a high impedance IN signal for any device operation that requires a defined IN state (such as I^2t Status readback, for example) is not recommended and may result in the requested routine not getting executed unless IN is driven with the required high/low state.

The table below presents some common mode transitions associated with different actions pertinent to IN latch functionality.

Table 22. STATE TRANSITIONS ASSOCIATED WITH IN LATCH FUNCTIONALITY

Present State	Actions		Next State	Qualifier	IN Latch/Output Channel
	IN	CS_EN			
SLEEP MODE	Low → Hi-Z	Low	SLEEP MODE	–	–
SLEEP MODE	Low → Hi-Z	High	STANDBY MODE	–	–
STANDBY MODE	Low → Hi-Z	High	STANDBY MODE	–	–
NORMAL MODE	High → Hi-Z	Low	NORMAL MODE	–	Latch Active, OUT stays ON
NORMAL MODE	High → Hi-Z	High	STANDBY MODE	$t_{IN(Rst)}$ Expired	Latch Inactive, OUT switched OFF
NORMAL MODE	High Hi-Z	Low	PROTECT MODE	Fault Counter > 0	Latch Active, OUT switched OFF w/ protect mode
NORMAL MODE	High → Hi-Z	Low	IDLE MODE	$I_{OUT} < I_{IDLE_TF}$ – AND – I^2t Monitor = 0	Latch Active, OUT stays ON in IDLE mode
PROTECT MODE	High → Hi-Z	Low	PROTECT MODE	–	Latch Active, OUT stays OFF in Protect mode

Table 22. STATE TRANSITIONS ASSOCIATED WITH IN LATCH FUNCTIONALITY (continued)

Present State	Actions		Next State	Qualifier	IN Latch/Output Channel
	IN	CS_EN			
PROTECT MODE	High → Hi-Z	High	NORMAL MODE	$t_{IN(Rst)}$ Not Expired – AND – $t_{CS_EN(Rst)}$ Expired	Latch Inactive, OUT stays OFF w/ Fault Counter reset to 0
PROTECT MODE	High → Hi-Z	High	STANDBY MODE	$t_{IN(Rst)}$ Expired	Latch Inactive, OUT stays OFF w/ Fault Counter reset to 0
IDLE MODE	High → Hi-Z	Low	IDLE MODE	–	Latch Active, OUT stays ON in IDLE mode
IDLE MODE	High → Hi-Z	Low	NORMAL MODE	$I_{OUT} > I_{IDLE_TR}$; $t > t_{IDLE_Exit}$	Latch Active, OUT stays ON w/ exit to Normal mode
IDLE MODE	High → Hi-Z	High	SLEEP MODE*	–	Latch Inactive, OUT switched OFF
CAPACITIVE LOAD MODE	High → Hi-Z	Low	CAPACITIVE LOAD MODE	Exit Conditions not met**	Latch Active, OUT ON in CL mode
CAPACITIVE LOAD MODE	High → Hi-Z	Low	NORMAL MODE	Exit Conditions met**	Latch Active, OUT stays ON w/ exit to Normal mode
CAPACITIVE LOAD MODE	High → Hi-Z	High	CAPACITIVE LOAD MODE	Exit Conditions not met**	Latch Inactive, OUT switched OFF w/ exit to Normal mode

* Subsequent transition from SLEEP → STANDBY provided CS_EN = High.
** Refer Resistive and Capacitive Load Switching Characteristics section.

Power Stage

NCV84003G provides output power through an integrated N-channel vertical power MOSFET. The gate overdrive is provided by an integrated charge pump.

Output ON-state Resistance

Like any MOSFET, the output's ON-state resistance R_{ON} increases with the junction temperature T_J. R_{ON} also depends on the supply voltage V_S (Figure 10).

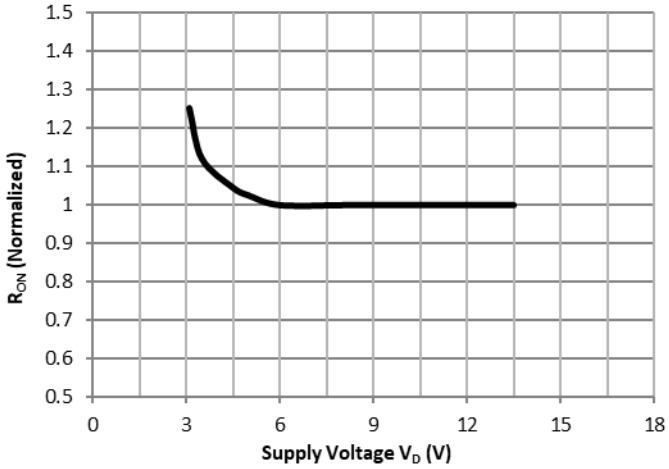


Figure 10. ON-state Resistance

In the idle mode of operation, the R_{ON} of the power stage increases to a higher value (Refer Table 5) as the internal controls are re-configured to allow for a reduced operating current consumption at lighter loads.

Resistive and Capacitive Load Switching Characteristics:

NCV84003G provides an integrated slew-rate control mechanism to minimize EMC in case of device switching. The turn on profiles are actively adjusted between CL mode and normal mode to differentiate a capacitive load from other types of loads.

As a default turn on strategy from sleep mode, the device automatically enters CL mode when IN is enabled. While switching on into CL mode, the slew rate is reduced leading to a gradual turn on of the output stage. The delayed turn on allows the device to charge a capacitive load by providing more power to meet the inrush requirements of the capacitor. The load levels in the initial phase of capacitor charging can

be quite high causing a severe transient stress on the device. To avoid such stress, the differential thermal shutdown threshold is reduced during operation in CL mode (Refer Table 8). The high capacitive inrush may trigger the DTSD or overcurrent trip threshold and invoke a shutdown of the output stage. To ensure that the load is fully charged, the control circuit allows for multiple retries (See Figure 12), thereby overriding the fault retry strategy described in ON State Fault Retry Strategy section.

As the capacitive load is being charged, the output voltage gradually increases. The drain-source voltage drop V_{DS} is continuously sensed and once it reaches the threshold defined by V_{DS_Norm}, the device exits to normal mode with normally defined DTSD threshold and retry strategy. Further, a max time specified by t_{max_Cap} is designed in to avoid extended operation in this condition. Since the device allows multiple retries in this mode (for the purpose of charging the capacitor), extended operation at high battery voltage levels should be always avoided. Such an operation may potentially overstress the device, especially if attempting to switch on an oversized capacitor or a short-circuit load with significant wiring harness inductance.

If CS_EN is asserted High, then current sensing is available in CL mode provided the output is fully on.

Since there may be applications that do not require capacitive charging, the following design implementations allow the device to operate in normal mode.

If CS_EN is forced low → high before turning on the input by a time period longer than t_{NORM}, then the device automatically enters normal mode upon enabling the input. Further, if already in CL mode, applying a CS_EN pulse equal to $t_{CS_EN(Rst)}$ while IN = low will force the device into normal mode of operation.

While applying this pulse, the input (IN) must be observed low as CS_EN observes a rising edge followed by a falling edge with the pulse width in the duration specified between the minimum and maximum per Table 9. It should be noted that a current sense enable pulse width, if applied outside the specified range will not trigger the exit to Normal Mode and the device will stay in CL Mode. Such an implementation is similar to the exit from protect mode (Refer ON State Fault Retry Strategy section).

The exit conditions to Normal Mode are summarized below:

1. Auto exit at $V_{DS} < V_{DS_Norm}$, indicating that capacitive load has sufficiently charged.
2. t_{max_Cap} expire as auto-exit to prevent extended operation in capacitive load mode.
3. Forcing CS_EN low → high before IN low → high by at least t_{NORM}.
4. Applying CS_EN pulse that is equal to $t_{CS_EN(Rst)}$ while IN = low.

The waveforms below depict the difference in turn on slew rates and turn on profiles when switching on a nominal resistive load from sleep vs standby mode.

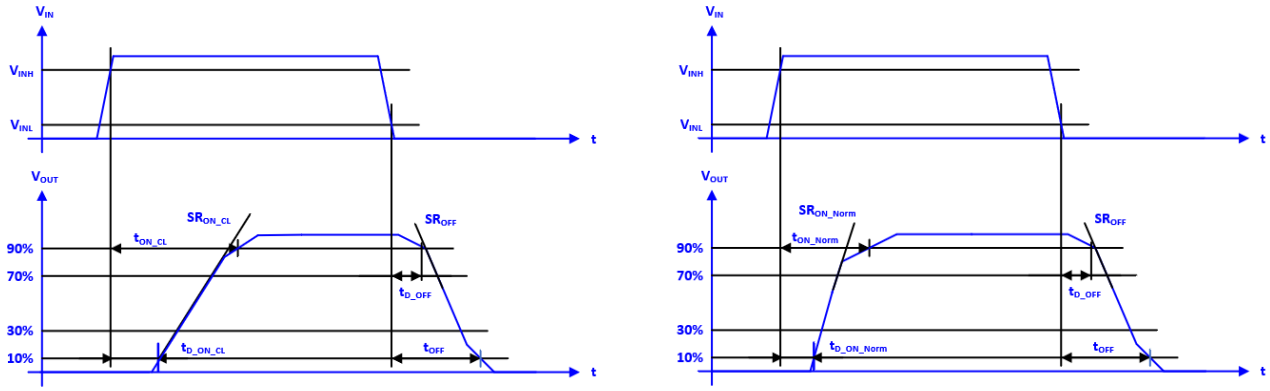


Figure 11. Resistive Load Switching Timing in turning on into a) Capacitive Load and b) Normal Mode

The transition between modes and the exit conditions cited above are described in the idealized wave-set below.

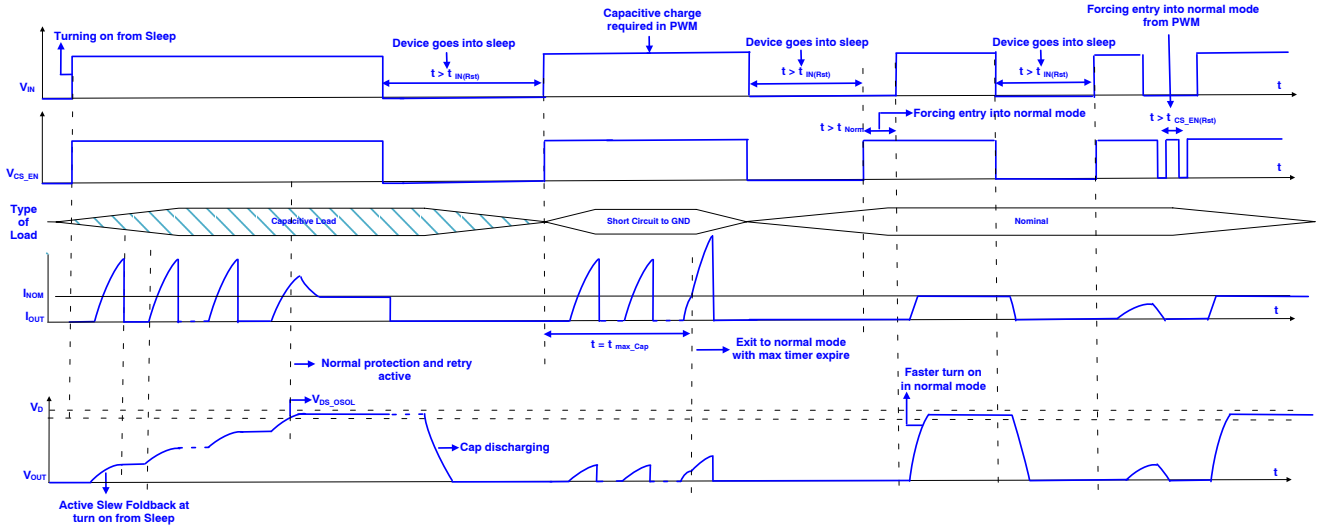


Figure 12. Capacitive Load Inrush Management

Output Clamping with Inductive Load Switch Off

The output voltage V_{OUT} drops below GND potential when switching off inductive loads. This is because the inductance develops a negative voltage across the load in response to a decaying current. The integral clamp diode (Z_{CL}) clamps the negative output voltage to a defined level relative to the supply voltage V_D. During output clamping with inductive load switch off, the energy stored in the inductance is rapidly dissipated in the device resulting in high power dissipation. This is a stressful condition for the device and the maximum energy allowed for a given load inductance should not be exceeded in any application.

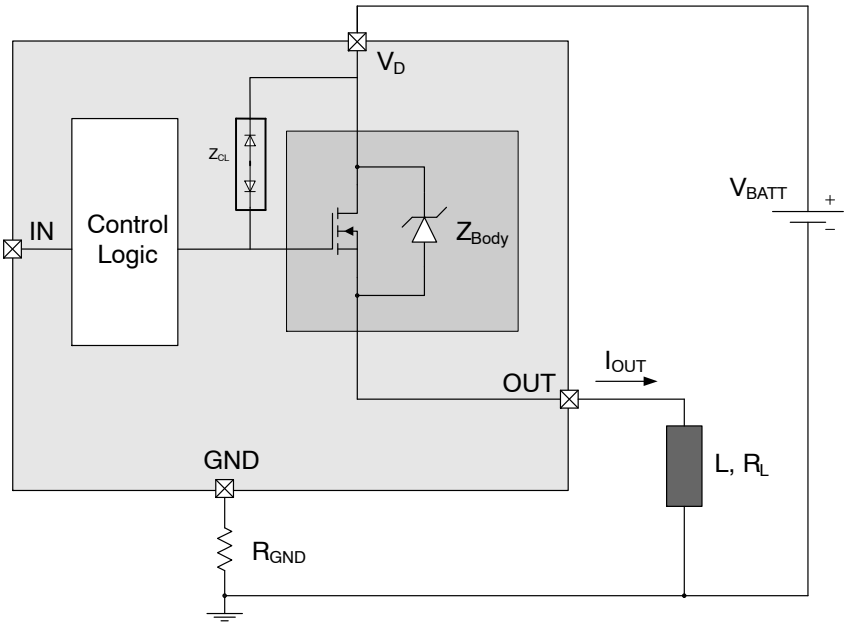


Figure 13. Output Clamping

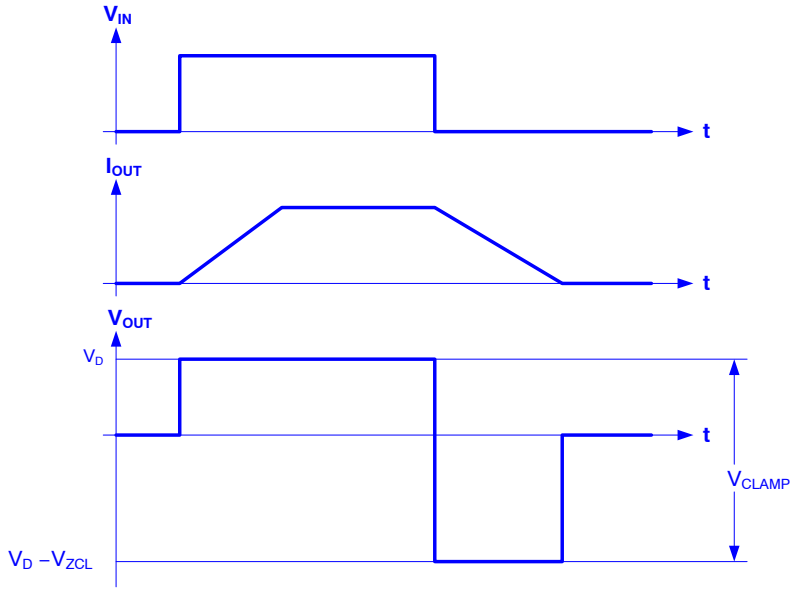


Figure 14. Inductive Load Switching Timing

The channel's energy capability [J] for inductive switching is given as follows, referring to Figure 13:

$$E = V_{ZCL} \cdot \left[\frac{V_D - V_{ZCL}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_{OUT}}{V_D - V_{ZCL}}\right) + I_{OUT} \right] \cdot \frac{L}{R_L} \quad \text{(eq. 1)}$$

Protection Features

In application, the device can be subject to stressful conditions which are outside of normal operating range. To prevent damage and destruction of the device from these fault conditions, several protection functions are integrated in device design. It is important to diagnose and remove any fault condition that may exist since the protection functions cannot prevent damage over sustained fault state operation.

Inverse Current

If an inverse current is applied in the application, VOUT observes a potential greater than V_D. In such case, if the device was OFF initially, the control logic allows the output stage to be turned on if V_{IN} is asserted Low → High. Such an operation limits the power dissipation across the device during inverse current as the body diode losses are succeeded by output FET R_{ON}. In case the device was initially switched ON, it is allowed to stay ON during inverse current mode. The parameter R_{ON_INV} (Refer Table 5) specifies the resistance offered by the output stage in an inverted configuration. The current sense output stays low during inverse current conduction at the output stage. Further, during inverse current operation, protection features as discussed in the ON State Fault Retry Strategy section may not be available.

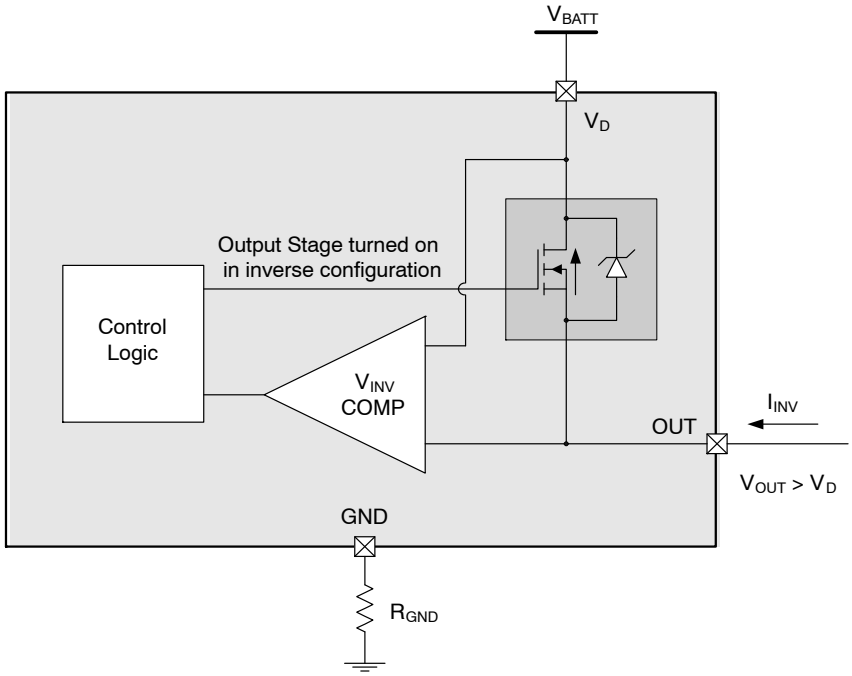


Figure 15. Inverse Current

Loss of Ground Protection

When device or ECU ground connection is lost and the load is still connected to ground, the device will turn the output OFF. In loss of ground state, the output stage is held OFF independent of the state of the input. Protection mechanisms and current sense output of the device will not be available during loss of device ground. Series resistors are recommended between the device and microcontroller to prevent the I/O pins from providing a parasitic GND path through microcontroller. Finally, it should be noted that loss of device ground protection is not guaranteed if the device is operating in IDLE mode.

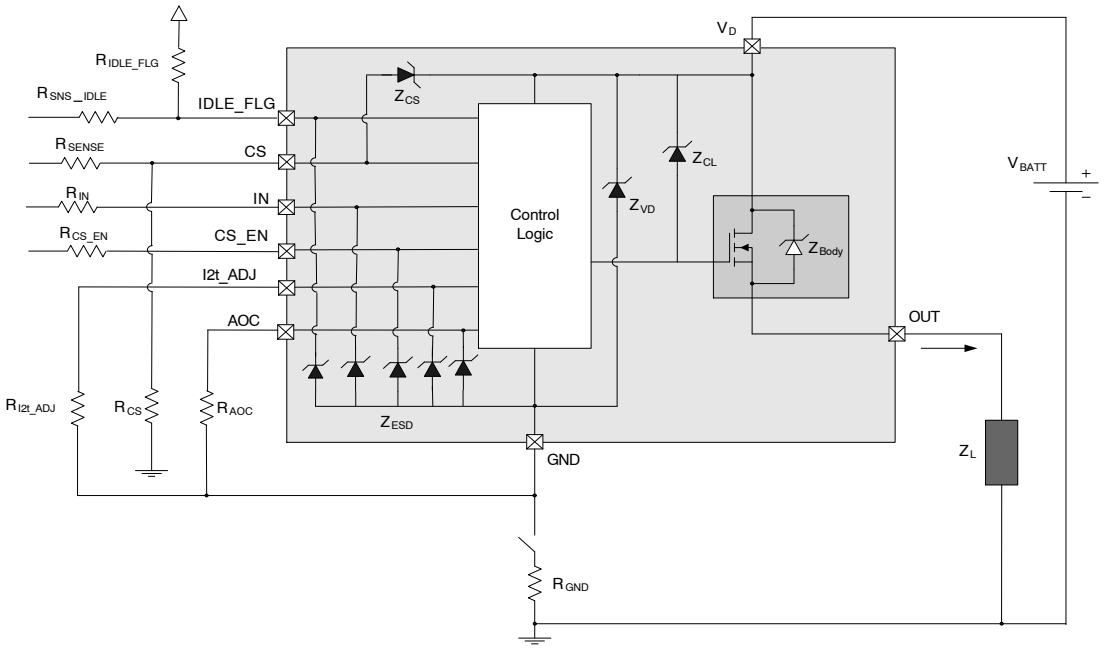


Figure 16. Loss of Ground Protection

Undervoltage Protection

The device has two under voltage threshold levels, V_{D_MIN} and V_{D_UV}. Switching function (ON/OFF) requires supply voltage to be at least V_{D_MIN}. The device features a lower supply threshold V_{D_UV}, above which the output can remain in ON state, if already ON. The protection and diagnostic features are available and functional down to V_{D_UV} (if switch already ON), however, may deviate from the nominally specified parametric performance.

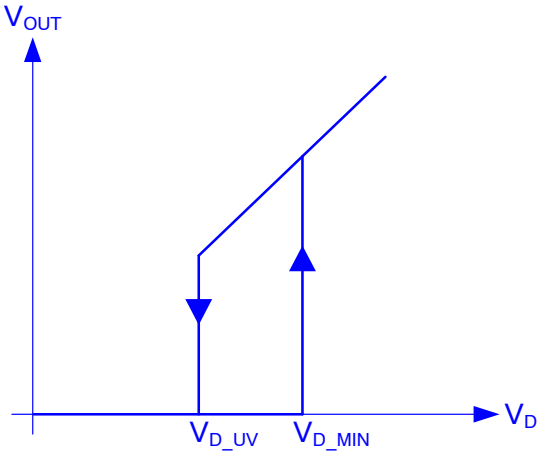


Figure 17. Under-voltage Behavior

In case the supply voltage drops below V_{D_UV} while the channel is ON (V_{IN} = High), the output stage shuts off and a delay time $t_{UV_Recover}$ is incorporated before turning on the output again once the supply increases more than V_{D_MIN}. Such a protection scheme precludes fast repetitive turn on and turn off events and reduces the transient stress on the device as the supply periodically increases or decreases around the under-voltage threshold while conducting high currents. Once initiated, this delay timer is independent of the transitions at the IN pin as shown in the figure below. The delay $t_{UV_Recover}$ is not present if the power supply voltage is greater than V_{D_MIN} at the time of turning the channel ON (V_{IN}: Low → High).

Further, this delay time is shortened in capacitive load mode (Refer Table 4) to allow fast inrush required for charging capacitive loads at low battery conditions such as cranking at cold temperatures. The waveforms below depict the behavior in case of an under-voltage event.

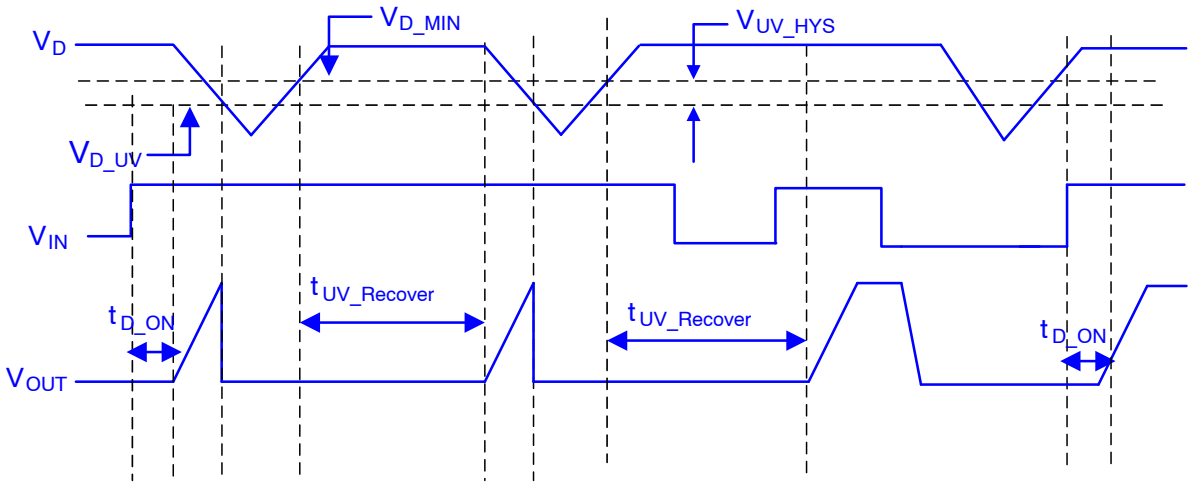


Figure 18. Under-voltage Recovery Timing

The supply dependence of operational transitions specific to IDLE mode (as discussed in section Modes of Operation) is depicted in the wave-set below. For the purpose of this depiction, it is assumed that I^2t monitor stays zero, IDLE functionality is always enabled via IDLE_FLG pin and the criteria for IDLE mode entry/exit is solely decided by the load level and supply voltage level at the drain pin.

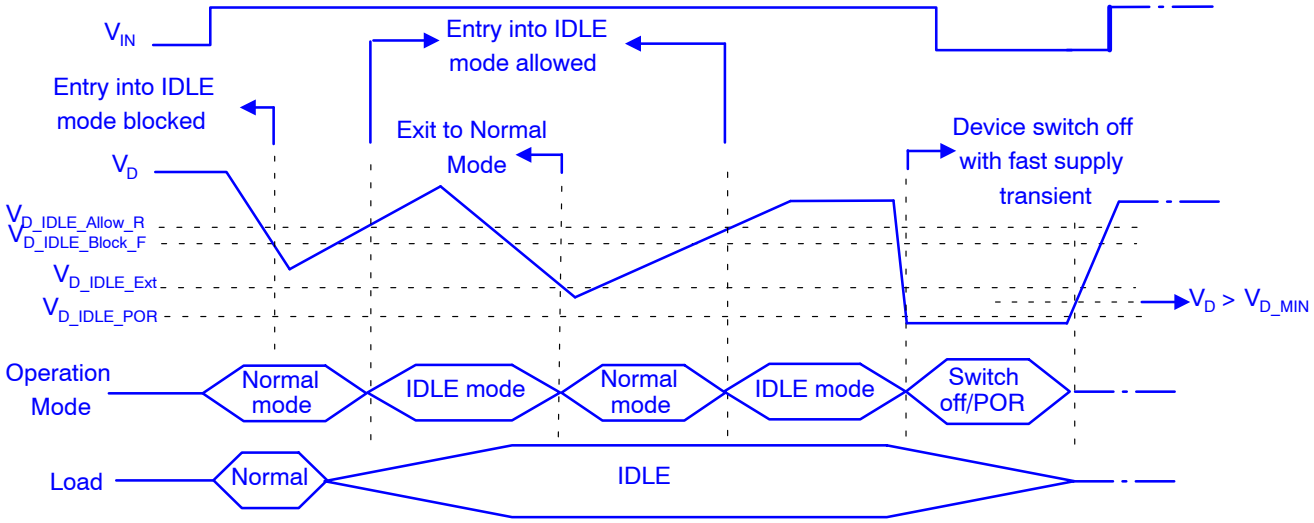


Figure 19. Operational Mode Dependence on Supply Transitions

As can be observed in the wave-set, the device will exit from IDLE mode to normal mode if V_D drops below $V_{D_IDLE_Ext}$ even though the load level is below the IDLE threshold I_{IDLE_TF} (Refer Table 4 and Table 5). Similarly, entry into IDLE mode will only be allowed once the supply level is greater than $V_{D_IDLE_Allow_R}$. Finally, in cases where V_D observes a fast downward transition in IDLE mode and does not allow a timely exit to normal mode, the device will be switched off immediately and internal logic be reset. A subsequent turn on of the output stage will be allowed once $V_D > V_{D_MIN}$ and the corresponding mode of operation (Normal mode/CL mode) will be determined by the state of IN and CS_EN.

Overvoltage Protection

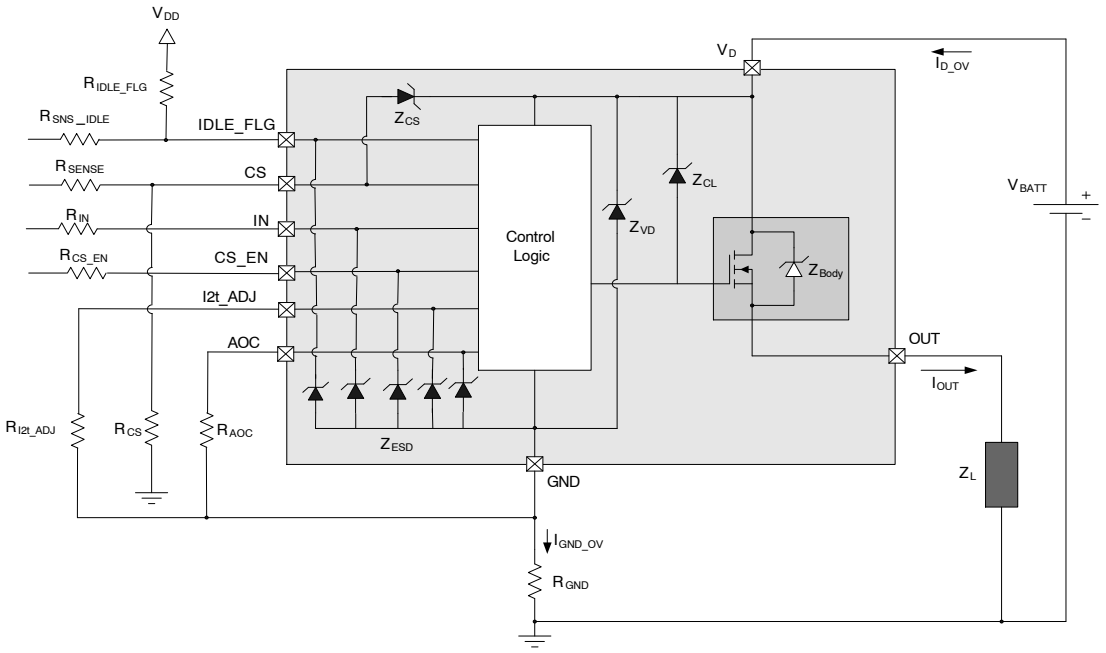


Figure 20. Overvoltage Protection Circuit

The NCV84003G employs a set of over-voltage protection zener clamp diodes − Z_{VD}, Z_{CL}, Z_{ESD} and Z_{CS}, which protect the device against abnormal high voltage events. Z_{VD} protects the logic part by clamping the voltage between supply pin V_D and ground pin GND to V_{ZVD}. Z_{CS} limits the voltage at current sense pin to $V_D - V_{ZCS}$. The output power MOSFET has an integrated drain to gate clamp Z_{CL} that provides protection by actively clamping the voltage across the MOSFET to ~V_{ZCL}. During overvoltage protection, current flowing through Z_{VD}, Z_{CS} and Z_{CL} must be limited. Load impedance Z_L limits the current in output clamp. In order to limit the current in Z_{VD}, a resistor, R_{GND}, is required in the GND path. External resistors R_{CS} and R_{SENSE} limit the current flowing through Z_{CS} and out of the CS pin into the micro-controller I/O pin. With R_{GND}, GND pin voltage is elevated to R_{GND} x I_{GND} during normal operation and must be accounted for while driving the logic inputs referenced to GND. ESD diodes Z_{ESD} clamp the voltage at logic inputs IN, CS_EN and I2t_ADJ, analog input AOC, as well as at open drain IDLE pin relative to the GND pin voltage. External resistors R_{IN}, R_{AOC}, R_{CS_EN}, R_{I2t_ADJ} and R_{IDLE_FLG} are required to limit the current flowing out of these pins. During overvoltage exposure, the device transitions into a self-protection state, with automatic recovery after the supply voltage comes back to the normal operating range. The parametric spec, diagnostic capability as well as short circuit robustness and energy capability of the output MOSFET cannot be guaranteed during overvoltage exposure.

Reverse Battery Protection

In case of Reverse Battery connection, the external load limits the current through the body diode of the output FET. An integrated blocking mechanism blocks the reverse current flowing into the GND and reduces the constraints on the value of R_{GND}. The diagnostic output stays OFF in a reverse battery configuration and no protection feature such as over-current detection or over-temperature shutdown is available. A typical application setup for reverse battery protection is shown in Figure 21. The current in the ESD protection diodes at logic pins and AOC input are limited by resistors R_{IN}, R_{CS_EN}, R_{SNS_IDLE}, R_{I2t_ADJ} and R_{AOC} respectively. Resistors R_{CS} and R_{SENSE} limit the current flowing in the CS pin. The resistor values have to be chosen to limit the current within the current ratings specified in the absolute maximum rating section.

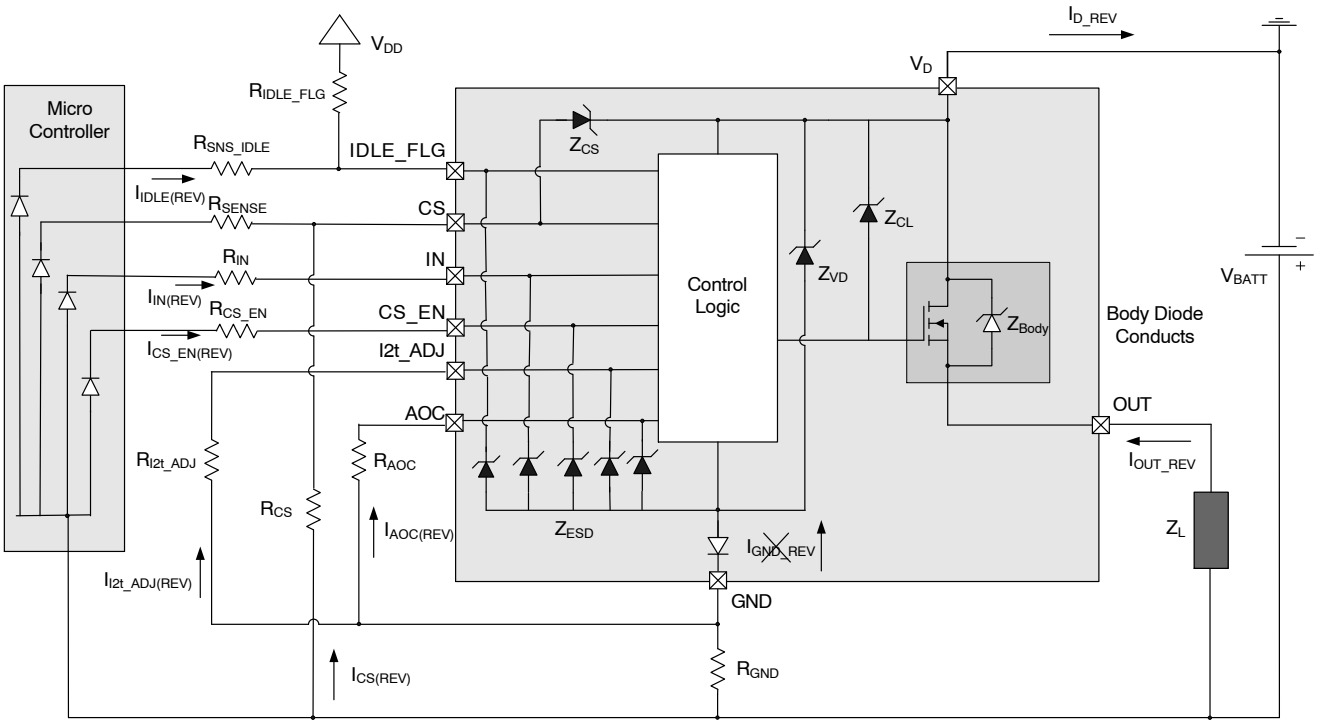


Figure 21. Reverse Battery Protection Circuit

Overload Protection

Overcurrent, I^2t, and over temperature shutdown mechanisms are integrated into NCV84003G to provide protection from overload, capacitive inrush or output short to ground conditions.

Overcurrent Shutdown

To serve multiple applications with different current and power requirements, NCV84003G offers an adjustable overcurrent detection mechanism. The overcurrent detection threshold can be adjusted by the user externally with the help of a resistor at AOC pin referenced to GND. The overcurrent threshold is designed to fold back with the AOC resistor between 25% (for R_{AOC} = 10 kΩ) and 75% (for R_{AOC} = 30 kΩ) of its maximum value. Every 1 kΩ increase in R_{AOC} in the linear range (Refer Figure 22) increases the overcurrent threshold by 2.5% of its maximum value. Table 8 provides thresholds specific to R_{AOC} = 10 kΩ, 20 kΩ and 30 kΩ which are folded back to 25%, 50% and 75% of the highest overcurrent threshold respectively. An R_{AOC} resistor outside the linear range sets the threshold at its maximum (100%) value. Figure 22 depicts the dependence of overcurrent detection threshold on R_{AOC} resistor.

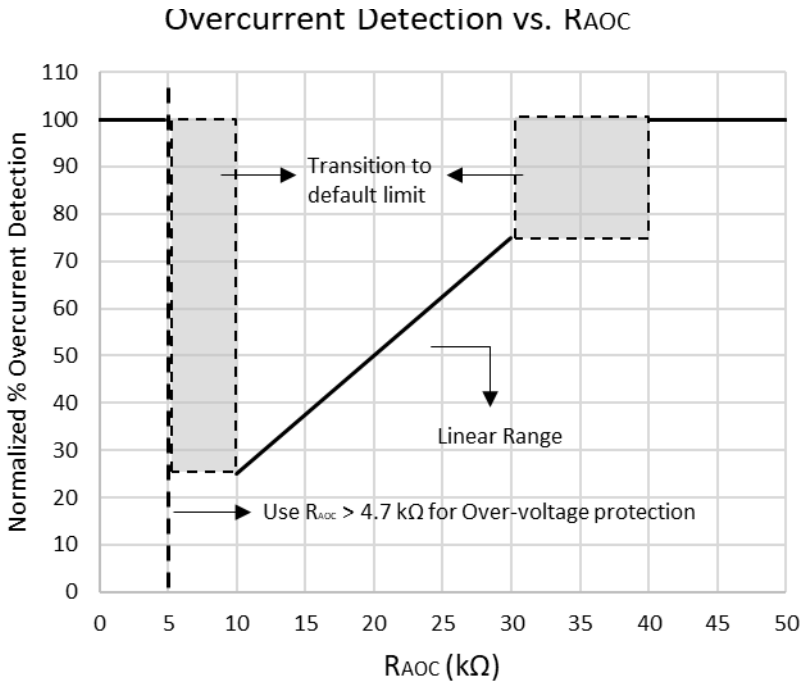


Figure 22. Adjustable Overcurrent Detection vs R_{AOC}

As shown in Figure 22, to set the threshold to its default maximum value, it is recommended to use a resistor at AOC pin that is sufficiently smaller than 10 kΩ or sufficiently greater than 30 kΩ while avoiding the resistors close to transitions in and out of linear range. For example, R_{AOC} = 4.7 kΩ or R_{AOC} = 40 kΩ will ensure that overcurrent detection threshold is set to its maximum value. Further, an $R_{AOC} \geq$ 4.7 kΩ is recommended to protect the ESD structures at this pin against reverse battery and overvoltage events. It is not recommended to short AOC pin to GND in order to protect the internal ESD from stresses inflicted in such events. Further, leaving this pin floating, or open in the application can lead the internal interface susceptible to inadvertent high frequency injections and is also therefore not recommended. Lastly, the resistor at this pin should be placed in close proximity to the device with short traces on the PCB to minimize the impact of any noise coupling on to the signal detected at this pin, especially in the case of high-speed load transients. Although internally filtered, significant noise at this pin may perturb the internal circuits and cause the overcurrent threshold to deviate from the selected value. The device allows readback of the selected overcurrent detection setting in the application using the intelligent current sense output as described in Configuration and Status Readback section.

It's possible for the current profile to observe overshoots beyond the specified I_{LIM} threshold such as in case of transient short circuits with extremely low impedance because of the delay between current detection and consequent shut-off of the output stage. It should be noted that the overcurrent detection thresholds specified in Table 8 are specific to turning the device on into a short circuit with output impedance per AEC Q100-012 Load Short Circuit. Any increase in the load/supply inductance may overstress the device and an external freewheeling path is recommended to discharge the short circuit current in such case.

The overcurrent detection threshold is reduced to a lower value in case of high drain-source voltage. This is done to limit the amount of power dissipation in the device and consequential thermal transients. The curve below depicts the trend in normalized I_{LIM} where the value "1" represents the peak measured at V_{DS} = 5 V. A similar protection logic is applied at high Drain voltages, specifically for conditions such as Jump Start (Refer Table 8). The corresponding I^2t

profiles (as described below), are specifically designed for harness protection and do not change with applied V_D or V_{DS}. The maximum voltage for short circuit protection per Table 2 assumes device operation in normal mode. For short circuit applied in other modes such as capacitive load mode or low power Idle mode, the supply voltage levels should be kept within the nominal operating range per Table 4 to avoid overstress to the device.

Finally, the over-current detection is designed to be relatively independent of junction temperature to ensure that it does not infringe with the I^2t protection.

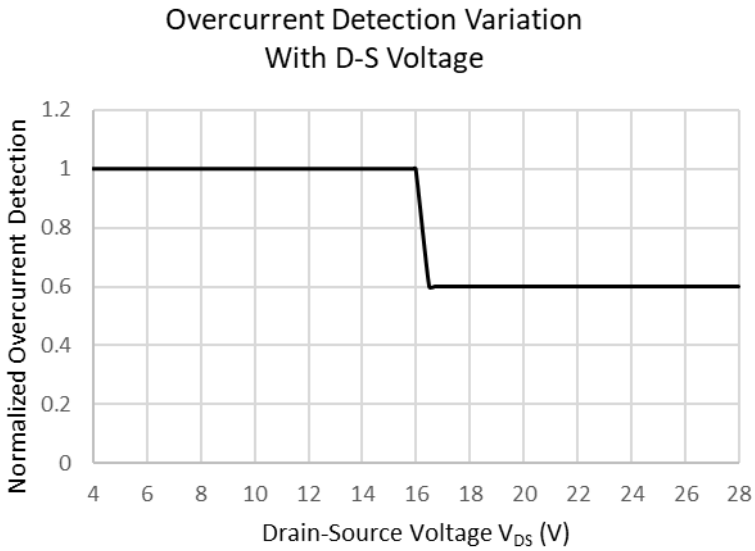


Figure 23. Over-Current Detection Variation with Drain-Source Voltage

I^2t Protection

In addition to overcurrent shutdown, NCV84003G comprises of a smart overload protection in the form of an I^2t function that emulates the current vs time profile of a conventional melting fuse. The built-in circuit forces a shutdown of the output stage when high current is conducted over extended intervals exceeding the I^2t limit of the device per the curve depicted in Figure 25 below. A close representation of conventional fuse's current-time relationship and greater precision than its mechanical counterpart allows the user to seamlessly replace conventional fuses with NCV84003G while guaranteeing harness protection in application. Table 10 specifies the I^2t profile in the form of ON time permitted at different current thresholds designed along the fuse profile. As the current level increases above the minimum threshold I_{I2t_1}, the internal I^2t monitor increases in value as well. Further, the I^2t monitor accounts for the changes in load level by integrating the timing response as output current increases through multiple thresholds, thereby keeping track of the "accumulated heat" as in case of a fuse. The intelligent monitor also reduces in value in case the output current falls below the threshold I_{I2t_1} to account for the "heat lost" in applications such as PWM at overload. When the I^2t monitor reaches 100% of the designed-in limit, the output stage is safely shut off. Once shut off, the retry strategy is defined in the section – ON State Fault Retry Strategy. This response allows proper sizing of the harness in an application by ensuring that a given current will never exceed over a given time threshold thereby keeping the harness insulation within the defined safe operating limits.

The I^2t function is bound on the lower end by highest allowed steady state current I_{I2t_1} below which the I^2t protection is inactive. It is also bound on the upper end by the selected overcurrent threshold that triggers immediate shutdown of the output stage.

Similar to the adjustability in overcurrent detection, NCV84003G offers adjustability in I^2t profiles that allow the user to choose wire harness size for different applications with the same device. The external resistor at I2t_ADJ pin allows scalable profiles in a foldback pattern as depicted in the figure below. Following the AOC dependence on external resistor, the I^2t profile also folds back with the I2t_ADJ resistor between 25% (for R_{I2t_ADJ} = 10 kΩ) and 75% (for R_{I2t_ADJ} = 30 kΩ) of the highest designed profile (outermost curve per Figure 25). Every 1 kΩ increase in R_{I2t_ADJ} in the linear range (Refer Figure 24) increases the I^2t profile by 2.5%. Table 10 provides maximum current thresholds for I^2t profiles specific to R_{I2t_ADJ} = 10 kΩ, 20 kΩ and 30 kΩ which are folded back to 25%, 50% and 75% respectively of the maximum current threshold for the highest I^2t profile. Other current thresholds for the selected profile, thereby, scale commensurately by the same percentage of the corresponding threshold for the highest profile. Figure 25 plots the I^2t profiles for the specified resistor values indicating that NCV84003G could be used to replace melting fuses in the range of 20 A (100% I^2t profile) rating to 5 A (25% I^2t profile) rating. It should be noted that

these curves are only representatives of the allowed range, and any I^2t profile can be selected between these curves by varying the R_{I2t_ADJ} resistor based on the requirements of the application. The internal logic defaults to the highest I^2t profile if the R_{I2t_ADJ} resistor is less than or equal to 4.7 kΩ or is greater than or equal to 40 kΩ (Refer to Figure 24).

To select the highest I^2t profile in the application, it is recommended to use a resistor at I2t_ADJ pin that is sufficiently smaller than 10 kΩ while avoiding the resistors close to transitions linear range. For example, R_{I2t_ADJ} = 4.7 kΩ will ensure the selection of highest profile. In case of an inadvertent open circuit, or a high "leakage" resistance observed at this pin will cause the selection of highest I^2t profile.

It is not recommended to short I2t_ADJ pin to GND in order to protect the internal ESD from stresses inflicted in reverse battery, or over-voltage events. Leaving this pin floating, or open in the application can lead the internal interface susceptible to high frequency injections and is also therefore not recommended.

Lastly, as in case of overcurrent threshold setting readback, the device also allows a readback of the selected I^2t setting in the application using the intelligent current sense output as described in Configuration and Status Readback section.

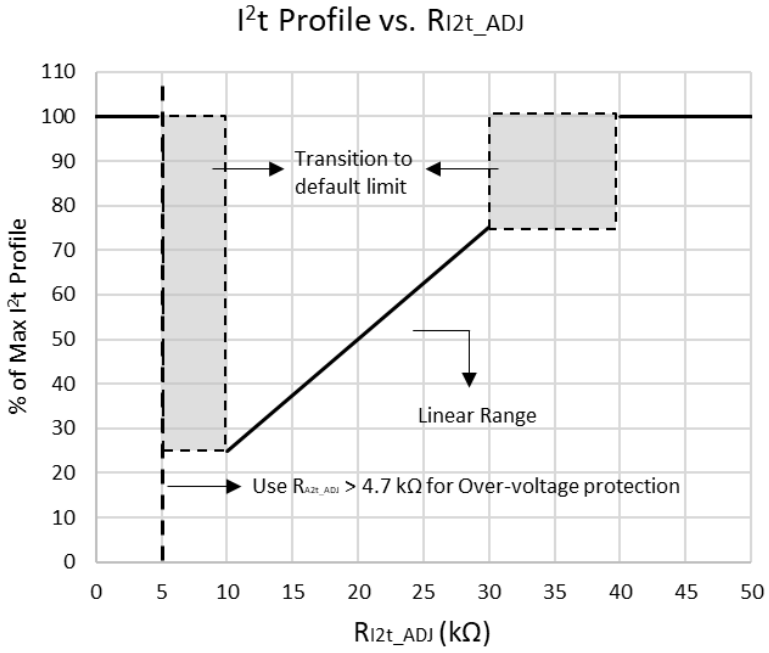


Figure 24. Adjustable I^2t Profiles vs R_{I2t_ADJ}

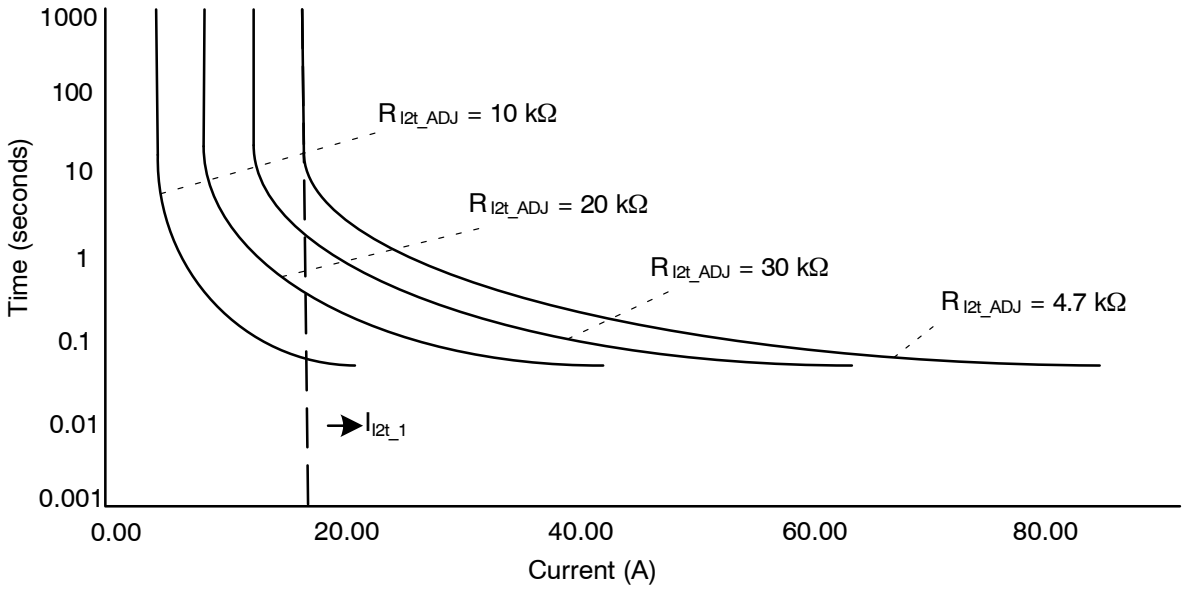


Figure 25. I^2t Protection Implementation

It should also be noted that the profiles depicted in Figure 25 are assuming $T_{J(start)} \leq 85$ °C for each current step and that the device is mounted on a four-layer 2s2p board based on JEDEC JESD 51-7 specification (Refer Table 3). Having inadequate external heat sinking in the application may cause the junction temperature to rise rapidly and output stage may be shut off sooner than the times indicated because of thermal shutdown.

As described above in this section, the internal I^2t monitor is designed to follow to the selected I^2t profile and represents the heat accumulated and lost by the harness in application. It is possible to retrieve the status of this monitor in real time as described in the Configuration and Status Readback section to provide the user dynamic feedback and control over the power dissipation in the application.

NCV84003G can serve multiple load and harness conditions by allowing independent adjustability of over-current detection threshold and I^2t profile. For example, if a high I^2t capability is desired with a reduced over-current threshold for the load, or a high load inrush is desired while keeping the I^2t profile for the harness at minimum, then the example profiles as depicted in Figure 26 can be referenced. Caution must be exercised while selecting an overcurrent trip threshold that is significantly greater than the maximum current threshold (I_{I2t_9}) for the selected I^2t profile. In such a case, the I^2t monitor will enforce the same allowed ON time − t_{I2t_9} for any current greater than I_{I2t_9} until the overcurrent protection is triggered.

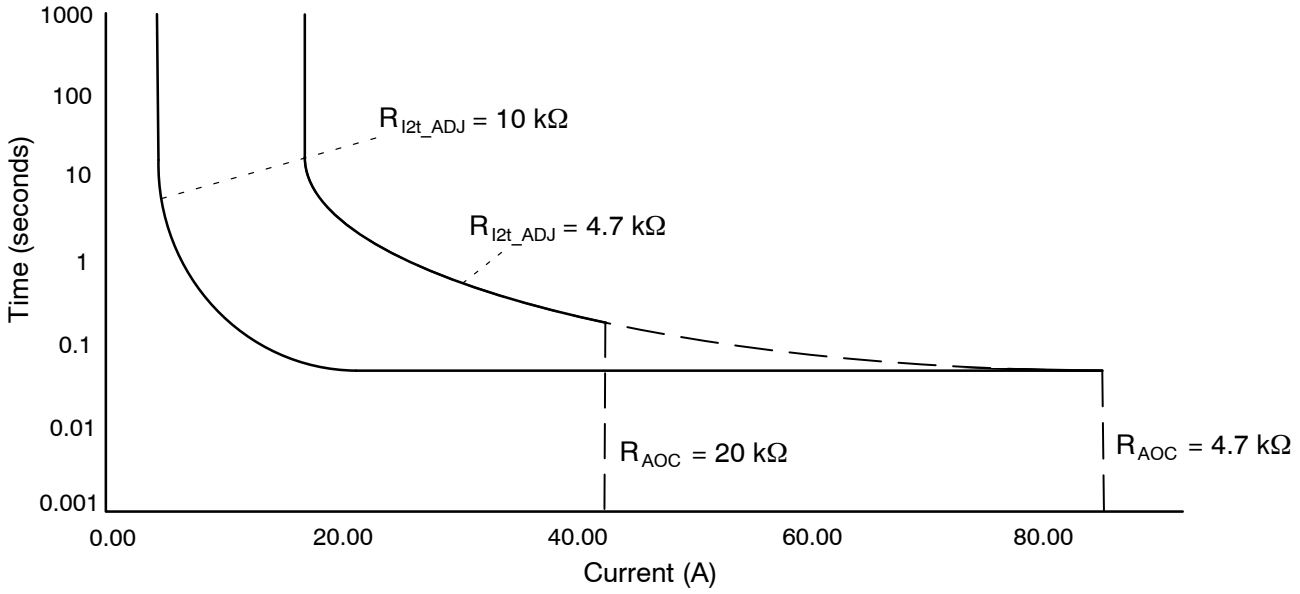


Figure 26. I^2t Maximum Overcurrent Adjustability

Over Temperature Protection

NCV84003G has two over temperature shutdown mechanisms. They are implemented by incorporating an absolute and a differential temperature sensor. To prevent damage and/or destruction, when either of the two sensors is activated, the output will be switched OFF. In case of a prolonged high power dissipation condition, a rapid increase in the junction temperature creates a severe temperature gradient within the device. When this differential temperature swing reaches the defined threshold (T_{DTSD}, per Table 8), the differential temperature sensor is activated thereby switching OFF the device. In case if the junction temperature reaches thermal shutdown temperature T_{TSD}, the absolute temperature sensor is activated, and the output stage will be switched OFF. The output will be allowed to turn back ON when the differential temperature drops to a safe value determined by the hysteresis T_{TSD_HYS} (Refer Table 8) with a retry strategy presented in the next section.

It should be noted that in capacitive load mode, the DTSD threshold is reduced to T_{DTSD_CL} (Refer Table 8) to limit the transient stress on the device while charging a capacitive load. Further, the thermal protections as described above will override the I^2t protection in case the differential or absolute thermal limits of the die are exceeded.

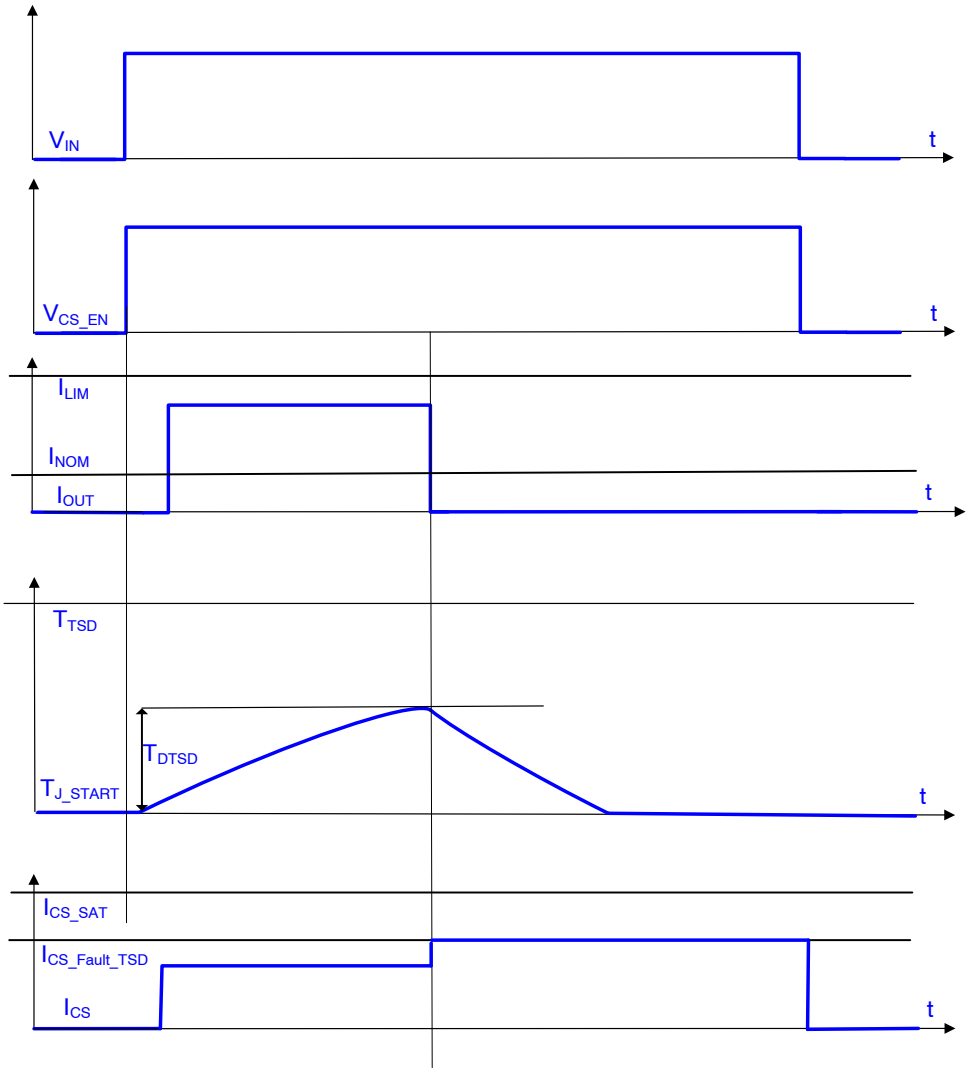


Figure 27. Over-Temperature Protection

ON State Fault Retry Strategy

The timing diagram below explains the Retry strategy in case of an overcurrent and/or over-temperature fault state. It should be noted that while the particular example below considers an overcurrent detection condition in case of short circuit to GND, the same philosophy can be applied to Retry strategy in case of an over-temperature shutdown event as well.

When exposed to the fault conditions mentioned above, the device emulates the behavior of a fuse and the output stage is latched off (thereby entering Protect Mode) after incrementing the fault counter once to protect the device from subsequent high power Retry pulses. The fault counter can be reset to zero (default) by forcing IN low for a time period $t > t_{IN(Rst)}$, or by asserting a current sense enable pulse while IN = low as shown below. If the IN pin is switched Low → High before the $t_{IN(Rst)}$ timer expires, then the output stage is forced to stay off. The timer is reset and starts over again when the input goes low the next time. A current sense enable based reset provides a faster solution to reset the fault counter (typically used in cases where the application microcontroller detects a normal operating condition, and a quick re-start is desired). While enforcing a current sense enable based reset, the input (IN) must be observed low as CS_EN observes a rising edge followed by a falling edge with the pulse width in the duration specified between the minimum and maximum per Table 9. It should be noted that a current sense enable pulse width, if applied outside the specified range will not reset the fault counter and the device will stay in Protect Mode. Further, if input is asserted high at any point during the CS_EN pulse, reset of the fault counter will not be allowed.

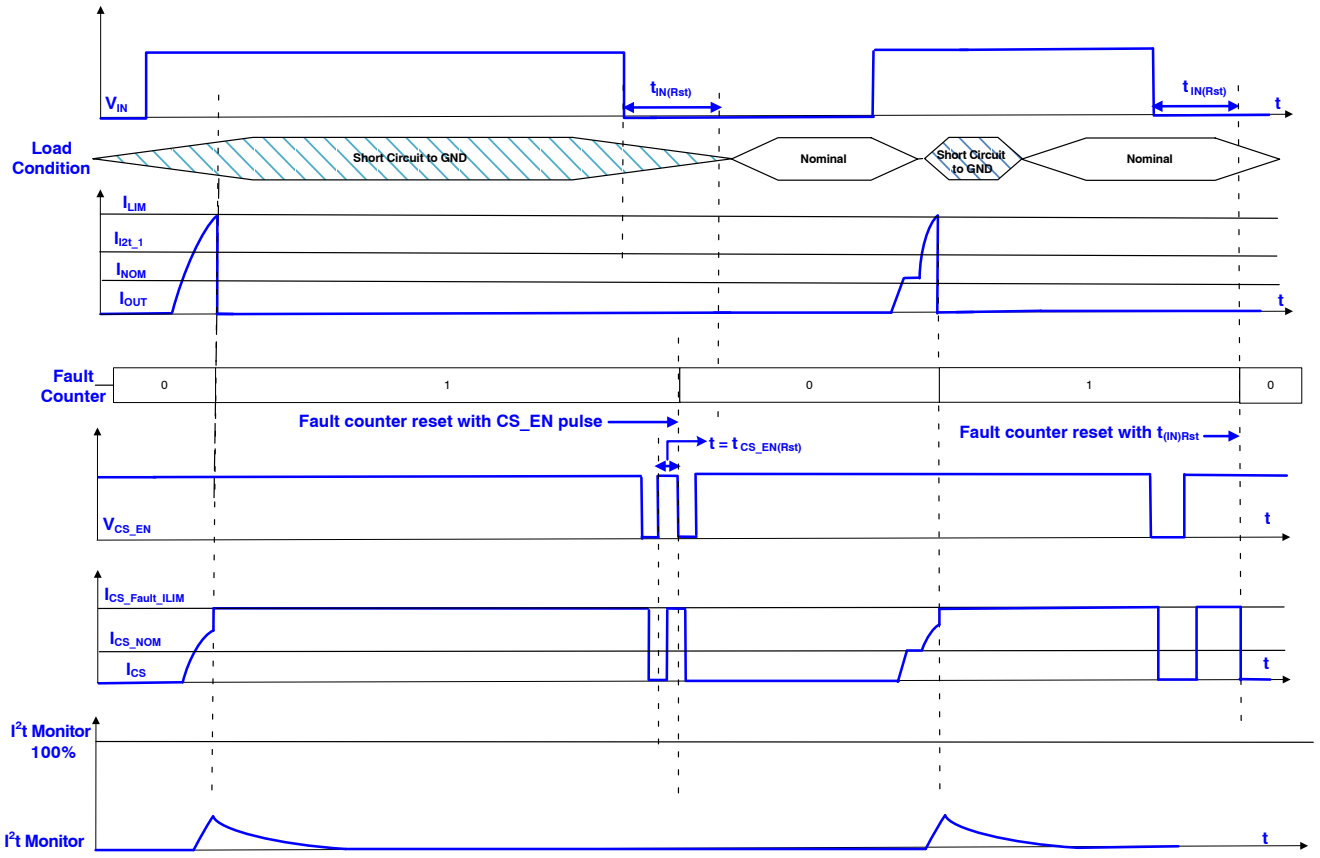


Figure 28. Retry Strategy in Case of Current Limit and/or Over-Temperature

The retry strategy as defined above is overridden while turning on into capacitive load mode to allow multiple retries while charging a capacitive load. It is therefore recommended to exit the capacitive charging mode with an IN pulse (Refer *Resistive and Capacitive Charging*) in case of a shorted load to prevent the device from repetitive transient stresses in this mode. The current sense fault output and voltage at the output node should be sensed to make this decision.

In case of extended overload condition applied to the device, the I^2t monitor increases in value and eventually reaches 100% of the designed limit which then latches off the output stage. The condition is depicted in the wave-set below.

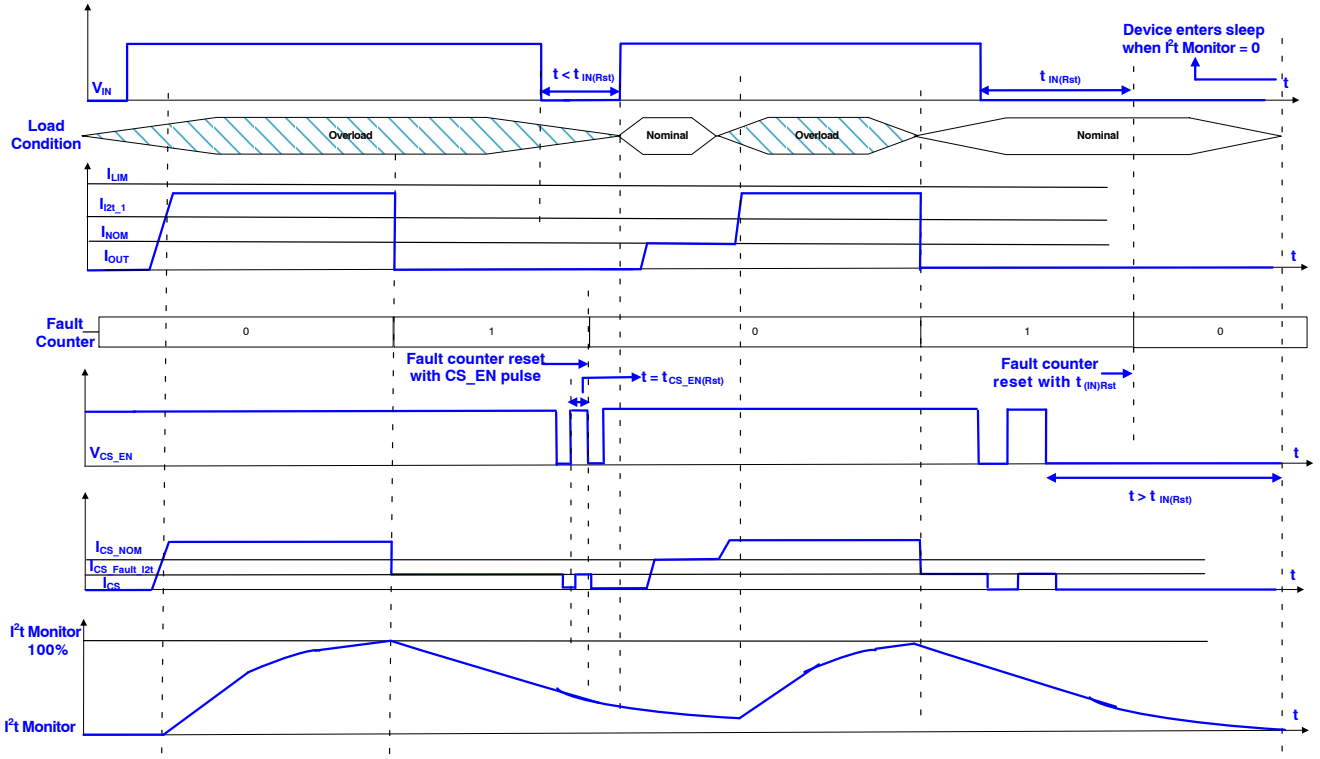


Figure 29. Retry Strategy in Case of I^2t Fault

The flowchart in Figure 30 below summarizes the operation in case of an ON-state fault.

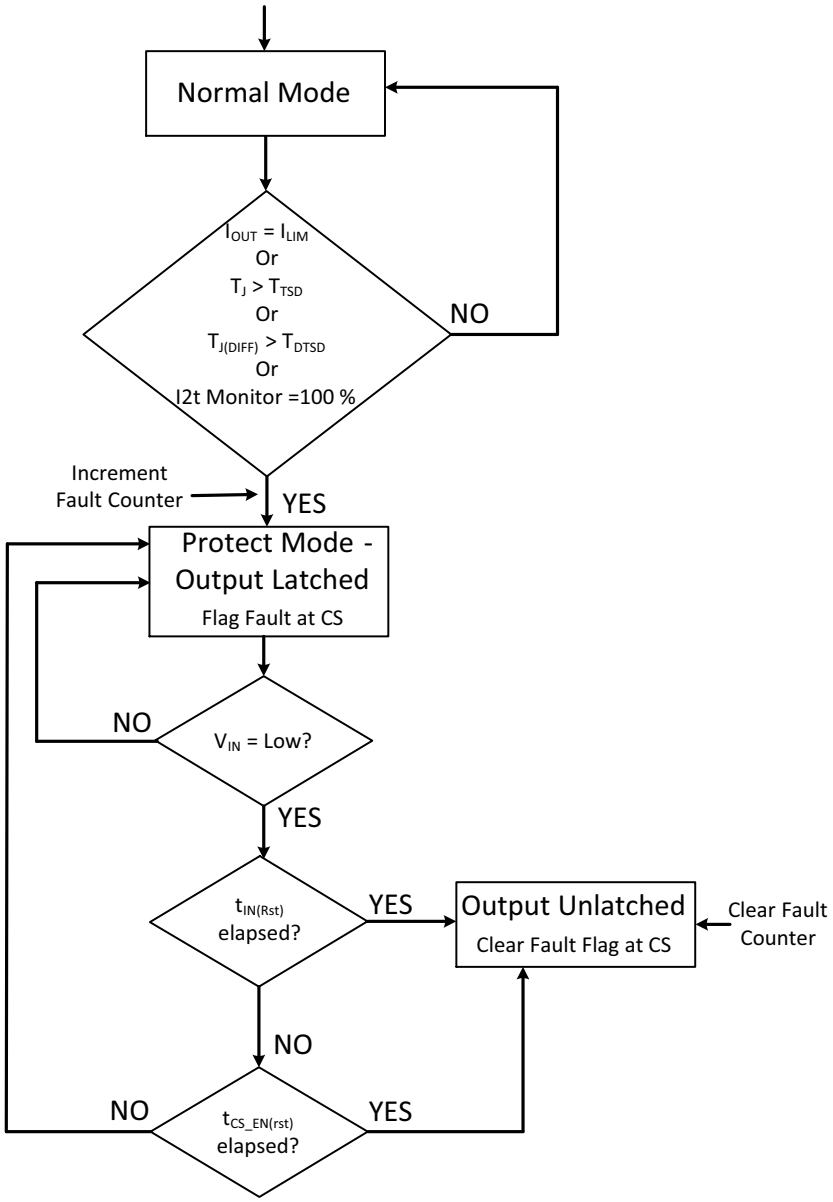


Figure 30. On-State Re-try Strategy Flowchart

Current Sense Output Timing

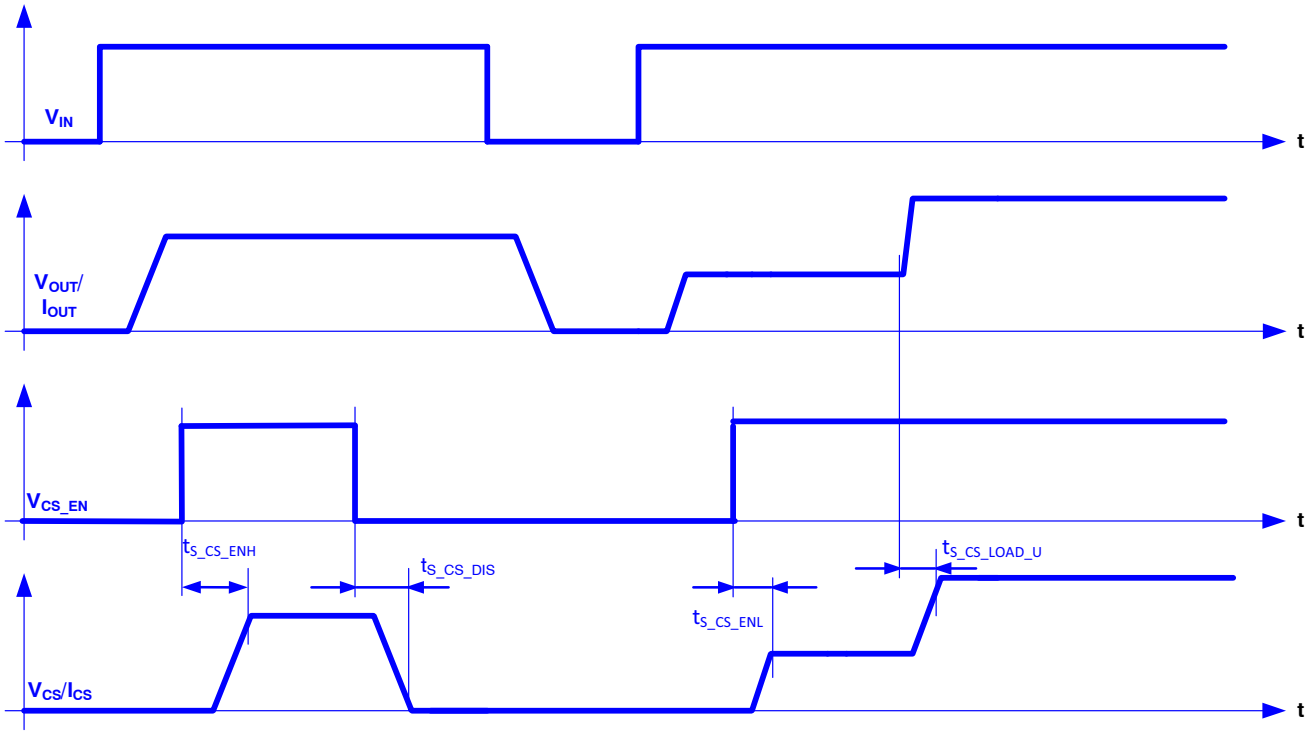


Figure 31. Current Sense Timings

Open Load/Short to V_{BATT} Detection in OFF State

OFF State Open Load (OSOL) diagnosis can be performed by activating an external resistive pull-up path (R_{PU}) to V_{BATT}. To calculate the pull-up resistance, external leakage currents (designed pull-down resistance, humidity-induced leakage etc.) as well as the open load threshold voltage V_{DS_OSOL} have to be considered. A switch can be used open the battery connection to R_{PU} to prevent undesired leakage through this path in case an open load diagnostic is not required.

A short circuit to V_{BATT} in off state is also detected by the same analog circuit block.

It should be noted that OSOL Fault current range is exclusive to and lower than other fault conditions such as a TSD or a current limit. This segregation of fault levels will help user to distinguish an OSOL fault from a case where a fault is being flagged high in OFF state due to an un-expired Fault counter (Refer Table 12. Diagnostic Truth Table).

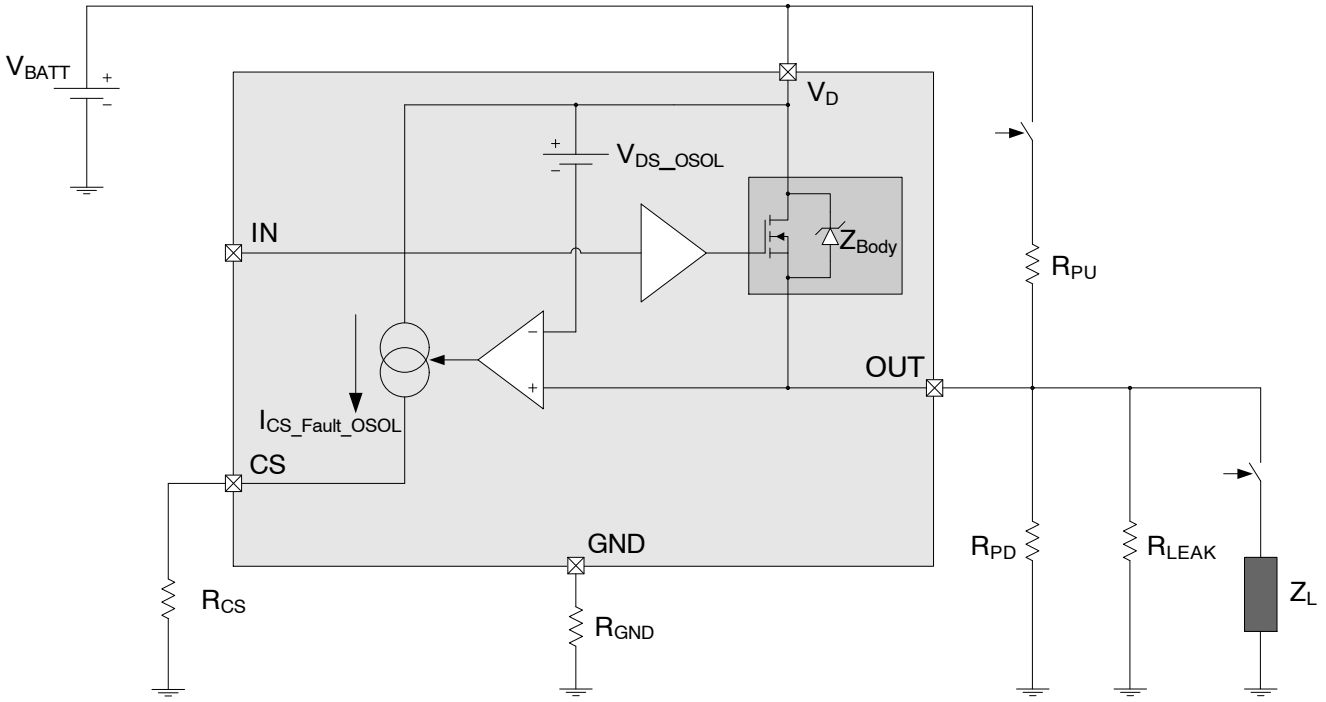


Figure 32. Off State Open Load Detection Circuit

Configuration and Status Readback with Intelligent Current Sense

Configuration Readback

NCV84003G allows the user to read back the device configuration, namely the selected settings for safety-critical protection features: Over-current detection threshold and I^2t profile. The current sense output can be configured such that the output current on CS pin reflects the AOC and I^2t settings as selected in the application with external resistors R_{AOC} and R_{I2t_ADJ} respectively. This readback enhances the functional safety in high power applications by ensuring that device's configuration for above mentioned protection features matches with the external selection made using resistors. Any unexpected overcurrent transients or overload profiles can therefore be prevented with the help of this readback. In addition to the AOC and I^2t configuration settings, the read-back sequence also provides a predefined current out of the CS pin for verifying the functionality of current sense path over time. The description below provides details on the implementation of this readback.

To enable the sequence, a timed pattern as depicted in the figure below needs to be applied to current sense enable logic input when the channel is OFF (V_{IN} = Low). The readback will only be allowed in normal and standby modes of operation, i.e. a) when ON State fault counter is equal to zero (Refer ON State Fault Retry Strategy), b) no Off-State Open Load is detected, and c) the device is not operating in CL mode to ensure that any fault information takes priority over any other data provided on the CS pin.

If all of the above conditions are met, and a CS_EN pulse is applied in the form of a V_{CS_EN}: Low → High transition (rising edge) followed by a V_{CS_EN}: High → Low transition (falling edge) with a pulse width in the duration specified between the minimum and maximum per Table 15, then the CS output is internally configured to provide the readback settings. Once configured, enabling the CS_EN pin (V_{CS_EN}: Low → High) within the specified blank time t_{CR_Blank} (Refer Table 15) will then allow the user to read back the settings on CS pin. It should be noted that a CS_EN pulse width, if applied outside the specified range will not configure the CS output to readback sequence and once configured, the device will only retain the CS configuration for a period of t_{CR_Blank} during which CS_EN input must be enabled to retrieve the information on CS pin, or otherwise the routine will time-out. Further, it is recommended to wait for a duration at-least longer than t_{OSOL_Blank} post V_{IN}: High → Low before applying this CS_EN pulse to allow for open load diagnosis.

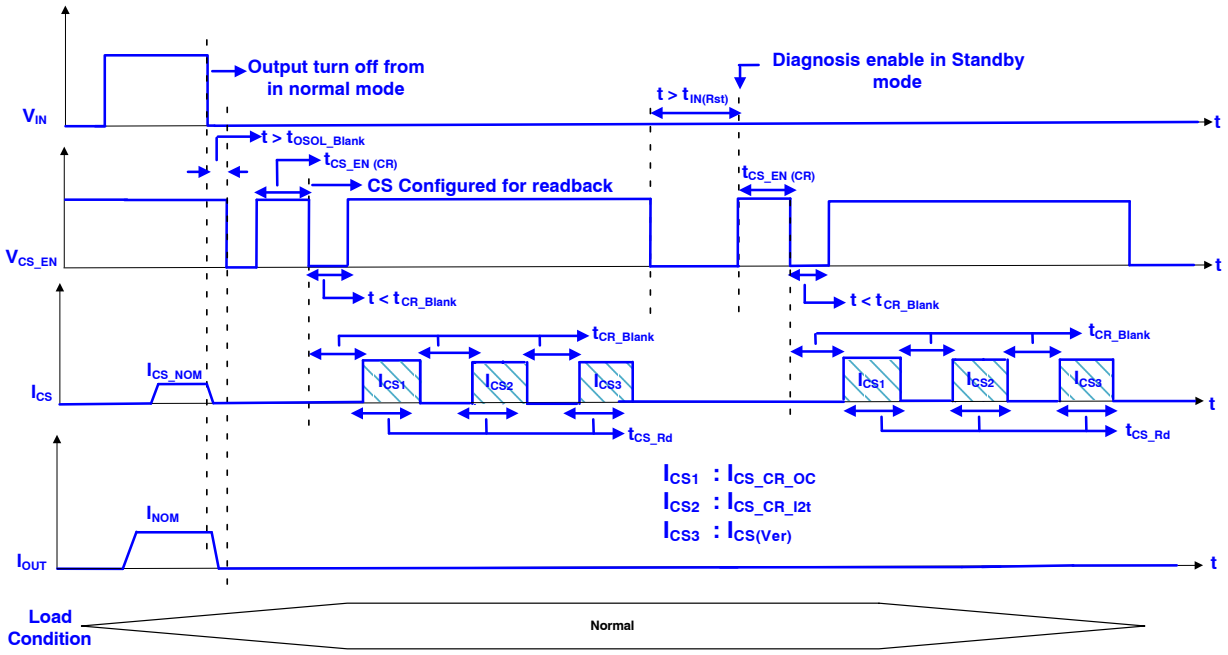


Figure 33. Configuration Readback Routine on CS

In the readback sequence, a single burst of three CS outputs is provided: the first CS output corresponds to the over-current detection setting $I_{CS_Rd(AOC)}$, the second CS output corresponds to I^2t detection setting $I_{CS_Rd(I2t)}$ and the third CS output corresponds to the sense verification current $I_{CS_Rd(Ver)}$. Each of these CS outputs is provided for a duration of t_{CS_RD} which is designed to ensure a timely readback by the application microcontroller while avoiding any signal noise associated with debouncing/filtering etc. A blank time t_{CR_Blank} is observed between successive CS outputs during which the CS output drops to zero to ensure that readback from one configuration does not interfere with the successive readback. Table 16 and Figure 34 describes the CS output currents corresponding to the linear range as well as those corresponding to the default 100% settings (Refer Overcurrent Shutdown and I^2t Protection respectively) for the protection features. The table also specifies the sense verification current. Once all the three CS outputs have been successfully read back, it is recommended to assert CS_EN = Hi → low (to reduce the device operating current) unless any off-state diagnosis is desired. It is also recommended that the supply voltage during readback is within the range specified per Table 16 to ensure a correct readback.

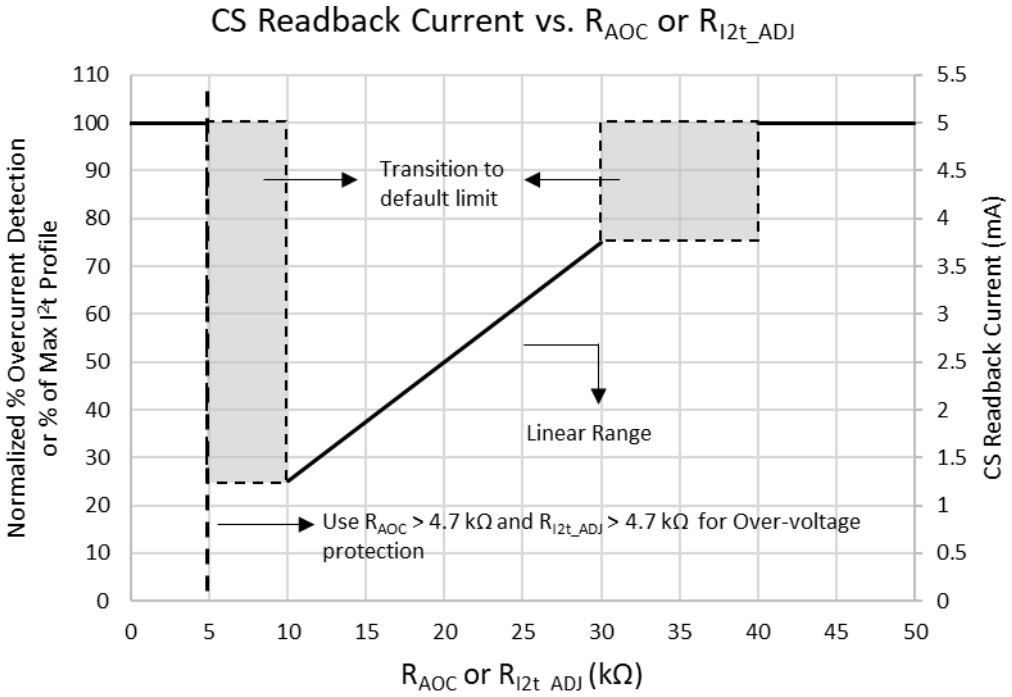


Figure 34. CS Readback Current vs R_{AOC} or R_{I2t_ADJ}

If a) the output channel is switched ON (IN: Low → High), or b) CS_EN is asserted High → Low, and the CS output will provide the proportional load sense/fault information depending on the state of CS_EN. An off state open load fault, if detected during the readback sequence, will be provided on CS pin once the routine has been completely executed.

Example waveforms below depict the device response to configuration readback request in different use-cases such as in the presence of CL mode and ON state fault respectively. As mentioned before, it is required for the device to exit to normal/standby mode first before a readback routine can be configured at CS output.

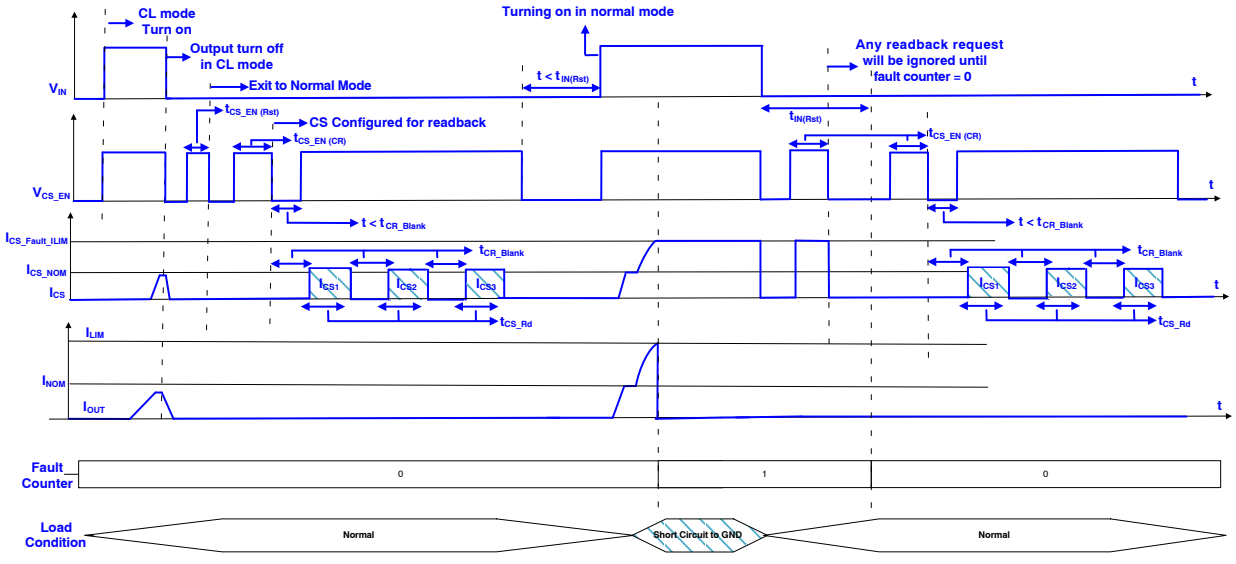


Figure 35. Example Use-cases: Configuration Readback Routine Handling

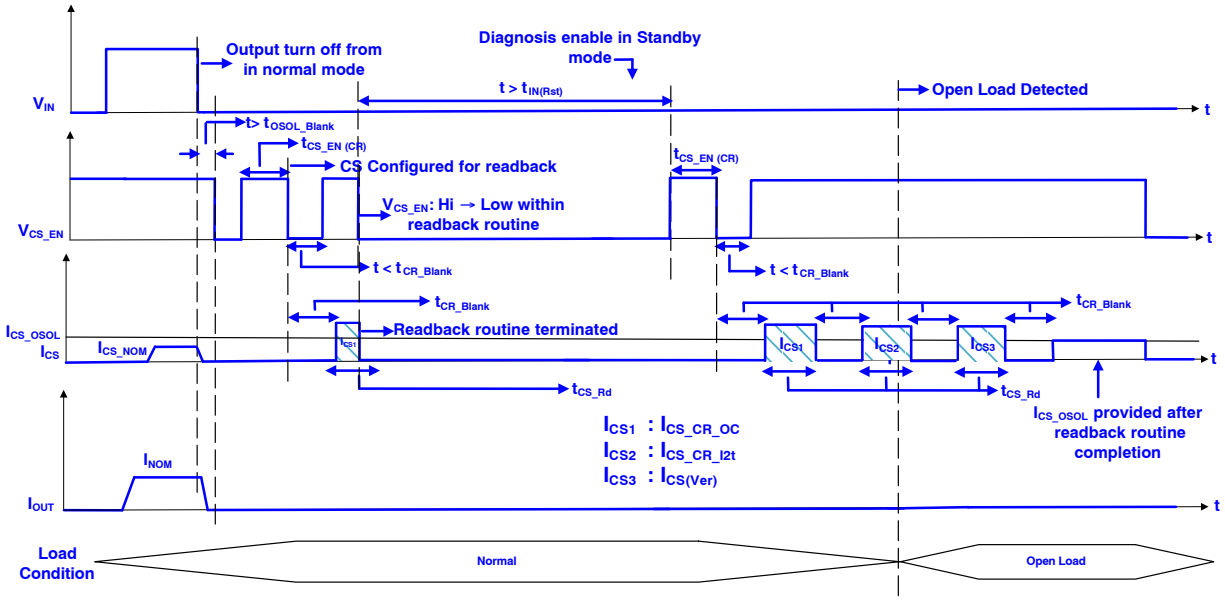


Figure 36. Example Use-cases: Configuration Readback Routine Handling (Continued)

Flowchart in Figure 37 depicts the sequence of operations associated with this readback routine.

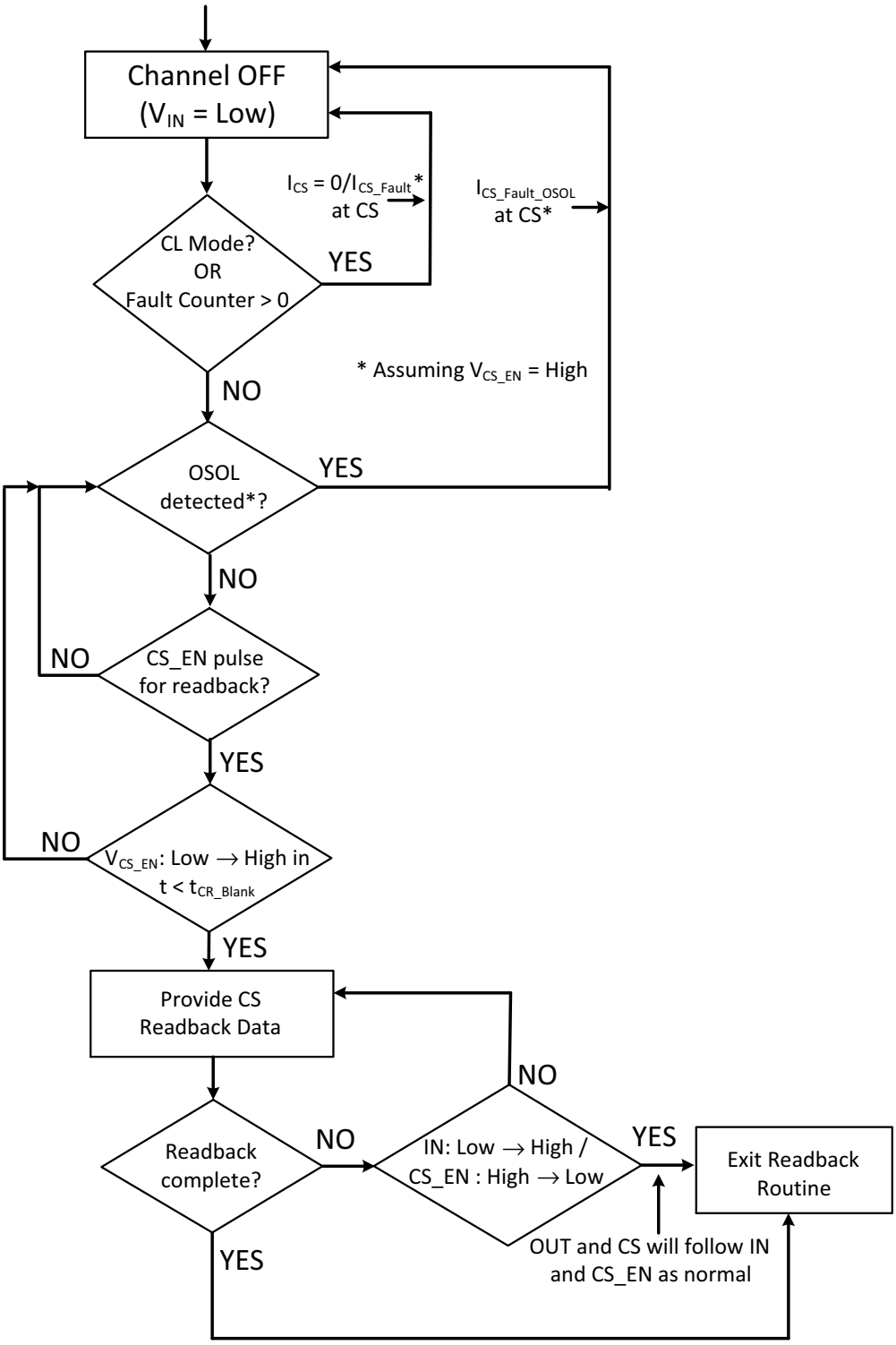


Figure 37. Configuration Readback Routine Sequence of Operations

Status Readback

In addition to the configuration readback, the CS output can also be configured to readback status of I^2t monitor. Since the I^2t feature protects the wire harness in the application, it may be desired to learn the dynamic status of the I^2t monitor, thereby allowing user to take corrective action (such as load regulation, checking for high impedance shorts etc.) before the protection mechanism in the form of output stage turn off is triggered.

Status readback is only allowed in normal and CL modes of operation, if ON State fault counter is equal to zero (Refer ON State Fault Retry Strategy) to ensure that any fault information takes priority over any other data provided on the CS pin.

The current sense enables pattern pulse, as described in Configuration Readback, if applied when output channel is ON (V_{IN} = High) while meeting the conditions described above, configures the CS output for I^2t status readback. Once configured, enabling the CS_EN pin (V_{CS_EN}: Low → High) within the specified blank time t_{CR_Blank} (Refer Table 15) will then allow the user to read back the I^2t status on CS pin. It should be noted that a CS_EN pulse width, if applied outside the specified range will not configure the CS output to readback sequence and once configured, the device will only retain the CS configuration for a period of t_{CR_Blank} during which CS_EN input must be enabled to retrieve the status information on CS pin, or otherwise the routine will time-out.

The status readback, once configured, is available during PWM operation of the output channel to provide information on I^2t monitor. A falling transition at CS_EN, i.e., V_{CS_EN}: High → Low transition at any time during the status readback will terminate the routine and thereafter, CS output will provide load current/fault information as usual depending on the state of V_{CS_EN}. If any ON state fault is detected (such as overcurrent, I^2t, etc.) during the status readback, then fault output at CS pin will take priority over status readback and the readback routine is terminated.

If, however, an open load is triggered during the readback routine, an exit from the routine (V_{CS_EN}: High → Low) will be required to be able to diagnose open load (by subsequently asserting V_{CS_EN}: Low → High). The timing diagram below depicts the use-cases and signal transitions associated with I^2t Status monitor.

As shown in the wave-set in Figure 38, the I^2t status output at CS is divided into discrete steps with each step representing a percentage range of I^2t monitor's maximum value of 100%. To provide high-accuracy feedback on I^2t status, this maximum value of I^2t monitor is divided into 10 ranges, namely 0%−10%, 10%−20%, 20%−30% and so on all the way up to 90%−100%. As the load current increases past different I^2t thresholds per the selected profile (Refer Table 10), the I^2t monitor increases in value. Similarly, when load current falls below the first threshold I_{I2t_1} (for example, in cases such as PWM, load cycling etc.), the I^2t monitor reduces in value. The real time value of the I^2t monitor is always compared against these 10 ranges and the corresponding current level at CS output is available for readback. Table 17 presents the CS output current levels for different ranges of I^2t monitor. Once the I^2t monitor reaches 100% of its value, the output stage is shut down and I^2t Protection is engaged following which the device enters protect mode. CS output, at this point, is therefore overridden by I^2t fault output until the fault counter is cleared per the description in ON State Fault Retry Strategy.

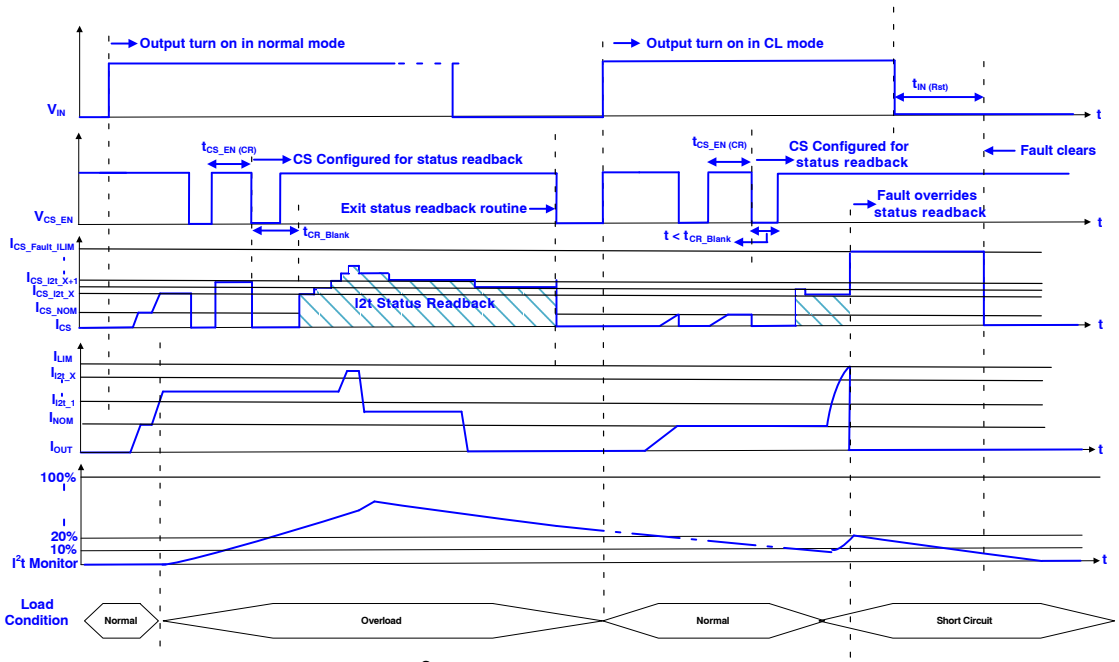


Figure 38. I^2t Status Readback Timing Diagram

The flowchart in Figure 39 depicts the sequence of operations associated with I^2t status readback routine.

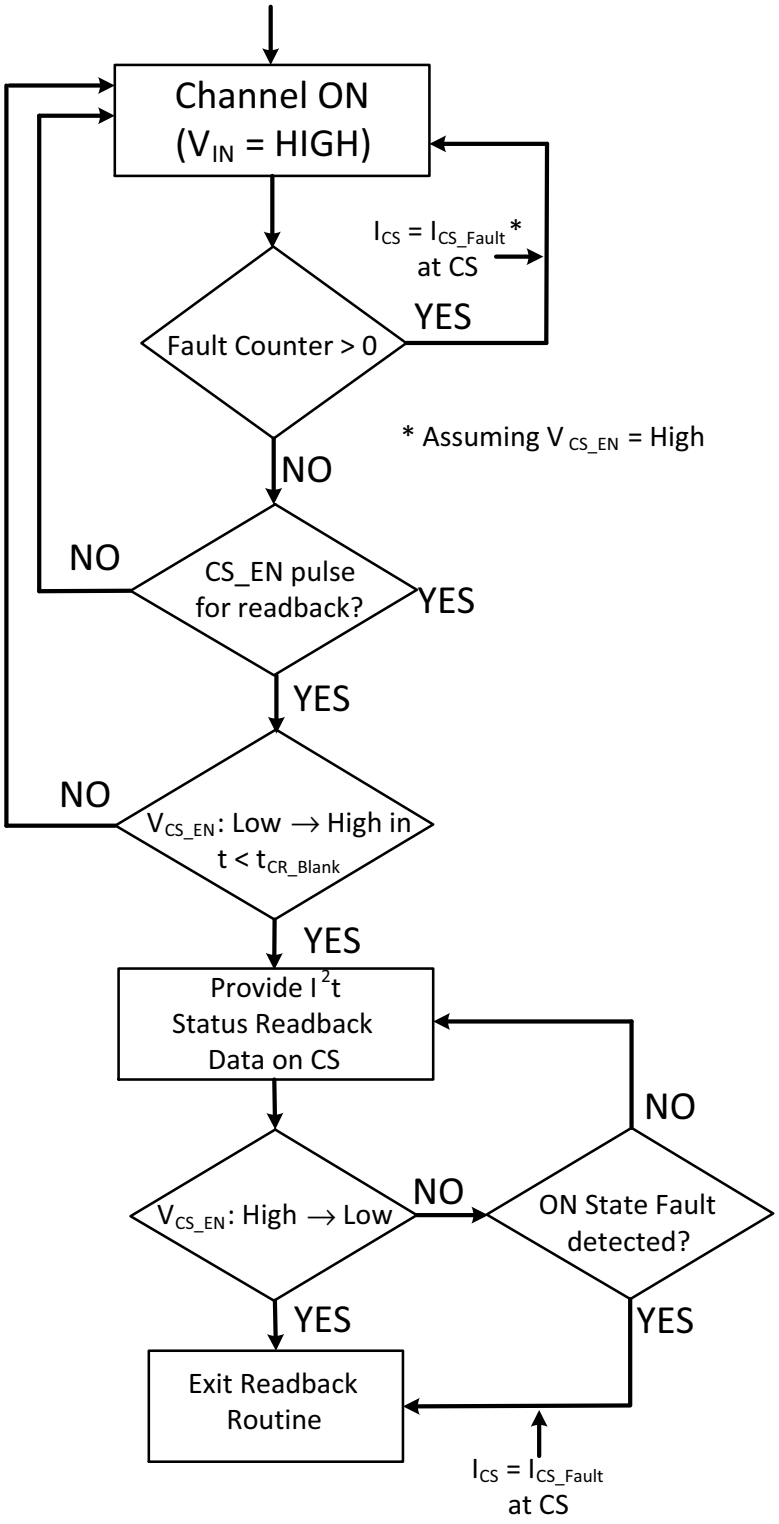


Figure 39. I^2t Status Readback Sequence of Operations

Finally, given the multiple functionalities associated with CS_EN digital input, the table below summarizes different operations and transitions as controlled by CS_EN.

Table 23. CS_EN TRANSITIONS SUMMARY

CS_EN Pulse (V_{CS_EN}: Low → High to High → Low)	IN	Present State	Operation
Pulse Width: $t_{CS_EN(Rst)}$	Low	CL Mode	Exit to normal mode (Note 28)
Pulse Width: $t_{CS_EN(Rst)}$	Low	Protect Mode	Exit to normal mode (Note 29)
Pulse Width: $t_{CS_EN(CR)}$	Low	Standby / Normal Mode	Configuration Readback Activated (Note 30)
Pulse Width: $t_{CS_EN(CR)}$	High	CL / Normal Mode	I^2t Status Readback Activated (Note 30)

28. Refer Resistive and Capacitive Load Switching Characteristics
29. Refer ON State Fault Retry Strategy
30. Refer Configuration and Status Readback with Intelligent Current Sense

Typical Characteristic Curves

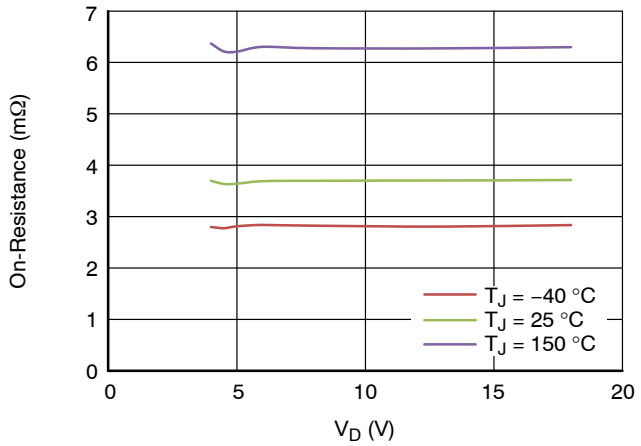


Figure 40. On-Resistance vs. V_D

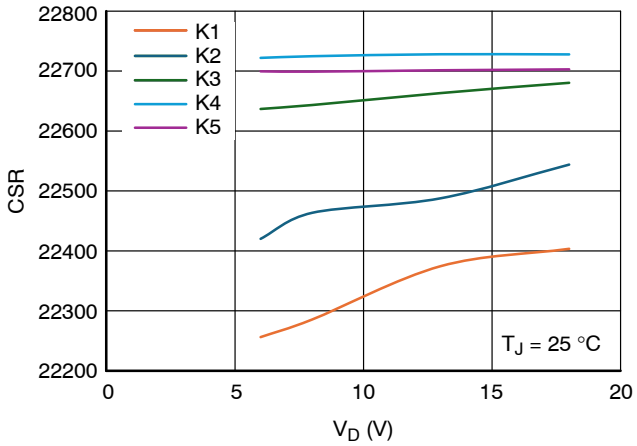


Figure 41. Current Sense Ratio vs. V_D

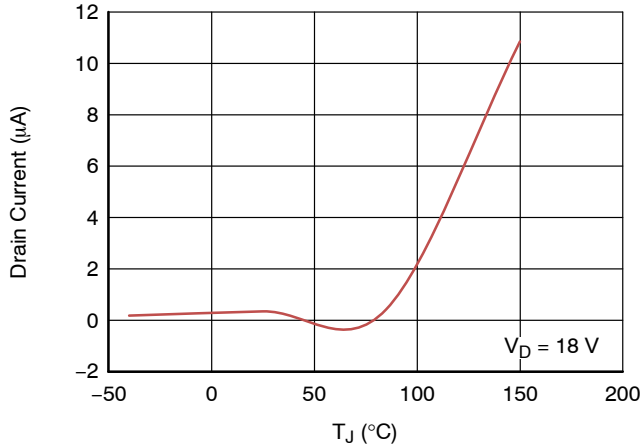


Figure 42. Quiescent Current vs. T_J

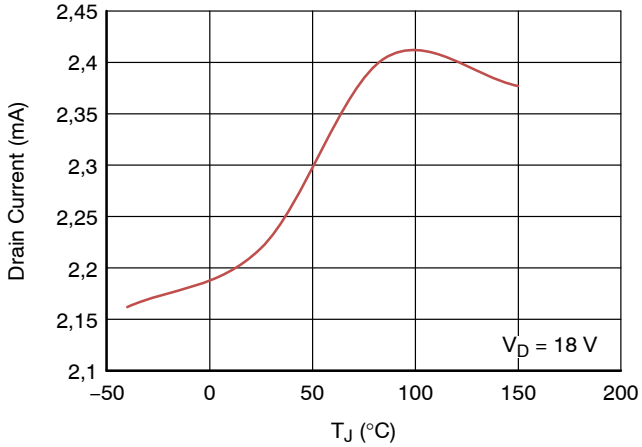


Figure 43. Quiescent Current, Diagnostic Active vs. T_J

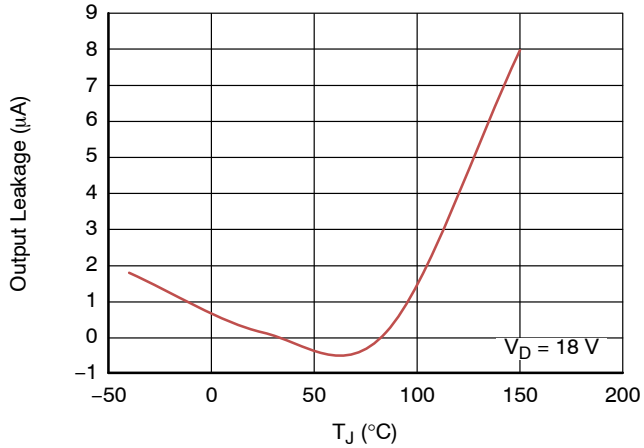


Figure 44. Output Leakage vs. T_J

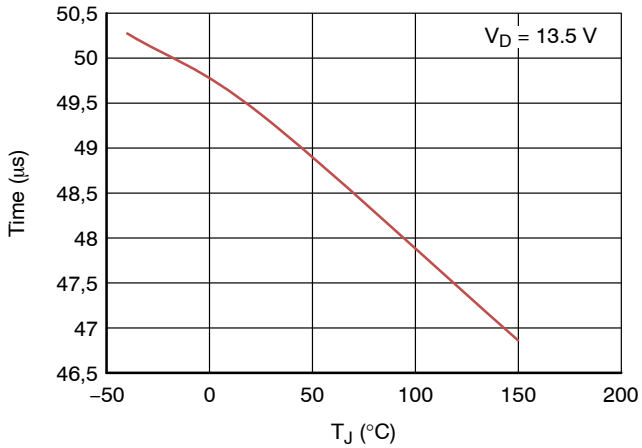


Figure 45. Turn Off Delay vs. T_J

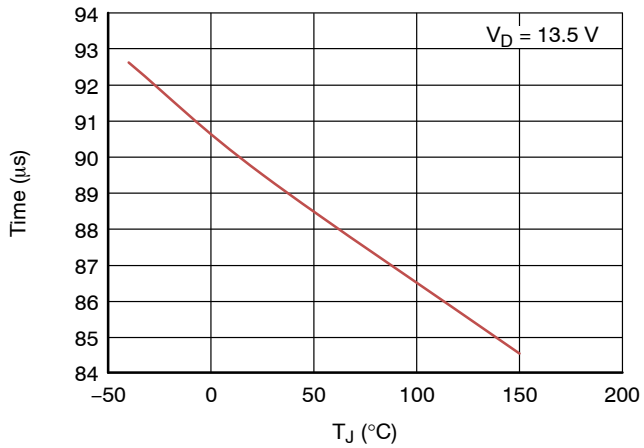


Figure 46. Turn Off Time vs. T_J

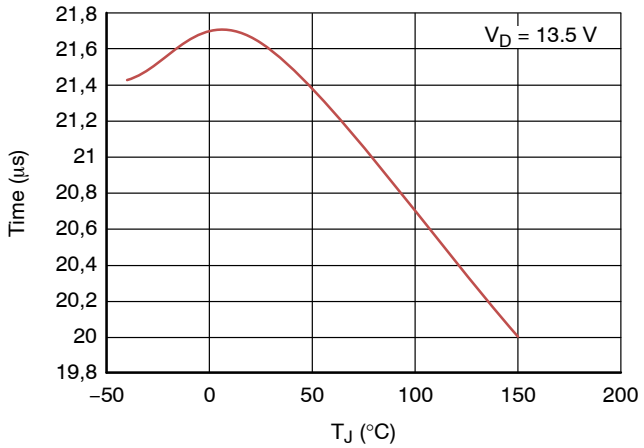


Figure 47. Turn On Delay Normal Mode vs. T_J

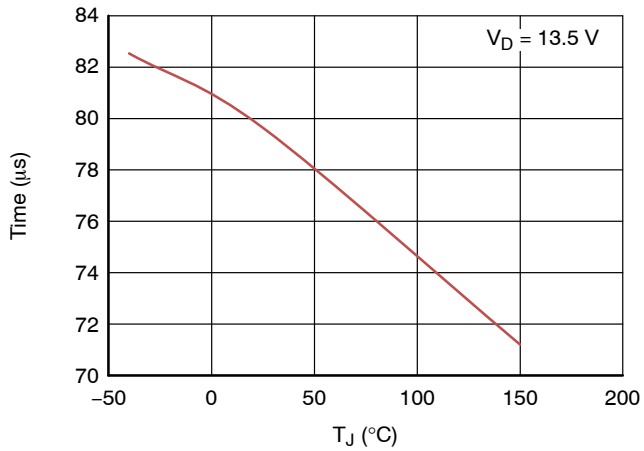


Figure 48. Turn On Time Normal Mode vs. T_J

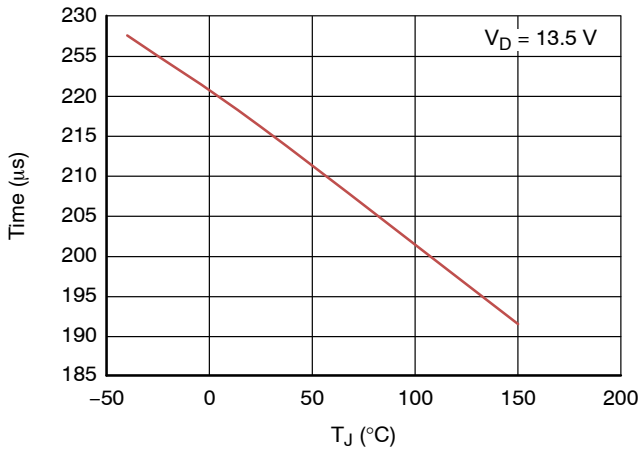


Figure 49. Turn On Delay CL Mode vs. T_J

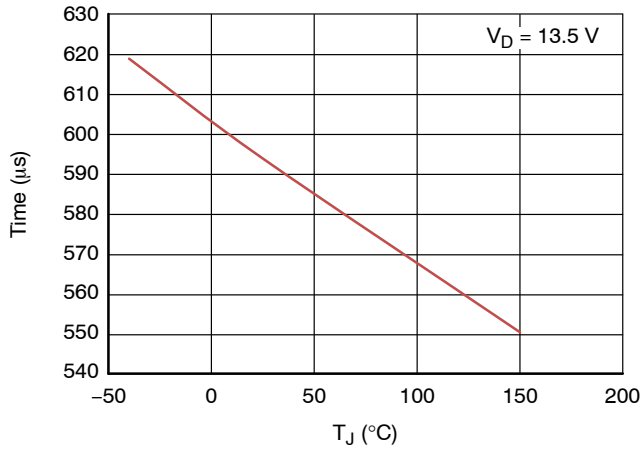


Figure 50. Turn On Time CL Mode vs. T_J

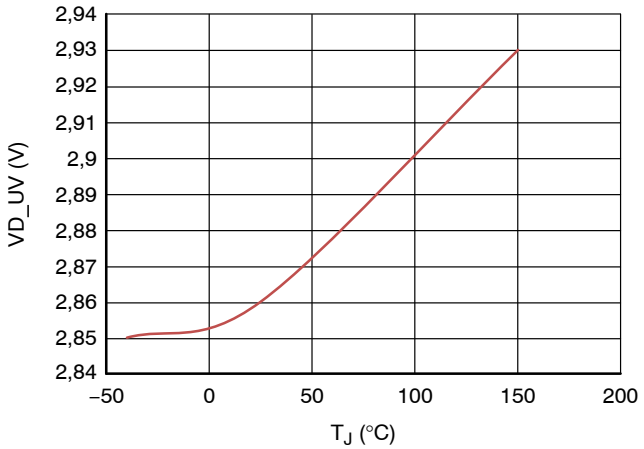


Figure 51. Undervoltage Shutdown (Turn-Off) vs. T_J

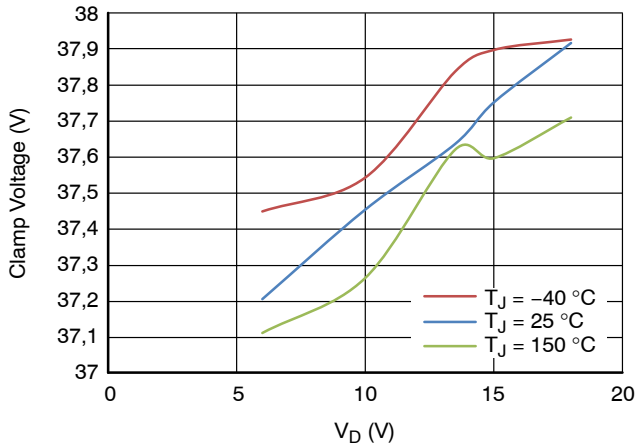


Figure 52. Drain-to-Source Clamping vs. T_J

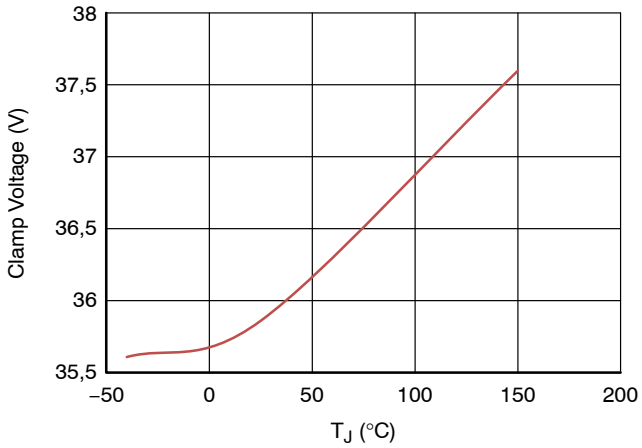


Figure 53. CS Clamp vs. T_J

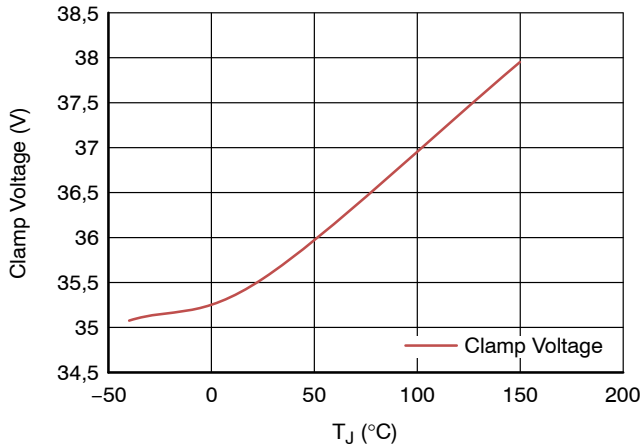


Figure 54. Overvoltage Clamp vs. T_J

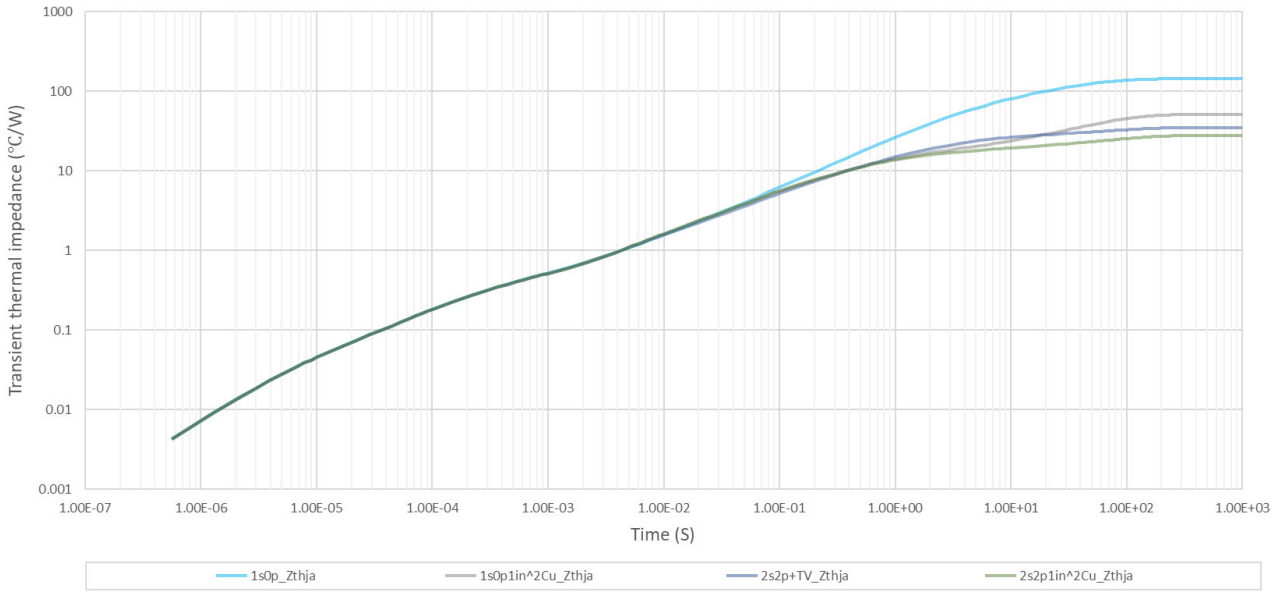
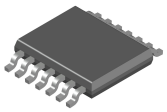


Figure 55. Transient Thermal Response

REVISION HISTORY

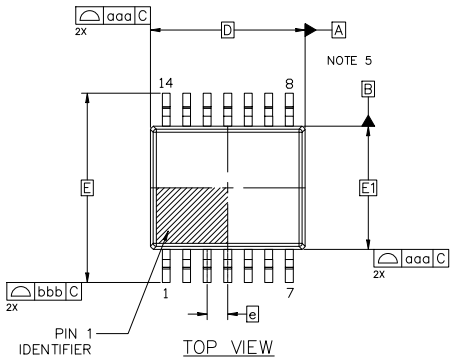
Revision	Description of Changes	Date
0	Initial datasheet release.	4/16/2026
1	Edit notes 5−7, changes to table 3, edit header on tables 4−11, 13−19, edit figure 50.	5/4/2026
2	Updated Typical Characteristics layout to 6-chart standard; corrected I_{GND} value in Feature Summary.	5/26/2026
3	Corrected marking information code.	8/11/2026

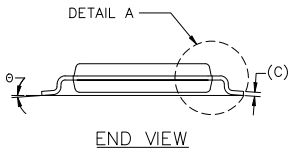


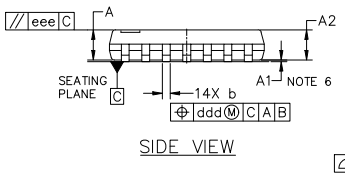
TSSOP14 4.90x3.90x0.95, 0.65P
CASE 948BZ
ISSUE C

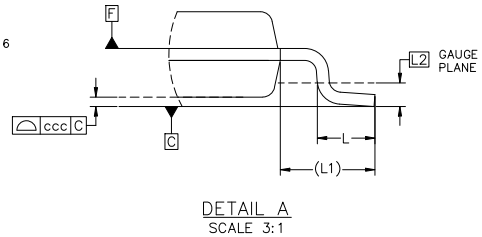
DATE 10 JUL 2025

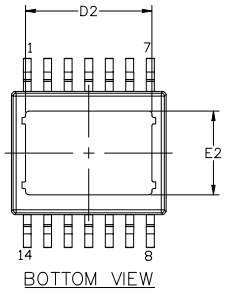
NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M, 2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLE IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.127 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY INCLUDING THE THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGUARATIONS.
7. LEAD THICKNESS (c) AND LEAD WIDTH (b) INCLUDE PLATING THICKNESS.

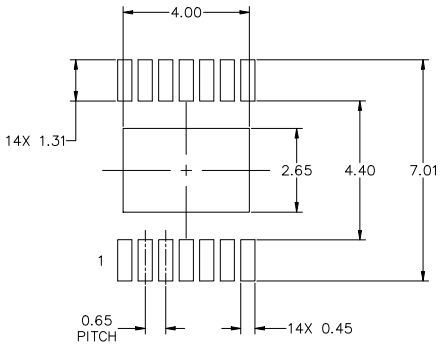










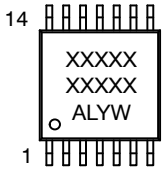


MILLIMETERS			
DIM	MIN	NOM	MAX
A	---	---	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.20	0.25	0.30
c		0.20 REF.	
D		4.90 BSC	
D2	3.90	4.00	4.10
E		6.00 BSC	
E1		3.90 BSC	
E2	2.55	2.65	2.75
e		0.65 BSC	
L	0.42	0.52	0.62
L1		1.05 REF.	
L2		0.25 BSC	
θ	0°	4°	8°
TOLERANCE FOR FEATURE CONTROL FRAME			
aaa		0.10	
bbb		0.20	
ccc		0.08	
ddd		0.10	
eee		0.08	

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON31412H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP14 4.90x3.90x0.95, 0.65P**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2021

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales