# LDO Regulator - High Performance, Low-Power, Enable

# NCV8560

DFN6
MN SUFFIX
CASE 488AE

DFN6
MN SUFFIX
CASE 506BA

TSOP−5
SN SUFFIX
CASE 483

The NCV8560 provides 150 mA of output current at fixed voltage options, or an adjustable output voltage from 5.0 V down to 1.250 V. It is designed for portable battery powered applications and offers high performance features such as low power operation, fast enable response time, and low dropout.

The device is designed to be used with low cost ceramic capacitors and is packaged in the DFN6, 3x3 and TSOP−5 packages.

### Features

- Output Voltage Options:
  Adjustable, 1.3 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 3.5 V, 5.0 V
- Ultra−Low Dropout Voltage of 150 mV at 150 mA
- Adjustable Output by External Resistors from 5.0 V down to 1.250 V
- Fast Enable Turn−on Time of 15 µs
- Wide Supply Voltage Range Operating Range
- Excellent Line and Load Regulation
- High Accuracy up to 1.5% Output Voltage Tolerance over All Operating Conditions
- Typical Noise Voltage of 50 $\mu V_{rms}$ without a Bypass Capacitor
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

### Typical Applications

- SMPS Post−Regulation
- Hand−held Instrumentation
- Noise Sensitive Circuits – VCO, RF Stages, etc.
- Camcorders and Cameras

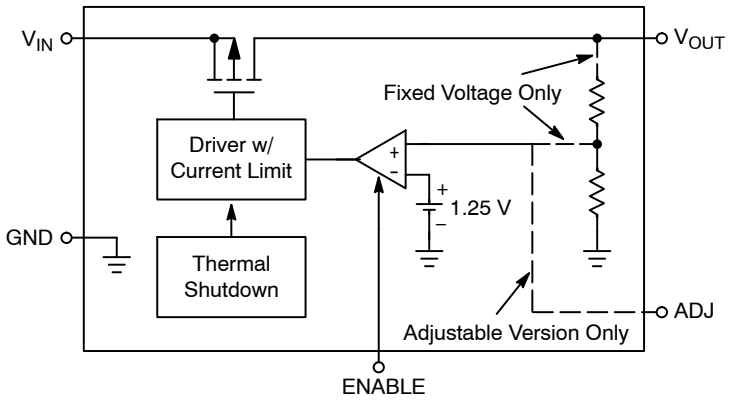
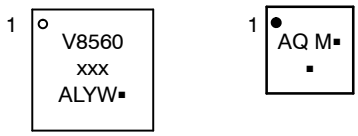



**Figure 1. Simplified Block Diagram**

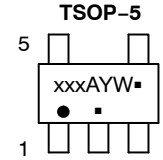
### MARKING DIAGRAMS

**DFN6**




V8560 or AQ = Specific Device Code
xxx = ADJ, 150, 180, 250, 280, 300, 330, 350 or 500
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

**TSOP−5**




xxx = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 13.

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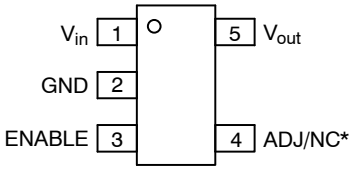
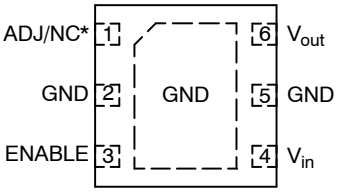
## PIN CONNECTIONS




(Top View)

* ADJ – Adjustable Version
NC – Fixed Voltage Version

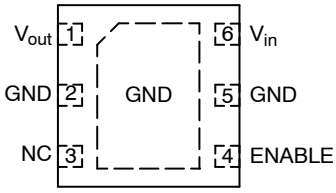
**Figure 2. TSOP5**




(Top View)

* ADJ – Adjustable Version
NC – Fixed Voltage Version

**Figure 3. DFN6 (3x3)**




(Top View)

**Figure 4. DFN6 (2x2.2)**

## PIN FUNCTION DESCRIPTION

| Pin No. | | | Pin Name | Description |
|---|---|---|---|---|
| DFN6 (2x2.2) | DFN6 (3x3) | TSOP−5 | | |
| 3 | 1 | 4 | ADJ/NC | Output Voltage Adjust Input (Adjustable Version), No Connection (Fixed Voltage Versions) (Note 1) |
| 2, 5, EPAD | 2, 5, EPAD | 2 | GND | Power Supply Ground; Device Substrate |
| 4 | 3 | 3 | ENABLE | The Enable Input places the device into low−power standby when pulled to logic low (< 0.4 V). Connect to $V_{in}$ if the function is not used. |
| 6 | 4 | 1 | $V_{in}$ | Positive Power Supply Input |
| 1 | 6 | 5 | $V_{out}$ | Regulated Output Voltage |

1. True no connect. Printed circuit board traces are allowable.

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage (Note 2) | $V_{in}$ | −0.3 | 6 | V |
| Output, Enable, Adjustable Voltage | $V_{out}$, ENABLE, ADJ | −0.3 | $V_{in}$ + 0.3 V | V |
| Maximum Junction Temperature | $T_{J(max)}$ | – | 150 | °C |
| Storage Temperature | $T_{STG}$ | −65 | 150 | °C |
| ESD Capability, Human Body Model (Note 3) | $ESD_{HBM}$ | 3500 | – | V |
| ESD Capability, Machine Model (Note 3) | $ESD_{MM}$ | 200 | – | V |
| Moisture Sensitivity Level | MSL | MSL1/260 | | – |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78.

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, DFN6, 3x3.3 mm (Note 4)<br>Thermal Resistance, Junction−to−Air (Note 5) | $R_{\theta JA}$ | 107 | °C/W |
| Thermal Characteristics, TSOP−5 (Note 4)<br>Thermal Resistance, Junction−to−Air (Note 5) | $R_{\theta JA}$ | 205 | °C/W |
| Thermal Characteristics, DFN6, 2x2.2 mm (Note 4)<br>Thermal Resistance, Junction−to−Air (Note 5) | $R_{\theta JA}$ | 122 | °C/W |

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. As measured using a copper heat spreading area of 650 mm², 1 oz copper thickness.



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## OPERATING RANGES

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Input Voltage (Note 6) | $V_{in}$ | $V_{out}$ + $V_{DO}$, 1.75 V (Note 7) | 6 | V |
| Adjustable Output Voltage Range (Adjustable Version Only) | $V_{out}$ | 1.25 | 5.0 | V |
| Operating Ambient Temperature Range | $T_A$ | −40 | 125 | °C |

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. Minimum $V_{in}$ = 1.75 V or ($V_{out}$ + $V_{DO}$), whichever is higher.

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 1.750 V, $V_{out}$ = 1.250 V (adjustable version)), ($V_{in}$ = $V_{out}$ + 0.5 V (fixed version)), $C_{in}$ = $C_{out}$ =1.0 μF, −40°C ≤ $T_A$ ≤ 125°C, Figure 5, unless otherwise specified.) (Note 8)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| Disable Current | $I_{DIS}$ | ENABLE = 0 V, Vin = 6 V<br>−40°C ≤ $T_A$ ≤ 85°C | – | 0.01 | 1.0 | μA |
| Ground Current<br>Adjustable Option<br>1.3 V Option<br>1.5 V Option<br>1.8 V to 3.0 V Option<br>3.3 V to 5.0 V Option | $I_{GND}$ | ENABLE = 0.9 V,<br>$I_{out}$ = 1.0 mA to 150 mA | <br>–<br>–<br>–<br>–<br>– | <br>100<br>135<br>135<br>140<br>145 | <br>135<br>150<br>170<br>175<br>180 | μA |
| Thermal Shutdown Temperature (Note 9) | $T_{SD}$ | | 150 | 175 | 200 | °C |
| Thermal Shutdown Hysteresis | $T_{SH}$ | | – | 10 | – | °C |
| ADJ Input Bias Current | $I_{ADJ}$ | | −0.75 | – | 0.75 | μA |
| **CHIP ENABLE** | | | | | | |
| ENABLE Input Threshold Voltage<br>Voltage Increasing, Logic High<br>Voltage Decreasing, Logic Low | $V_{th(EN)}$ | | <br>0.9<br>– | <br>–<br>– | <br>–<br>0.4 | V |
| Enable Input Bias Current (Note 9) | $I_{EN}$ | | – | 3.0 | 100 | nA |
| **TIMING** | | | | | | |
| Output Turn On Time<br>Adjustable Option<br>1.3 V to 3.5 V Option<br>5.0 V Option | $t_{EN}$ | ENABLE = 0 V to $V_{in}$ | <br>–<br>–<br>– | <br>15<br>15<br>30 | <br>25<br>25<br>50 | μs |

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization, production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Values based on design and/or characterization.


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## ELECTRICAL CHARACTERISTICS

($V_{in}$ = 1.750 V, $V_{out}$ = 1.250 V, $C_{in}$ = $C_{out}$ =1.0 μF, −40°C ≤ $T_A$ ≤ 125°C, Figure 5, unless otherwise specified.) (Note 10)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REGULATOR OUTPUT (Adjustable Voltage Version)** | | | | | | |
| Output Voltage | $V_{out}$ | $I_{out}$ = 1.0 mA to 150 mA<br>$V_{in}$ = 1.75 V to 6.0 V,<br>$V_{out}$ = ADJ | 1.231<br>(−1.5%) | 1.250 | 1.269<br>(+1.5%) | V |
| Ripple Rejection<br>($V_{in}$ = $V_{out}$ + 1.0 V + 0.5 $V_{p-p}$) | RR | $I_{out}$ = 1.0 mA to 150 mA<br>f = 120 Hz<br>f = 1.0 kHz<br>f = 10 kHz | <br>–<br>–<br>– | <br>62<br>55<br>38 | <br>–<br>–<br>– | dB |
| Line Regulation | $Reg_{line}$ | $V_{in}$ = 1.750 V to 6.0 V,<br>$I_{out}$ = 1.0 mA | – | 1.0 | 10 | mV |
| Load Regulation | $Reg_{load}$ | $I_{out}$ = 1.0 mA to 150 mA | – | 2.0 | 15 | mV |
| Output Noise Voltage (Note 11) | $V_n$ | f = 10 Hz to 100 kHz | – | 50 | – | $\mu V_{rms}$ |
| Output Short Circuit Current | $I_{sc}$ | | 300 | 550 | 800 | mA |
| Dropout Voltage<br>$V_{out}$ = 1.25 V<br>$V_{out}$ = 1.3 V<br>$V_{out}$ = 1.5 V<br>$V_{out}$ = 1.8 V<br>$V_{out}$ = 2.5 V<br>$V_{out}$ ≥ 2.8 V | $V_{DO}$ | Measured at: $V_{out}$ − 2.0%,<br>$I_{out}$ = 150 mA, Figure 6 | <br>–<br>–<br>–<br>–<br>–<br>– | <br>175<br>175<br>150<br>125<br>100<br>75 | <br>250<br>250<br>225<br>175<br>150<br>125 | mV |
| **REGULATOR OUTPUT (Fixed Voltage Version)**<br>($V_{in}$ = $V_{out}$ + 0.5 V, $C_{in}$ = $C_{out}$ =1.0 μF, −40°C ≤ $T_A$ ≤ 125°C, Figure 7, unless otherwise specified.) (Note 10) | | | | | | |
| Output Voltage<br>1.3 V Option<br>1.5 V Option<br>1.8 V Option<br>2.5 V Option<br>2.8 V Option<br>3.0 V Option<br>3.3 V Option<br>3.5 V Option<br>5.0 V Option | $V_{out}$ | $I_{out}$ = 1.0 mA to 150 mA<br>$V_{in}$ = ($V_{out}$ + 0.5 V) to 6.0 V | <br>1.274<br>1.470<br>1.764<br>2.450<br>2.744<br>2.940<br>3.234<br>3.430<br>4.900<br>(−2%) | | <br>1.326<br>1.530<br>1.836<br>2.550<br>2.856<br>3.060<br>3.366<br>3.570<br>5.100<br>(+2%) | V |
| Power Supply Ripple Rejection (Note 11)<br>($V_{in}$ = $V_{out}$ + 1.0 V + 0.5 $V_{p-p}$) | PSRR | $I_{out}$ = 1.0 mA to 150 mA<br>f = 120 Hz<br>f = 1.0 kHz<br>f = 10 kHz | <br>–<br>–<br>– | <br>62<br>55<br>38 | <br>–<br>–<br>– | dB |
| Line Regulation | $Reg_{line}$ | $V_{in}$ = 1.750 V to 6.0 V,<br>$I_{out}$ = 1.0 mA | – | 1.0 | 10 | mV |
| Load Regulation<br>1.3 V to 1.5 V Option<br>1.8 V Option<br>2.5 V to 5.0 V Option | $Reg_{load}$ | $I_{out}$ = 1.0 mA to 150 mA | <br>–<br>–<br>– | <br>2.0<br>2.0<br>2.0 | <br>20<br>25<br>30 | mV |
| Output Noise Voltage (Note 11) | $V_n$ | f = 10 Hz to 100 kHz | – | 50 | – | $\mu V_{rms}$ |
| Output Short Circuit Current | $I_{sc}$ | | 300 | 550 | 800 | mA |
| Dropout Voltage<br>1.3 V Option<br>1.5 V Option<br>1.8 V Option<br>2.5 V Option<br>2.8 V to 5.0 V Option | $V_{DO}$ | Measured at: $V_{out}$ − 2.0% | <br>–<br>–<br>–<br>–<br>– | <br>175<br>150<br>125<br>100<br>75 | <br>250<br>225<br>175<br>150<br>125 | mV |

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization, production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Values based on design and/or characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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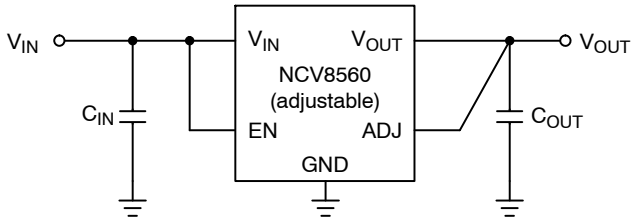


**Figure 5. Typical Application Circuit for $V_{out}$ = 1.25 V (Adjustable Version)**

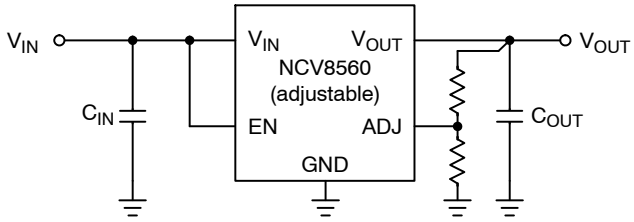


**Figure 6. Typical Application Circuit for Adjustable $V_{out}$**

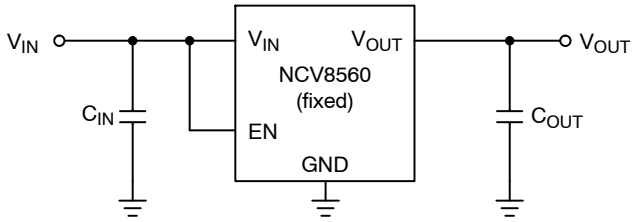


**Figure 7. Typical Application Circuit (Fixed Voltage Version)**



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## TYPICAL CHARACTERISTICS

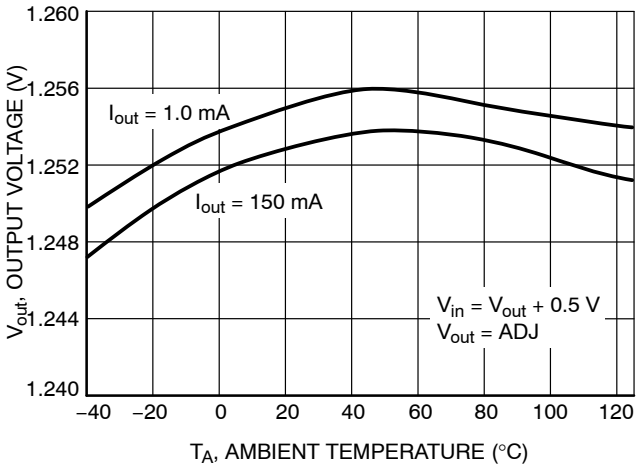


**Figure 8. Output Voltage vs. Temperature ($V_{in}$ = $V_{out}$ + 0.5 V)**

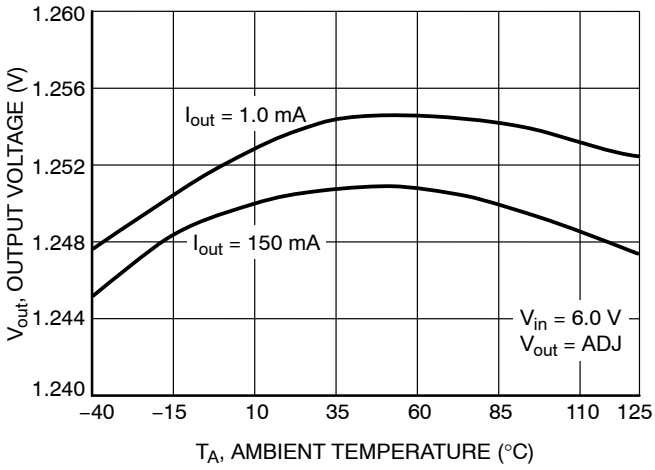


**Figure 9. Output Voltage vs. Temperature ($V_{in}$ = 6.0 V)**

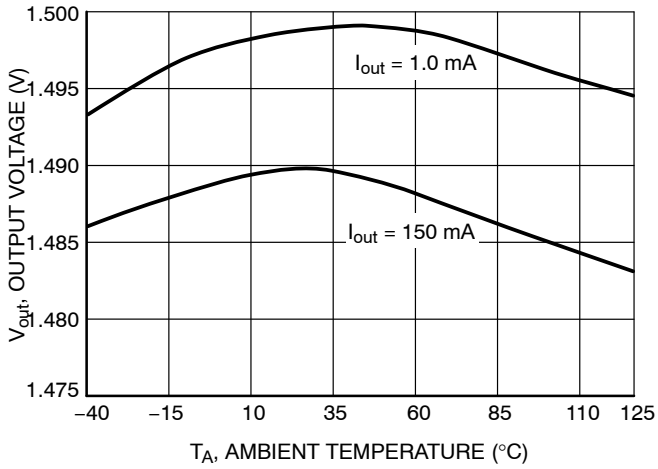


**Figure 10. Output Voltage vs. Temperature (1.5 V Fixed Output, $V_{in}$ = 2 V)**

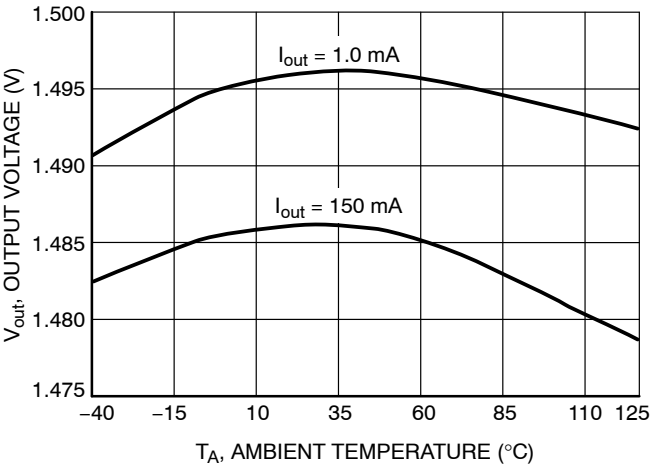


**Figure 11. Output Voltage vs. Temperature (1.5 V Fixed Output, $V_{in}$ = 6 V)**

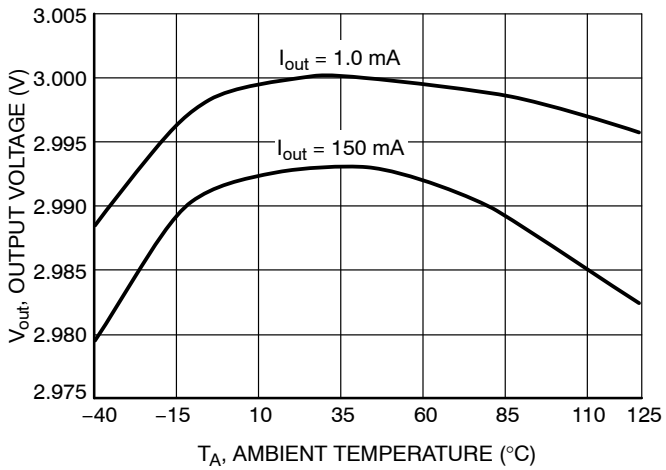


**Figure 12. Output Voltage vs. Temperature (3.0 V Fixed Output, $V_{in}$ = 3.5 V)**

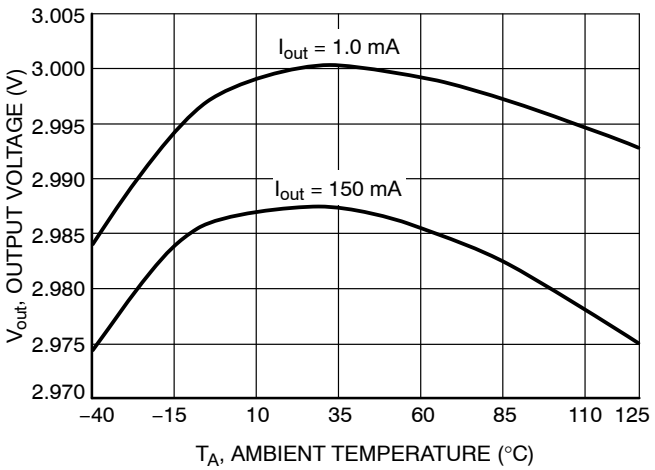


**Figure 13. Output Voltage vs. Temperature (3.0 V Fixed Output, $V_{in}$ = 6 V)**



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## TYPICAL CHARACTERISTICS

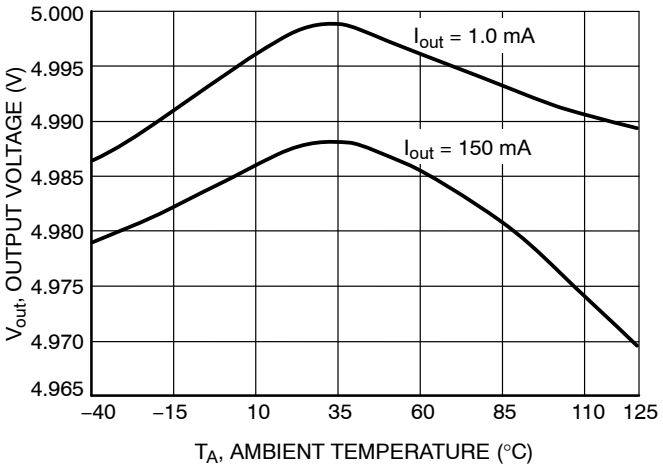


**Figure 14. Output Voltage vs. Temperature (5.0 V Fixed Output, $V_{in}$ = 5.5 V)**

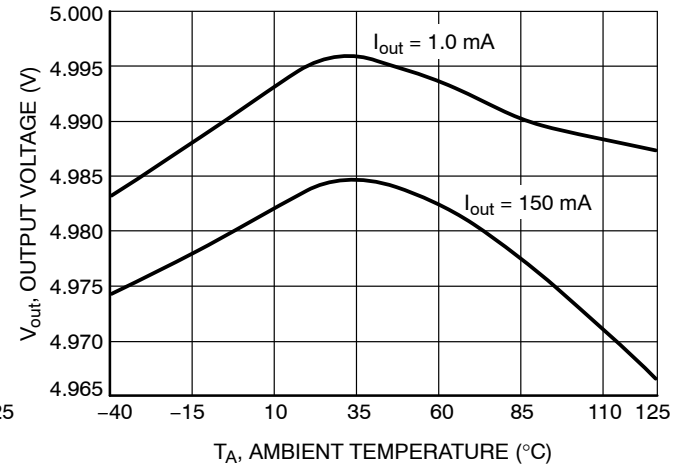


**Figure 15. Output Voltage vs. Temperature (5.0 V Fixed Output, $V_{in}$ = 6 V)**

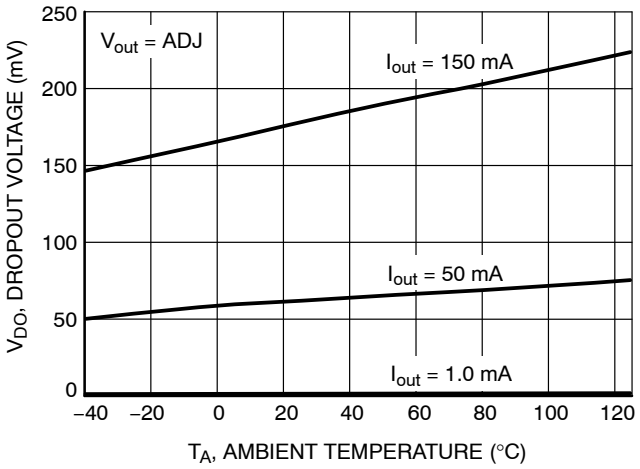


**Figure 16. Dropout Voltage vs. Temperature (Over Current Range)**

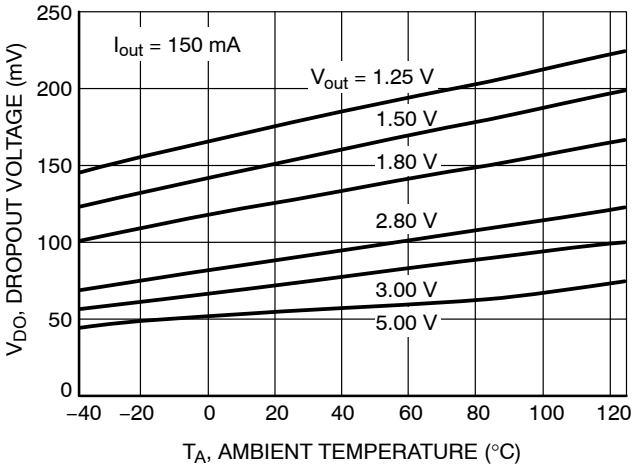


**Figure 17. Dropout Voltage vs. Temperature (Over Output Voltage)**

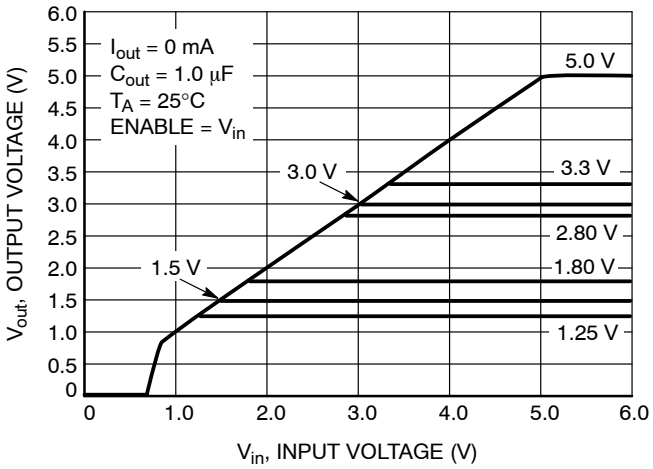


**Figure 18. Output Voltage vs. Input Voltage**

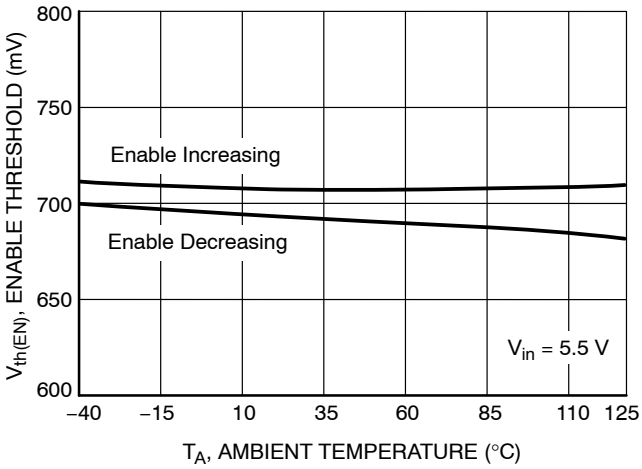


**Figure 19. Enable Threshold vs. Temperature**



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## TYPICAL CHARACTERISTICS

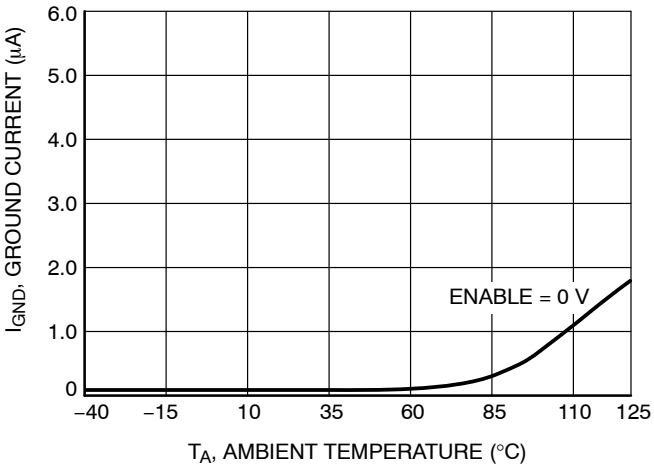


**Figure 20. Ground Current (Sleep Mode) vs. Temperature**

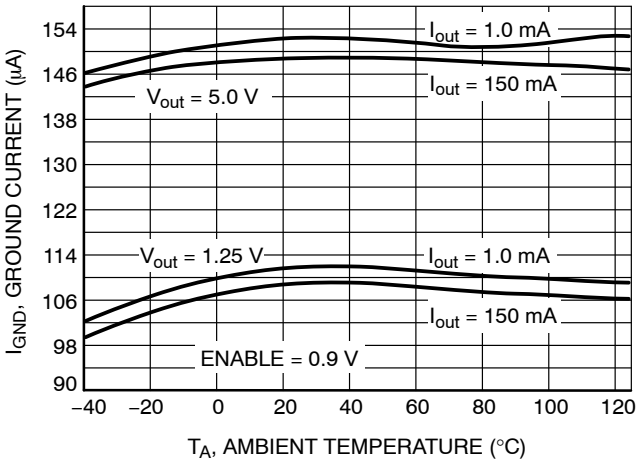


**Figure 21. Ground Current (Run Mode) vs. Temperature**

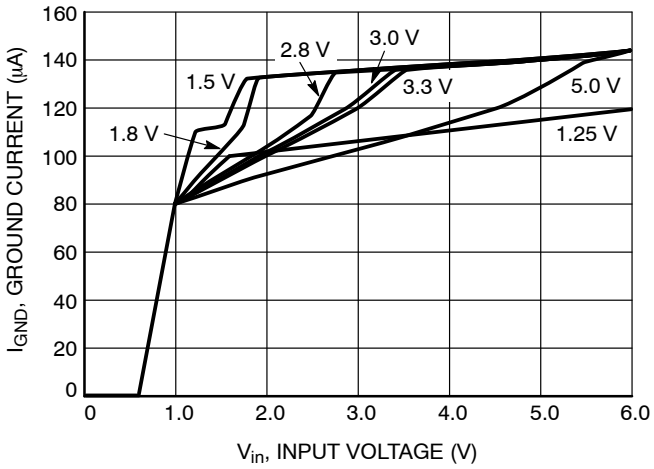


**Figure 22. Ground Current vs. Input Voltage**

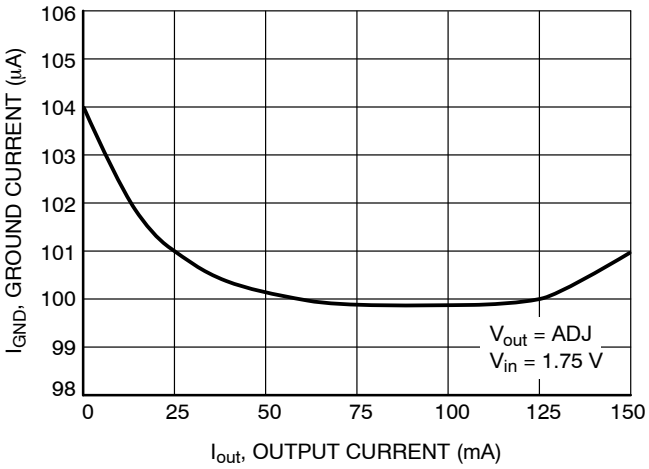


**Figure 23. Ground Current vs. Output Current**

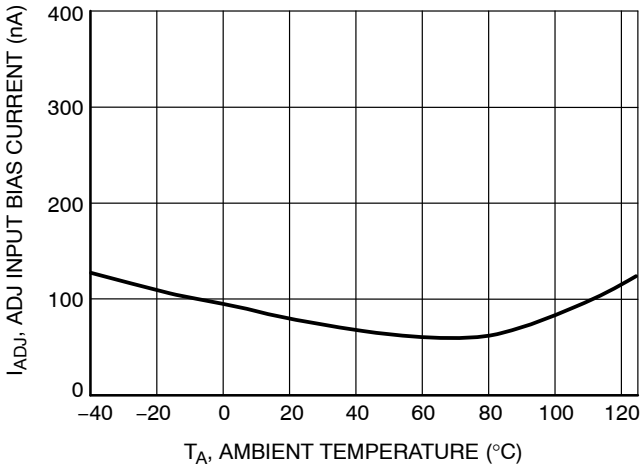


**Figure 24. ADJ Input Bias Current vs. Temperature**



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## TYPICAL CHARACTERISTICS

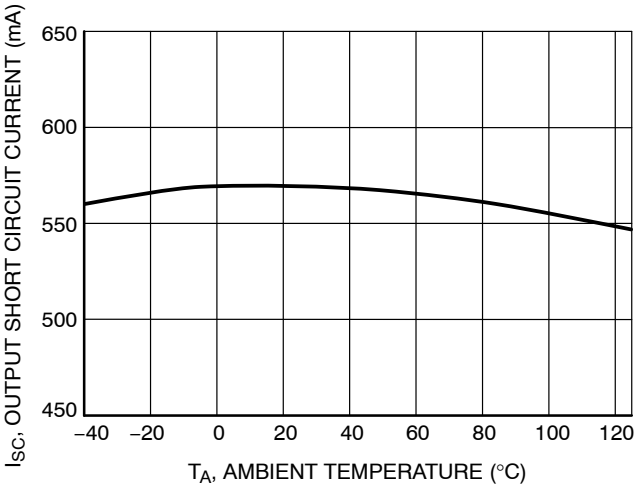


**Figure 25. Output Short Circuit Current vs. Temperature**

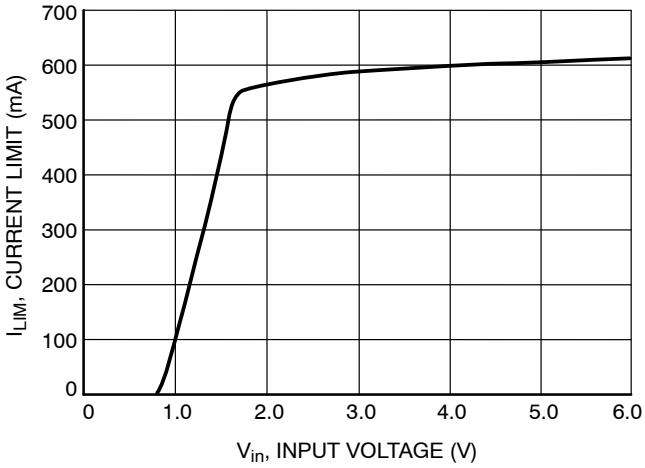


**Figure 26. Current Limit vs. Input Voltage**

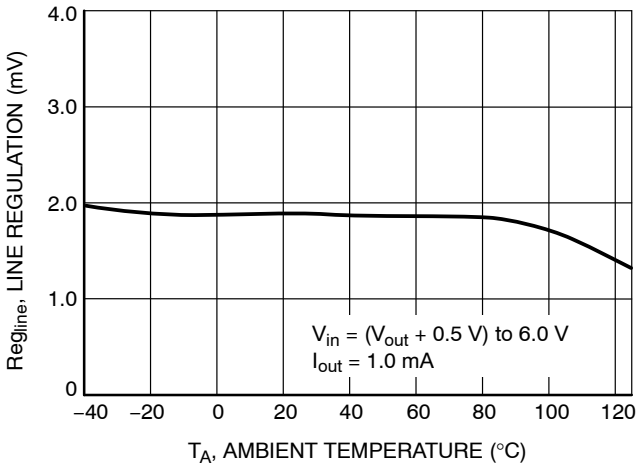


**Figure 27. Line Regulation vs. Temperature**

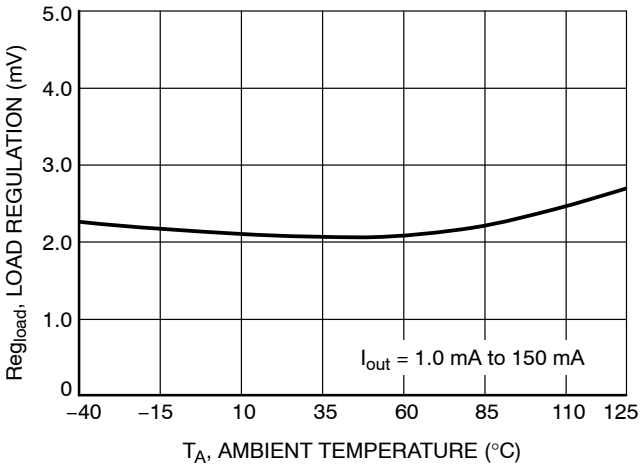


**Figure 28. Load Regulation vs. Temperature**

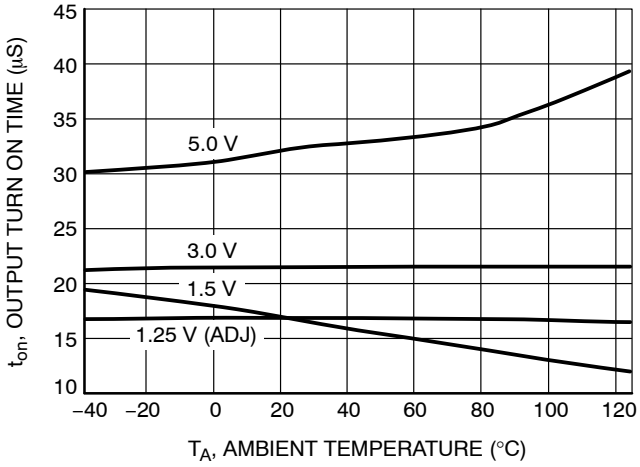


**Figure 29. Output Turn On Time vs. Temperature**

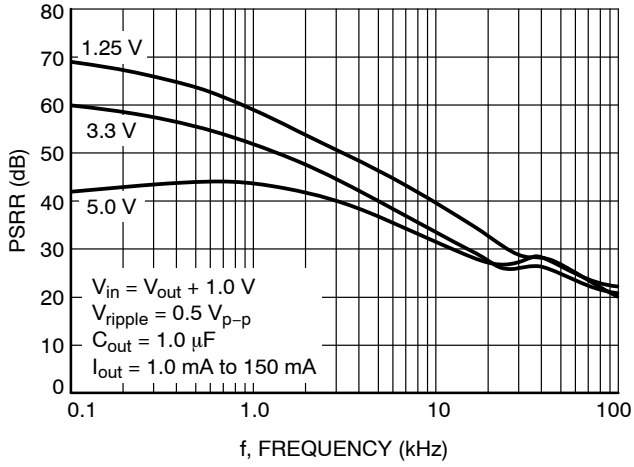


**Figure 30. Power Supply Ripple Rejection vs. Frequency**



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## TYPICAL CHARACTERISTICS

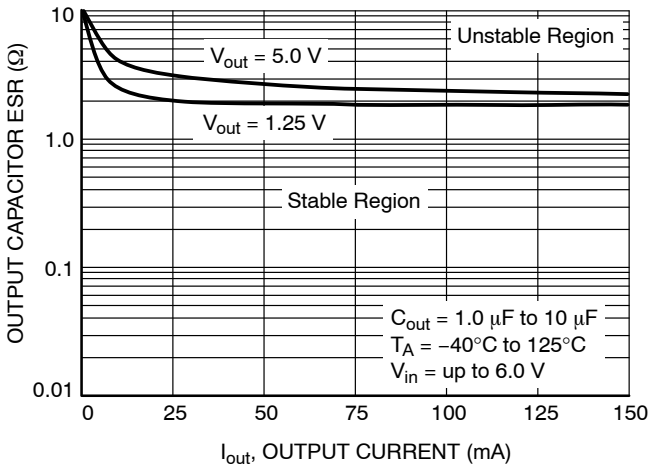


**Figure 31. Output Stability with Output Capacitor ESR over Output Current**

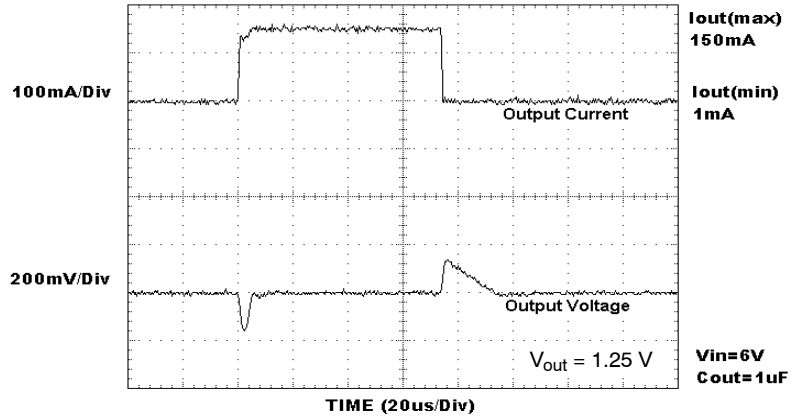


**Figure 32. Load Transient Response (1.0 μF)**

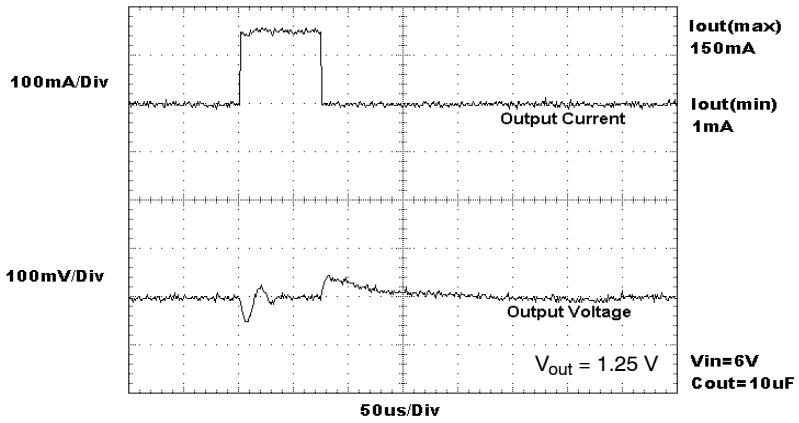


**Figure 33. Load Transient Response (10 μF)**



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## DEFINITIONS

### Load Regulation

The change in output voltage for a change in output load current at a constant temperature.

### Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

### Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in $\mu V_{rms}$ or $nV/\sqrt{Hz}$.

### Ground Current

Ground Current ($I_{GND}$) is the current that flows through the ground pin when the regulator operates with a load on its output. This consists of internal IC operation, bias, etc. It is actually the difference between the input current (measured through the LDO input pin) and the output load current. If the regulator has an input pin that reduces its internal bias and shuts off the output (enable/disable function), this term is called the disable current ($I_{DIS}$).

### Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average junction temperature is not significantly affected.

### Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

### Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between no−load and full−load conditions.

### Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

### Maximum Package Power Dissipation

The power dissipation level at which the junction temperature reaches its maximum operating value.

## APPLICATIONS INFORMATION

The NCV8560 series regulator is self−protected with internal thermal shutdown and internal current limit. Typical application circuits are shown in Figures 5 and 6.

### Input Decoupling ($C_{in}$)

A ceramic or tantalum 1.0 μF capacitor is recommended and should be connected close to the NCV8560 package. Higher capacitance and lower ESR will improve the overall line transient response.

### Output Decoupling ($C_{out}$)

The NCV8560 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response. Figure 31 shows the stability region for a range of operating conditions and ESR values.

### No−Load Regulation Considerations

The NCV8560 adjustable regulator will operate properly under conditions where the only load current is through the resistor divider that sets the output voltage. However, in the case where the NCV8560 is configured to provide a 1.250 V output, there is no resistor divider. If the part is enabled under no−load conditions, leakage current through the pass transistor at junction temperatures above 85°C can approach several microamps, especially as junction temperature approaches 150°C. If this leakage current is not directed into a load, the output voltage will rise up to a level approximately 20 mV above nominal.

The NCV8560 contains an overshoot clamp circuit to improve transient response during a load current step release. When output voltage exceeds the nominal by approximately 20 mV, this circuit becomes active and clamps the output from further voltage increase. Tying the ENABLE pin to $V_{in}$ will ensure that the part is active whenever the supply voltage is present, thus guaranteeing that the clamp circuit is active whenever leakage current is present.

When the NCV8560 adjustable regulator is disabled, the overshoot clamp circuit becomes inactive and the pass transistor leakage will charge any capacitance on $V_{out}$. If no load is present, the output can charge up to within a few millivolts of $V_{in}$. In most applications, the load will present some impedance to $V_{out}$ such that the output voltage will be inherently clamped at a safe level. A minimum load of 10 μA is recommended.



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### Noise Decoupling

The NCV8560 is a low noise regulator and needs no external noise reduction capacitor. Unlike other low noise regulators which require an external capacitor and have slow startup times, the NCV8560 operates without a noise reduction capacitor, has a typical 15 μs start up delay and achieves a 50 $\mu V_{rms}$ overall noise level between 10 Hz and 100 kHz.

### Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. The turn−on/turn−off transient voltage being supplied to the enable pin should exceed a slew rate of 10 mV/μs to ensure correct operation. If the enable function is not to be used then the pin should be connected to $V_{in}$.

### Output Voltage Adjust

The output voltage can be adjusted from 1 times (Figure 5) to 4 times (Figure 6) the typical 1.250 V regulation voltage via the use of resistors between the output and the ADJ input. The output voltage and resistors are chosen using Equation 1 and Equation 2.

$$V_{out} = 1.250\left(1 + \frac{R_1}{R_2}\right) + \left(I_{ADJ} \times R_1\right) \quad \text{(eq. 1)}$$

$$R_2 \cong \frac{R_1}{\frac{V_{out}}{1.25} - 1} \quad \text{(eq. 2)}$$

Input bias current $I_{ADJ}$ is typically less than 150 nA. Choose R2 arbitrarily to minimize errors due to the bias current and to minimize noise contribution to the output voltage. Use Equation 2 to find the required value for R1.

### Thermal

As power in the NCV8560 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8560 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8560 can handle is given by:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad \text{(eq. 3)}$$

Since $T_J$ is not recommended to exceed 125°C ($T_{J(MAX)}$), then the NCV8560 in a DFN6 package can dissipate up to 600 mW when the ambient temperature ($T_A$) is 25°C, and PCB area is 150mm$^2$ and larger, see Figure 34.

The power dissipated by the NCV8560 can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_{GND} @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 4)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_{GND}} \quad \text{(eq. 5)}$$

If a 150 mA output current is needed, the quiescent current $I_{GND}$ is taken from the data sheet electrical characteristics table or extracted from Figure 21 and Figure 23. $I_{GND}$ is approximately 108 μA when $I_{out}$ = 150 mA. For an output voltage of 1.250 V, the maximum input voltage will then be 3.9 V, good for a 1 Cell Li−ion battery.

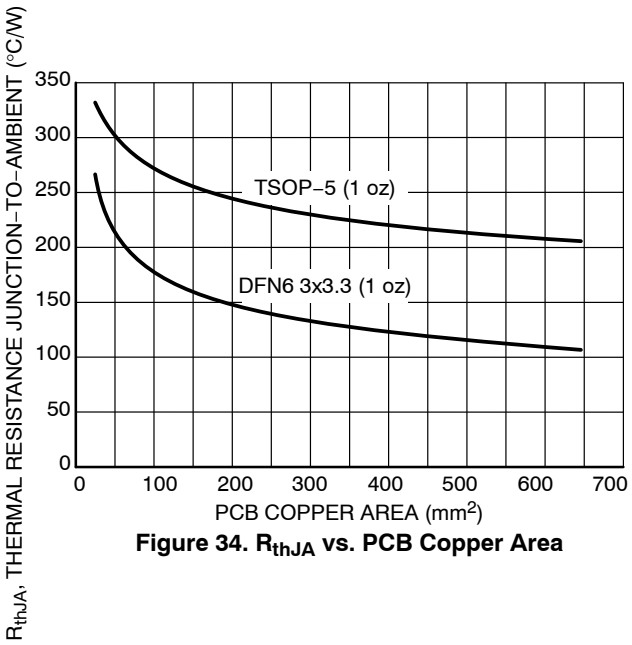


**Figure 34. $R_{thJA}$ vs. PCB Copper Area**

### Hints

$V_{in}$ and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8560, and make traces as short as possible.



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## DEVICE ORDERING INFORMATION

| Device* | Marking Code | Version | Package | Shipping† |
|---|---|---|---|---|
| NCV8560MN150R2G | 1st Line: V8560<br>2nd Line: 150 | 1.5 V | DFN6 (3x3)<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560MN330R2G | 1st Line: V8560<br>2nd Line: 330 | 3.3 V | | |
| NCV8560SN130T1G | LJ2 | 1.3 V | TSOP−5<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560SN180T1G | LJ3 | 1.8 V | | |
| NCV8560SN250T1G | AAQ | 2.5 V | | |
| NCV8560SN280T1G | AAR | 2.8 V | | |
| NCV8560SN330T1G | LJ5 | 3.3 V | | |
| NCV8560SN350T1G | LJ7 | 3.5 V | | |

**DISCONTINUED** (Note 12)

| | | | | |
|---|---|---|---|---|
| NCV8560MNADJR2G | 1st Line: V8560<br>2nd Line: ADJ | ADJ | DFN6 (3x3)<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560MN180R2G | 1st Line: V8560<br>2nd Line: 180 | 1.8 V | DFN6 (3x3)<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560MN250R2G | 1st Line: V8560<br>2nd Line: 250 | 2.5 V | | |
| NCV8560MN280R2G | 1st Line: V8560<br>2nd Line: 280 | 2.8 V | | |
| NCV8560MN300R2G | 1st Line: V8560<br>2nd Line: 300 | 3.0 V | | |
| NCV8560MN350R2G | 1st Line: V8560<br>2nd Line: 350 | 3.5 V | DFN6 (3x3)<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560MN500R2G | 1st Line: V8560<br>2nd Line: 500 | 5.0 V | | |
| NCV8560MN130R2G | 1st Line: AQ(M) | 1.3 V | DFN6 (2x2.2)<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560SNADJT1G | LJ9 | ADJ | TSOP−5<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560SN150T1G | AAJ | 1.5 V | TSOP−5<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560SN300T1G | LJ4 | 3.0 V | TSOP−5<br>(Pb−Free) | 3000 / Tape & Reel |
| NCV8560SN500T1G | LJ8 | 5.0 V | TSOP−5<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

12. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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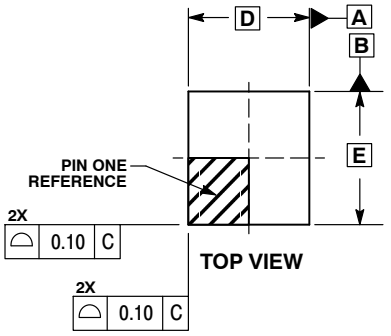
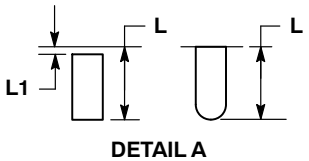
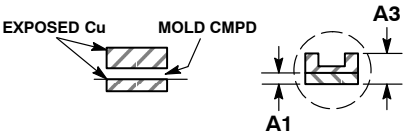
## PACKAGE DIMENSIONS

**DFN6, 2x2.2, 0.65P**
CASE 506BA−01
ISSUE A

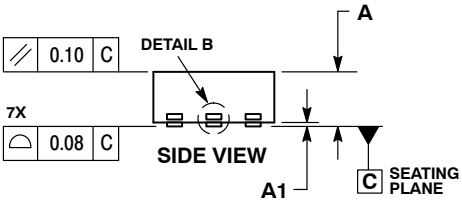


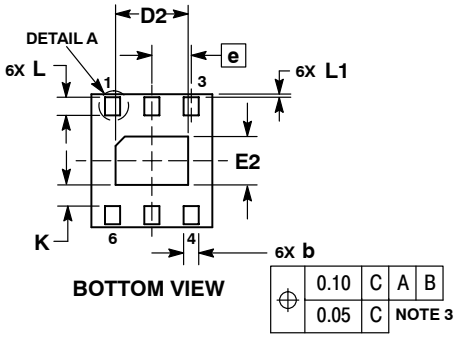




**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**




**DETAIL B**
**ALTERNATE CONSTRUCTIONS**

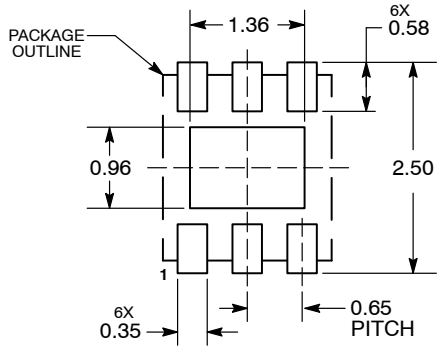



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.20 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.65 BSC | |
| K | 0.20 | --- |
| L | 0.25 | 0.35 |
| L1 | 0.00 | 0.10 |

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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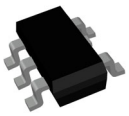
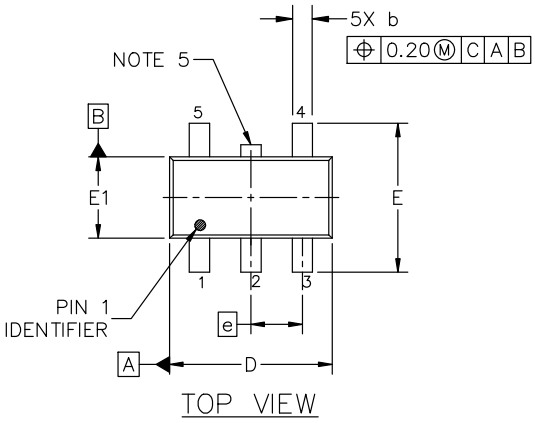
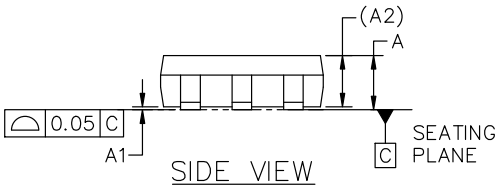


**TSOP−5 3.00x1.50x0.95, 0.95P**
CASE 483
ISSUE P

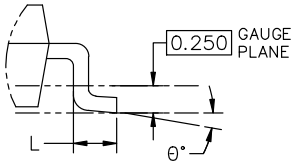
DATE 01 APR 2024



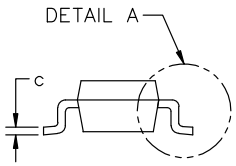

TOP VIEW




SIDE VIEW




DETAIL "A"
SCALE 2:1



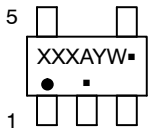

END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

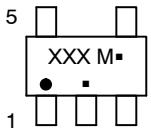
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.900 | 1.000 | 1.100 |
| A1 | 0.010 | 0.055 | 0.100 |
| A2 | | 0.950 REF. | |
| b | 0.250 | 0.375 | 0.500 |
| c | 0.100 | 0.180 | 0.260 |
| D | 2.850 | 3.000 | 3.150 |
| E | 2.500 | 2.750 | 3.000 |
| E1 | 1.350 | 1.500 | 1.650 |
| e | | 0.950 BSC | |
| L | 0.200 | 0.400 | 0.600 |
| θ | 0° | 5° | 10° |

**GENERIC**
**MARKING DIAGRAM***




**Analog**

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

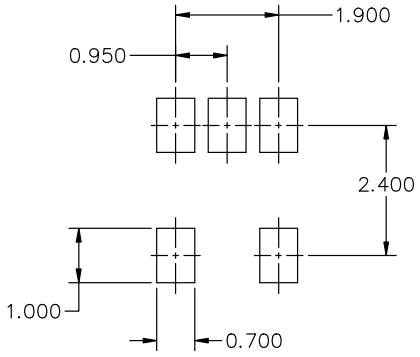



**Discrete/Logic**

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ARB18753C** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **TSOP−5 3.00x1.50x0.95, 0.95P** | **PAGE 1 OF 1** |

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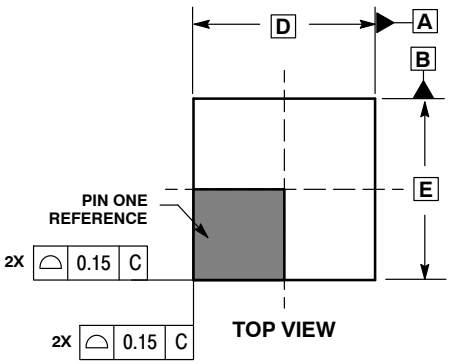
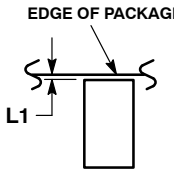
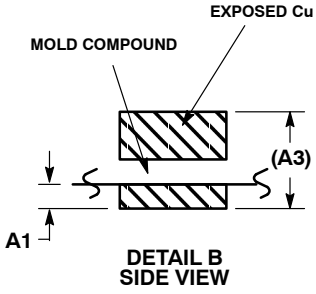
**6 PIN DFN, 3x3x0.9**
CASE 488AE
ISSUE B

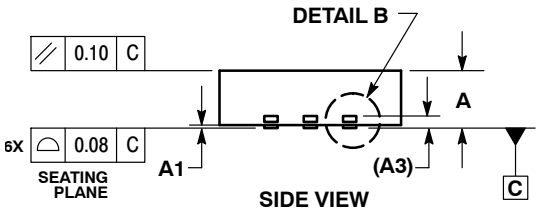
DATE 30 NOV 2005

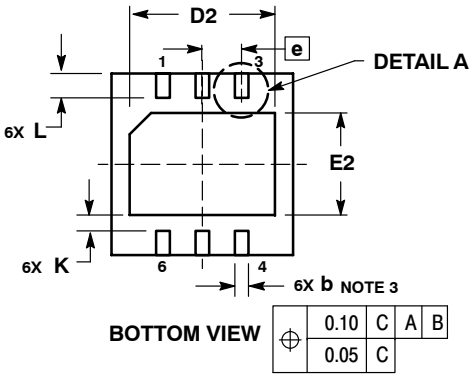
**SCALE 2:1**




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | 0.25 |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 2.25 | 2.55 |
| E | 3.00 BSC | |
| E2 | 1.55 | 1.85 |
| e | 0.65 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.021 |

## GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **6 PIN DFN, 3X3X0.9 MM, 0.65 MM PITCH** | | **PAGE 1 OF 1** |

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